14.4 A 3D Integration Scheme utilizing Wireless Interconnections for Implementing Hyper Brains

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In order to break Moore's law by 3D integration, innovative solutions for inter- and intra-chip interconnections have to be developed. Inter-chip interconnection technologies using via-holes have been developed however their associated fabrication cost and yield are still unacceptable. To overcome these problems, wireless interconnects using capacitive coupling of small pads [1] or inductive coupling of on-chip spiral inductors [2] are proposed. With the former technique, since a pair of pads formed on different chips must couple with an insulation layer with the thickness of 1 to 2μm, the problems are not satisfactorily solved. The latter technique consumes large power of more than 10mW for a single interconnect. Therefore, expected requirements of over 1000 connections between chips cannot be realized in practice.

Another bottleneck for 3D integration lies in the processing algorithm and architecture of conventional Neumann computers. Although living systems use a vast number of mutually connected neural cells that are sensitive to noise, these systems achieve highly sophisticated capabilities with sufficiently high reliability. To mimic biological systems, a processing architecture for aggregating information and making perspective judgment based on the advanced interconnection techniques is developed.

From the view point of a complete system, global interconnects throughout whole chips and local parallel interconnects between adjacent chips are required. The former is used for system clocking over 10GHz as well as busses that enables synchronous processing and accessing to a G-byte database. The latter transfers 2D data such as image data, without the requirement of gathering and multiplexing.

The proposed local wireless interconnection scheme (LWI) between chips utilizes the principle of magnetic coupling and resonance of on-chip spiral inductors. A circuit schematic and an inductor structure are shown in Fig. 14.4.1. TX consists of a switching MOST and a pulse shaper, and RX consists of an LC resonator, a detector, and a reconstruction FF. Current and voltage characteristics of the circuit are also shown in Fig. 14.4.1. To optimize transmission delay and power dissipation, the pulse width is set to the time when the inductor current (i_L) reaches its maximum value. FDTD analysis and circuit simulation show found that the inductor size (L_{ind}) should be larger than twice of the inductor distance (t_{chip}) to obtain a large enough coupling coefficient (k). These sizes are scalable under a constant current condition.

The test chip is developed with a 0.25μm CMOS technology. Two chips are mounted on manipulators for measuring the transfer characteristics. Measured results are also shown in Fig. 14.4.1. A data rate of 800Mb/s is obtained at supply voltage of 2.5V and power consumption of 9mW. By circuit simulation using 0.18μm CMOS devices, 2Gb/s data rate are obtained with only 1mW power dissipation. The LWI can be applied to asynchronous interconnects corresponding to wires as well as synchronous systems using a global clock. By optimizing inductor size, chip thickness and power dissipation, it is possible to transfer data in highly parallel form between neighboring chips.

A multi-chip vision (MCV) system based on hierarchical biological processing is investigated. An MCV test chip that consists of a pixel array and a PWM-based line parallel I/O is implemented in a 0.35μm CMOS technology. Two MCV chips are connected with two LWI chips using analog PWM signaling as shown in Fig. 14.4.2. The pixel output voltage of MCV1 is modulated to an analog PWM signal. It is re-modulated to the RZ signal and drives the TX MOST. The received signal is detected by a comparator and reconstructed to the original PWM signal. The PWM signals are then demodulated to the analog signals. Measured waveforms are shown in Fig. 14.4.3. P_{1o} and P_{2i} are the PWM output of MCV1 and the PWM input to MCV2, respectively. In the experiment, since 1760 pixel data are transferred across only one LWI channel, a long period of 3.17ms is needed. If a column parallel scheme is applied, this transfer time is drastically reduced. The time resolution is 2.5ns, which is limited by the comparator response delay due to the 0.35μm CMOS device speed. $v_o(1)$ and $v_o(2)$ are output voltages, without smoothing and with smoothing, respectively. The 8b accuracy is obtained by PWM analog data transfer using LWI.

The proposed global wireless interconnection (GWI) utilizes high-frequency electromagnetic (EM) wave transmission using integrated antennas [3] and an ultra-wideband (UWB) transceiver system. EM wave propagation characteristics through stacked silicon substrates are measured using integrated dipole antennas, as shown in Fig. 14.4.4. A 20GHz sinusoidal wave propagates with a low loss of 0.14dB/chip through Si chips with increased substrate resistivity of 2.29kΩ-cm. Clock distribution at over 10GHz can be implemented with a sinusoidal wave transmission. UWB monocycle pulse transmission characteristics are also measured and a low loss of 0.24dB/chip is obtained. Experimental UWB TX and RX chips are designed with a 0.18μm CMOS technology. A bit rate of 50Mb/s and 8-channel multiplex are obtained by simulation. Influence of the EM wave on circuit operations and interference with external EM waves are now under investigation.

3D integration using GWI and LWI, called 3-dimensional custom stack system (*3DCSS*), is proposed. By the *3DCSS* concept, over 10 chips can be stacked as shown in Fig. 14.4.5. Required alignment accuracy of chips is very relaxed and as low as about half of the inductor size. Power/Ground pins are bonded with existing techniques. The feature of *3DCSS* is to realize a flexible customized system integrating various kinds of chips with a wireless interface. Yield and known-good-die problems are also resolved by chip testing using wireless pads.

For implementing a hyper brain, the concept of a multi-object recognition system using the *3DCSS* approach is studied. The principal component analysis and the eigen face method for realizing multi-object detection and recognition in a natural scene are adopted. The proposed hyper brain is composed of wireless interconnected multiple chips including image sensor, early-vision processor, object detector, feature detector, object recognizer, and database, as shown in Fig. 14.4.6. The expected performance is 10frame/s frame rate, 10 objects and 1000 data/object matching.

Acknowledgement:
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[2] D. Mizoguchi et al. "A 1.2Gb/s/pin Wireless Superconnect Base on Inductive Inter-Chip Signaling (IIS)," *ISSCC Dig.Tech. Papers*, pp. 142-143, Feb., 2004.
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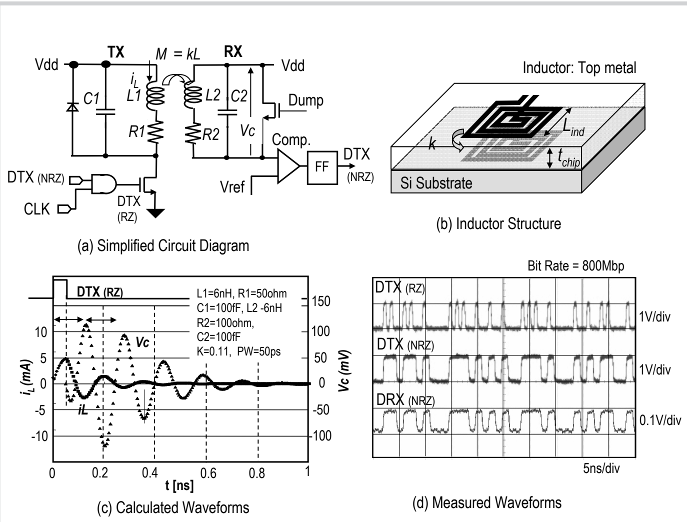

Figure 14.4.1: Wireless interconnect (LWI) based on resonated inductor coupling.

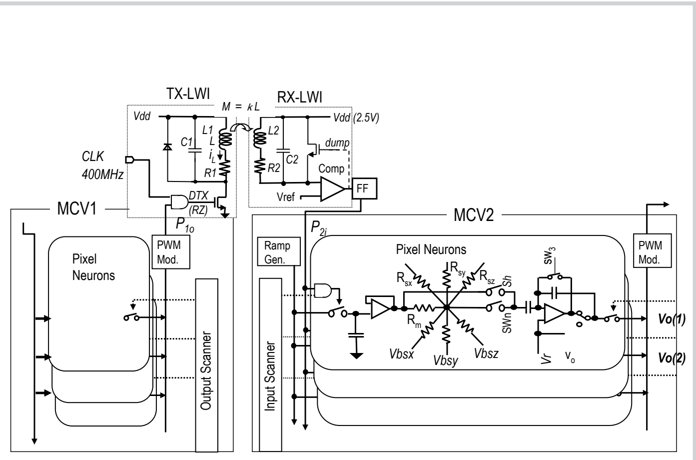

Figure 14.4.2: Experimental setup of multi-chipvVision connected with analog LWIs.

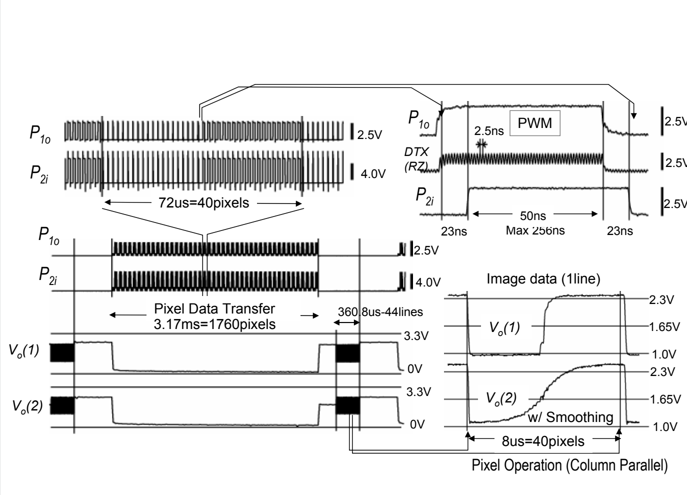

Figure 14.4.3: Measured waveforms of MCV using analog-LWI.

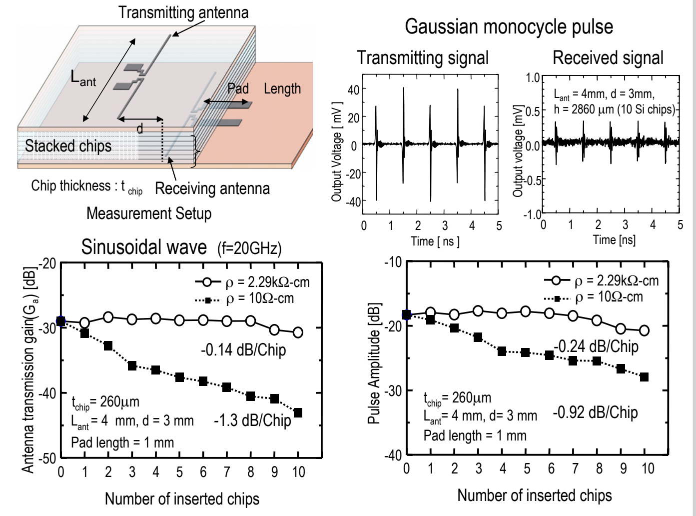

Figure 14.4.4: Measurement results of EM wave transmission through stacked chips.

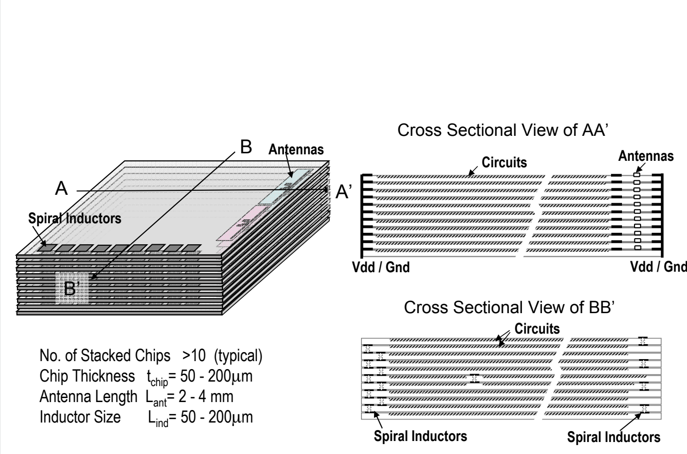

Figure 14.4.5: Structure of 3DCSS.

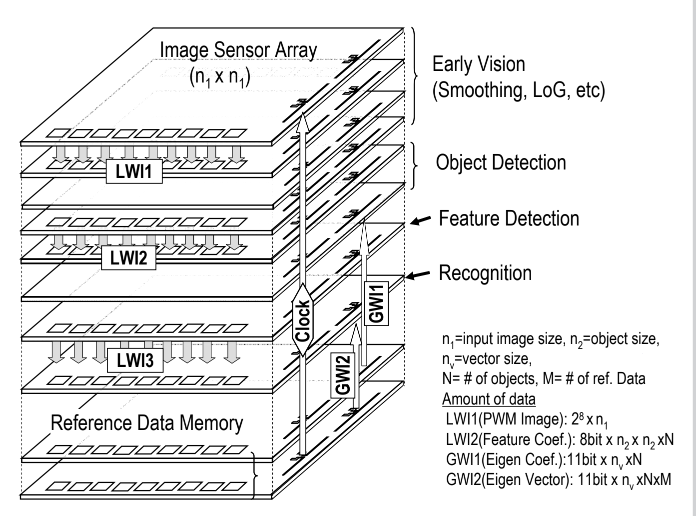

Figure 14.4.6: Schematic view of hyper brain and data transfer.

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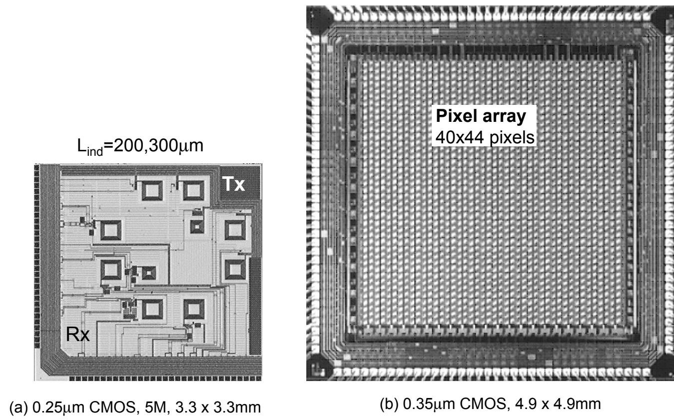

Figure 14.4.7: Test chips for (a) LWI and (b) PWM I/O MCV.

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