A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication Scheme

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Abstract

This paper presents a reduction method of power consumption and an asynchronous communication scheme for spiral-inductor based wireless chip-interconnect. The power reduction is achieved by utilizing positively resonance phenomena between two spiral inductors. Further, employing dynamic circuits and self pre-charging technique realizes an asynchronous communication without any clocking. The methodology was verified and evaluated by measuring a test chip in 0.18µm 6 metal CMOS technology. The performance of 0.95mW/1.0Gbps/ch was achieved without any clocking.

Keyword: wireless chip-interconnect, spiral inductor, 3D-ICs, low power, asynchronous communication

Introduction

With the continuous downsizing of CMOS technology, various components such as processors, memories, analog circuits, RF interface, are integrated in a single chip. It is called a system LSI. However, it takes considerable time to develop system LSIs, and the integration of a wide variety of system functions on a single chip invites considerable low yield. As an alternative, attention has been drawn to the System-in-Package. In a 3D-IC fabrication technique, small stacked via-hole technologies are now under development but the processing cost and yield problems are still unresolved [1]. To solve these problems, wireless interconnect using capacitive coupling between small pads [2] and wireless interconnect based on inductive coupling of spiral inductors [3],[4] were proposed. The former requires small pad-to-pad distance of 1-2µm. The latter is not applicable to parallel connections because of its large power consumption, and it requires a complex synchronization scheme. In this manuscript, a reduction method of power consumption and an asynchronous communication scheme without any clocking are proposed for the spiral-inductor based wireless chip-interconnect. The power reduction is very important for parallel interconnects between neighboring chips, which distribute 2D data such as image data in stacked 3D-IC systems [5].

Reduction of Power Consumption

Figure 1 illustrates the inductive coupling between spiral inductors on stacked silicon chips. The inductive coupling structure has self-resonance frequencies due to relatively large parasitic capacitances, unlike conventional pulse transformers. Although the resonance phenomena are typically awkward, they will be utilized for reducing the power consumption in the wireless chip-interconnect.

As shown in Fig.2, an nMOS FET excites the spiral inductor pair by pulse. The spiral inductors are modeled as π–type equivalent circuits. The magnetic coupling is introduced as a coupling coefficient "k" into the equivalent circuit model. Spice simulation results are shown in Fig.3. Let us consider, first, a case of the wide-width pulse shown at the left hand in the figure. Two damping oscillations appear on the output node (Vout), at the times when the input pulse (Vin) rises and falls. However, the amplitude at the later is larger than the former one. The difference has been caused by on-conductance of the nMOS FET. The former one arises, in case that the input inductor has conductive connection to the ground due to the nMOS FET. On the other

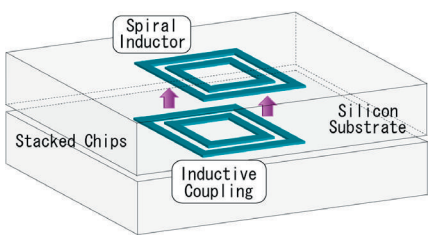

Fig.1 Spiral inductor pair.

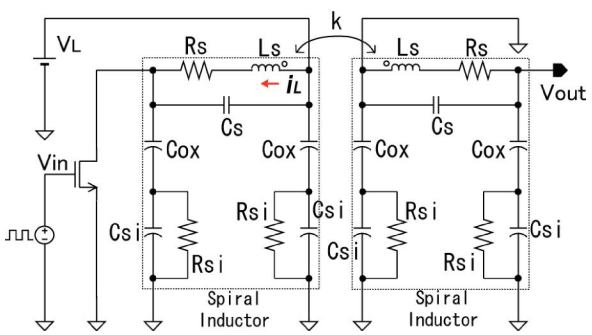

Fig.2 Pulse excitation to spiral inductor pair.

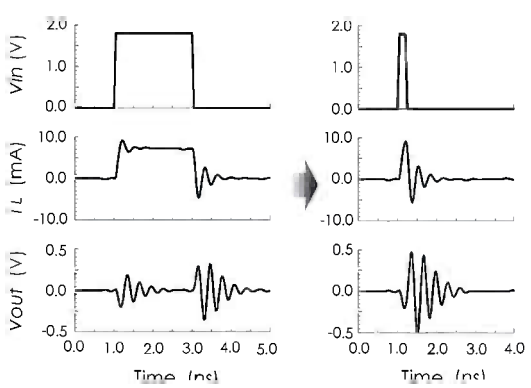

Fig.3 Damping oscillations.

hand, two spiral inductors are identical in the later oscillation, because the nMOS FET is off. The identity enlarges the resonance phenomenon between two spiral inductors and it results in large amplitude of the damping oscillation. Of course, the phenomena become conspicuous when the on-conductance is large. Thus, it is important to generate damping oscillation without on-conductance. Next, let us consider the right hand case in Fig.3. In this case, narrow-width pulse is employed in order to enlarge the amplitude still more, by superposing the two damping oscillations. The pulse width t_{pw} that can superpose the two damping oscillations is :

$$t_{pw} = \frac{1}{2 f_{self}} \tag{1}$$

where f_{self} is the self resonance frequency of the spiral inductor.

The power consumption is dominantly determined by the inductance current i_L. The above techniques enlarging the amplitude result in reduction of the peak value of the inductance current and the narrow-width pulse shortens the time when the current flows into the inductor. Thus, the average of the inductance current i_L becomes small and the power consumption can be drastically reduced.

The self-resonance frequency of the spiral inductor has upper bound because IC fabrication technology restricts narrow pulse generated by typical logic circuits and the self-resonance frequency is related to the pulse width as shown in (1). For example, in a 0.18μm CMOS technology, the lower bound of the pulse width becomes 100-150ps and the self-resonance frequency is restricted below 3.3-5GHz. As well known, parasitic capacitors and resistors of the spiral inductor degrade the amplitude gain in LC oscillator. Hence, the self-resonance frequency of the spiral inductor should be lowered by only increase of the inductance without increase of the parasitic capacitors and resistors. In order to satisfy the requirement, a stacked structure of spiral inductor is employed as shown in Fig.4. The 4-stacked inductor is implemented with 3rd-6th metal layers (the 6th is top metal). The parameters in the π–type equivalent model have been derived by 3-D electromagnetic field solver. The results are described in Table I. In order to realize larger coupling coefficient "k" than 0.1, diameter of spiral inductor is needed with twice as wide as the distance between the inductor pair. The distance is nearly equal to the thickness of the silicon chip. Because the chip thickness (the distance) becomes 100μm in 3D-stacked structure of our prototype system, the diameter is 200μm as shown in Fig.4.

Conductivity of Silicon Substrate

It is feared that conductivity of silicon substrate becomes obstacle to inductive coupling between spiral inductors. The following equation is still held in the spiral inductor coupling :

$$f_{self} << \frac{\sigma}{2\pi \varepsilon_o \varepsilon_r} \tag{2}$$

where σ and ε_r are conductivity and permitivity of silicon substrate, respectively. Hence, attenuation of magnetic field due to silicon substrate can be estimated as illustrated in Fig.5. In the silicon substrate of 100μm thickness, the attenuation is 0.96. The above estimation has been also confirmed by 3D electromagnetic field solver. In fact, the coupling coefficient "k" described in Table I has been calculated on 100μm thickness silicon substrate with 10S/m conductivity (ρ=10Ωcm).

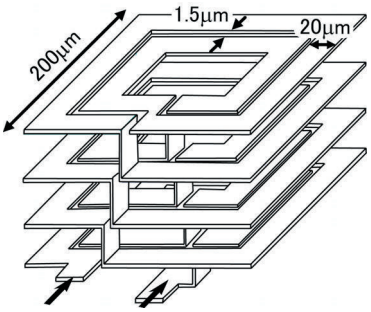

Fig.4 Stacked structure of spiral inductor.

TABLE I PARAMETERS OF SPIRAL INDUCTOR

Ls	17nH	Rsi	920Ω
Cs	95fF	k	0.11
Rs	19Ω	distance	100μm
Cox	180fF	ρ	10Ωcm
Csi	39fF	---	---

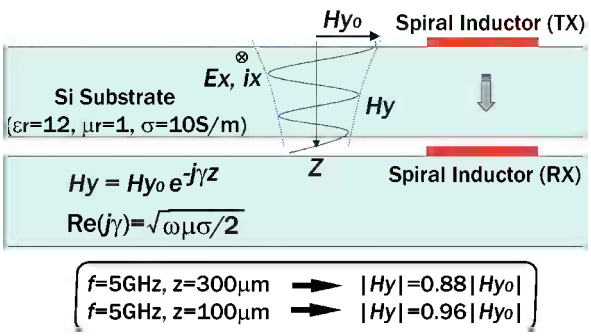

Fig.5 Analysis of silicon substrate conductivity.

Asynchronous Communication Scheme

In order to realize an asynchronous communication without any clocking, dynamic circuits and self pre-charge technique are employed for sensing the received signal. Circuit schematics of a transmitter and a receiver are depicted in Fig.6. Spice simulation results are shown in Fig.7. The received signal indicated by "V_C" is damping oscillation wave and the center voltage is 0V. First, the signal is level-shifted by C1 and R1 to a bias voltage "Vbn" generated by the bias circuit. The shifted signal is indicated by "V_G". The bias voltage "Vbn" can tune the receiving sensitivity by changing the transconductance of M3. The node indicated by "V_D" is dynamically charged up and discharged. M3 discharges the node according to the shifted receiving signal. After discharging, M4 charges up again the node according to the delayed pulse "V_P". This mechanism is called with

"self pre-charging". It can regenerate the transmitted pulse V_{TX}" into the received node "V_{RX}", without any clocking scheme. M2 enlarges the damping in the received wave in order to decrease the signal interference. In order to keep the stable operation of the self pre-charging, the leakage current compensator is prepared. The leakage current of M3 gradually discharges the dynamic node and an erroneous pulse is finally output into "V_{RX}" node. Circuit schematics of the leakage compensator and the bias circuit are depicted in Fig.8. The leakage compensator can distinguish the leakage current and the receiving signal by the low-pass filter composed with M3 and M4. M3 and M4 work as a resistor and a capacitor respectively and they implement an RC low-pass filter.

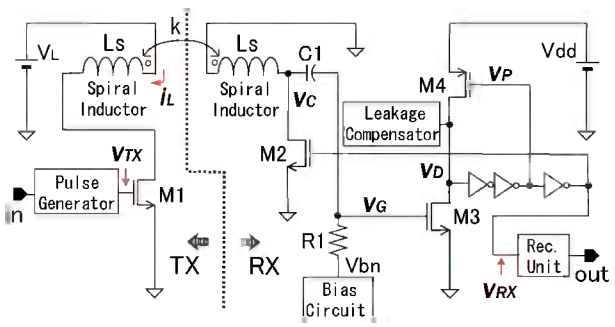

Fig.6 Transmitter and receiver.

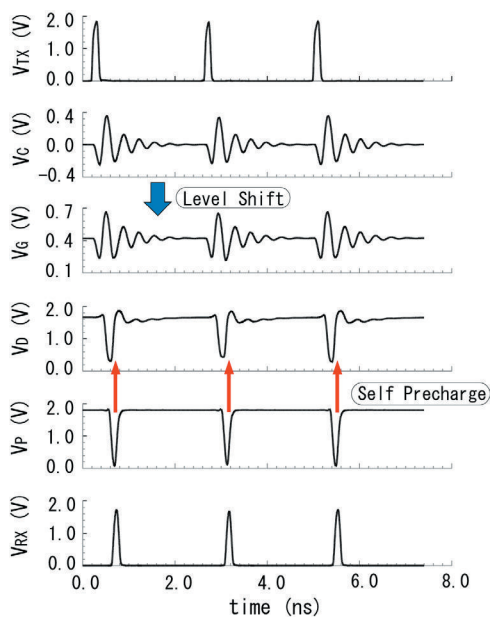

Fig.7 Operations of dynamic circuit and self pre-charging.

The communication scheme can transmit NRZ signal using "Pulse Generator" (PG) and "Rec. Unit" (RU). The schematics are depicted in Fig.9. Spice simulation results are shown in Fig.10. As shown in Fig.10, PG generates single pulse and double pulses when the input NRZ signal falls and rises, respectively. On the other hand, RU regenerates the input NRZ signal from the received single pulse and double pulses. Hence, an equivalent circuit of the proposed communication scheme including PG and RU, is just delay element. Furthermore, by only introducing M5 as shown in Fig.11, a transceiver can be simply implemented.

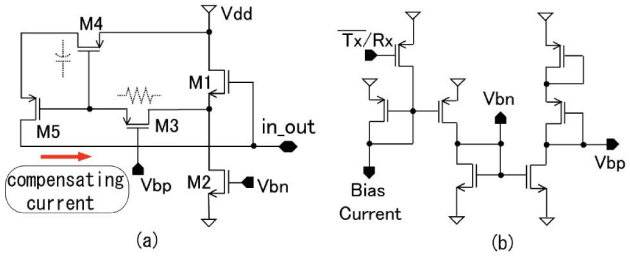

Fig.8 (a) Leakage compensator and (b) bias circuit.

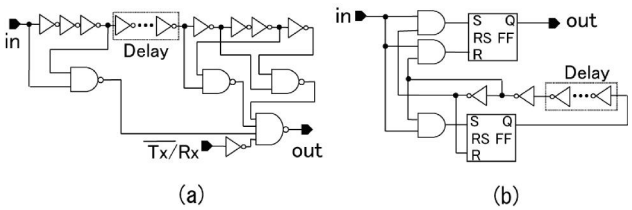

Fig.9 (a) Pulse Generator and (b) Rec. Unit.

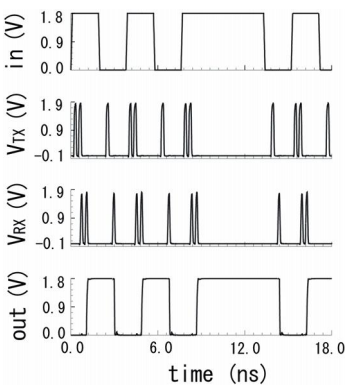

Fig.10 Pulse sequence coding.

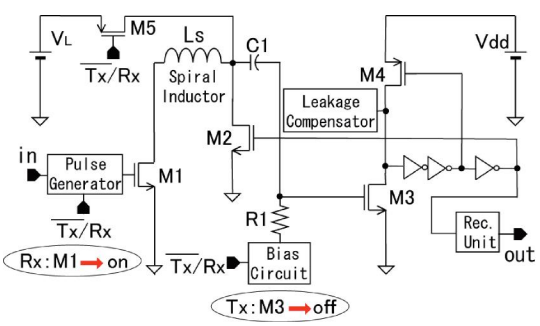

Fig.11 Transceiver.

Test Chip Fabrication and Measurement

In order to confirm the proposed concept, a test chip was designed and fabricated in 0.18μm 6 metal CMOS technology. Fig.12 shows a micrograph of the test chip and 12 transceivers were integrated. Two chips were set on manipulators in face to face and transfer characteristics were measured. Measured results are shown in Figs.13-15. Fig.13 shows transmitted data and received waveforms of the neighboring three channels, where pseudo random data were transmitted at 1.0Gbps. BER (Bit Error Ratio) < 10^{-10} was achieved without cross talk between the neighboring spiral inductors. The delay time was 2.7ns (=1.2ns[transceiver] + 1.0ns[I/O] + 0.5ns[PCB]). Measured power consumption is

shown in Fig.14. "Inductor (Tx)" and "Sensing (Rx)" are powers consumed by the spiral inductor in Tx and the dynamic circuits with pre-charging operation in Rx, respectively. The data activities were set to 0.5. The power consumptions were proportional to the data-rate and they were also reduced proportionally by the activity due to the asynchronous scheme. The power consumptions of PG and RU were relatively large. However, they are CMOS logic circuits and it is expected that the power consumptions are reduced in scaled devices. Fig.15 shows relationship between the distance and tolerance for position deviation. In this measurement, the receiving sensitivity was tuned by the bias current in Fig.8 (b), according to the distance. The criteria for passing were BER < 10^{-10} at 1.0Gbps. The symbol of triangle means that the criteria were not satisfied in this measurement but it was caused by cross talk through the power supply line. The performance is summarized and compared with those in literatures in Table II.

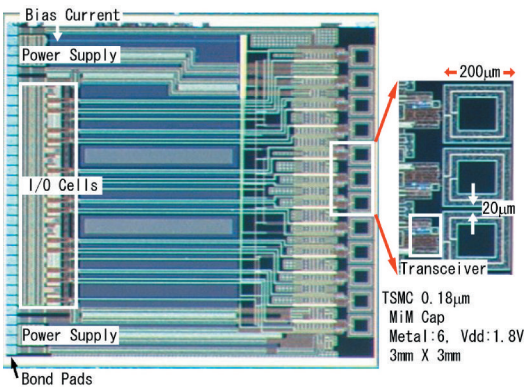

Fig.12 Photomicrograph of test chip.

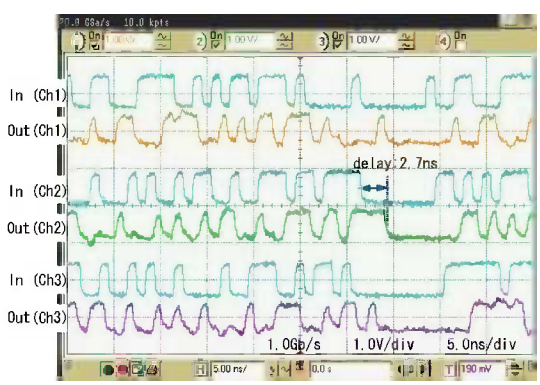

Fig.13 Transmitted data and received waveforms.

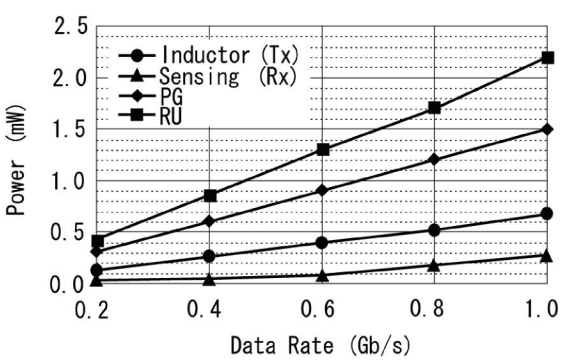

Fig.14 Measured power consumptions.

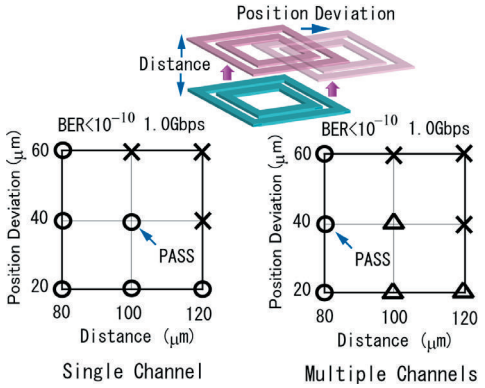

Fig.15 Relationships between distance and position deviation.

TABLE II PERFORMANCE COMPARISON

			This work	[3], [4]	Scaling Scenario in [4]
Technology			0.18μm	0.35μm	90nm
Communication distance			100μm	240μm	30μm
Inductor Diameter			200μm	300μm	300μm
Data Rate			1.0Gbps	1.25Gbps	1.25Gbps
Power	Tx	Inductor	0.67mW	43mW	1mW
		PG	1.5mW		
	Rx	Sensing	0.28mW	3mW	0.1mW
		RU	2.2mW		

Conclusions

A reduction method of power consumption and an asynchronous communication scheme without any clocking has been proposed for the spiral-inductor based wireless chip-interconnect. The methodology was verified and evaluated by measuring a test chip in 0.18μm 6 metal CMOS technology. The performance of 0.95mW/1.0Gbps/ch was achieved without any clocking. A 3D stacked system using the proposed wireless chip-interconnect and introducing an error-correct technique into the narrow pulse sequence are future study.

Acknowledgments

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References

[1] M. Koyanagi et al., "Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology," *ISSCC Digest of Technical Papers*, pp.270-271, Feb. 2001.

[2] K. Kanda et al., "1.27Gb/s/ch 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Digest of Technical Papers*, pp.186-187, Feb. 2003.

[3] D. Mizoguchi et al. "A 1.2Gb/s/pin Wireless Superconnect Base on Inductive Inter-Chip Signaling (IIS)", *ISSCC Digest of Technical Papers*, pp142-143, 2004.

[4] N. Miura et al. "Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-Chip Wireless Superconnect", *Dig. of Symp. on VLSI Circuits*, pp.246-249, June, 2004.

[5] A. Iwata et al., "A 3 Dimensional Integration Scheme Utilizing Wireless Interconnections for implementing Hyper Brains," to be published in *ISSCC 2005*.