Paper: Rb17-4-2351; 2005/6/3

A 2.7 Gcps and 7-Multiplexing CDMA Serial Communication Chip for Real-Time Robot Control with Multiprocessors

Mitsuru Shiozaki, Toru Mukai, Masahiro Ono, Mamoru Sasaki, and Atsushi Iwata

Hiroshima University
1-3-1 Kagamiyama, Higashihiroshima-shi, Hiroshima 739-8530, Japan
E-mail: shiozaki@dsl.hiroshima-u.ac.jp
[Received November 30, 2004; accepted February 19, 2005]

Intelligent robot control using multiprocessors, sensors, and actuators requires real-time flexible networks for communicating various types of real-time data, e.g., sensing data and interrupt signals. Furthermore, serial data transfer is required for implementing the network using a few wiring lines. To meet these requirements, we propose a CDMA serial communication interface utilizing novel two-step synchronization. The transmitter and receiver chip fabricated with 0.25μm digital CMOS technology achieved 2.7Gcps (chips per second) and 7-multiplex communication. The experimental interface board was developed for demonstrating flexible transfer of multiimage data by installing CDMA chips in addition to an FPGA.

Keywords: CDMA, serial communication, real-time, synchronization technique

1. Introduction

For advanced robot control using multiprocessors, sensors, and actuators, real-time communication between subsystems is crucial to satisfy each restriction on sampling time of sensing and control. Real-time communication is classified into hard and soft real-time [1]. Hard real-time communication refers to an absolute response to an event and pertains to command data transmitted to actuators, the task of calculation, etc. Data is small and latency time demanding. Soft real-time communication refers to slightly less restriction than hard real-time and pertains to image data from sensors, etc. This property becomes unreliable over time. Data is huge and requires throughput instead of latency time. Robot control requires flexible communication with two types of real-time data.

In addition, the networks must be implemented with a small number of wiring lines, since too many restrict smooth, high-speed movement of robot arms and hands.

Time-division multiple access (TDMA) cannot communicate varying amounts of real-time data within a restricted time frame well because data is transmitted in fixed packets or frames [1, 2]. Communication channels and individual bandwidth are difficult to change dynamically because control overhead is high and network flexibility sacrifices transmission efficiency.

We propose a communication scheme suitable for robot control whose key concept is code-division multiple access (CDMA) serial communication, which enables data multiplexing and transfer with several virtual paths on a single wire. Several types of data are independently transmitted through virtual paths.

In research thus far, CDMA has been implemented with wired communication [3, 4] and a bus configuration [3]. The bus configuration, however, adversely affects multiplex reflection and results in low data transfer of less than 100Mbps. CDMA has also been applied to point-to-point serial links and a communication chip developed [4]. Although high data transfer of 2.7Gcps was achieved, the number of multiplexing channels was limited to two. CDMA transmits multiplexed multivalued signals with several amplitude steps. The size of each step increases as the number of amplitude steps increases, necessitating synchronization that is robust against small-amplitude signals.

To achieve high-speed, highly multiplexed CDMA communication, we innovated two-step synchronization that includes code and chip synchronization to the point-to-point serial link [5, 6]. We designed and fabricated a test chip with a transmitter and receiver for CDMA serial communication with 0.25μm digital CMOS technology. The proposed CDMA achieved multi-Gcps P-to-P data transfer rate and 7-multiplexed communication.

2. Proposed Communication

2.1. Network for Robots

Figure 1 shows robot control connected by a point-to-point serial link configuration. Each processing block consists of processor units, such as DSPs and CPUs, and a high-speed CDMA serial communication chip; it has image sensors, and robot arms or hands. The execution frequency of servocontrol must be 10kHz for stable movement. Data transfer of 2Gbps is required overall for the network to transmit image data from image sensors (soft real-time), calculation results of manipulator dynamics (hard real-time), etc. So, the communication chip uses high-speed point-to-point link communication and operates as a bus by sending or receiving data through the chip.

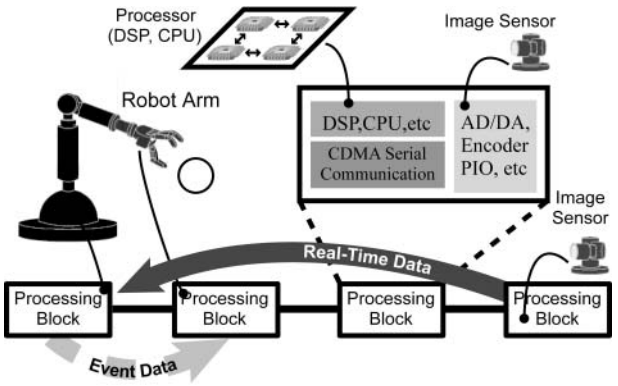

Fig. 1. A robot system implemented using CDMA serial communication.

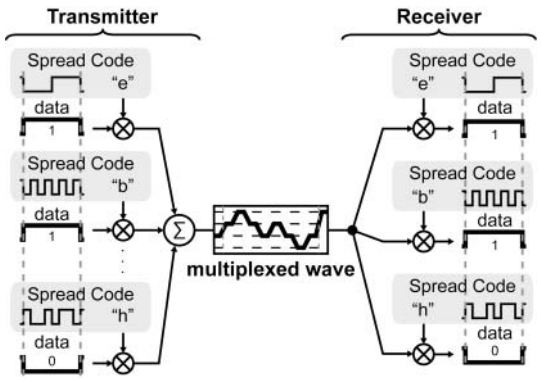

Fig. 2. Conceptual block diagram of the CDMA system.

2.2. CDMA

CDMA communication is diagrammed in **Fig.2**. On the transmitter side, data is encoded by a spread code set and each encoded signal multiplexed by summation and transmitted through a transmission line. On the receiver side, transmitted data is reconstructed by decoding the received signal. Decoding is processed by correlation between the received signal and a code identical to that used for encoding in the transmitter.

Spread codes create virtual channels, and each code can be used independently. Various real-time data, such as hard real-time data or soft real-time data, is communicated to satisfy constraints of restricted time on single wiring. Since data transfer is changed by the assignment of spread codes, data paths are reconfigured without disrupting real-time communication, resulting in real-time reconfigurable communication using a small number of wiring lines.

It is difficult to achieve high-speed communication using CDMA in part due to the difficulty in synchronization when using multiplexed multivalued signals with several amplitude steps. If the number of amplitude steps increases, the step size decreases and synchronization simply detecting rising edges of received signals becomes ineffective, making synchronization used for time multiplexed serial links inapplicable to the CDMA serial link.

Table 1. The Walsh code of length 8.

Name	Code
"a"	$+1+1+1+1+1+1+1+1$
"b"	$-1+1-1+1-1+1-1+1$
"c"	$-1-1+1+1-1-1+1+1$
"d"	$-1+1+1-1-1+1+1-1$
"e"	$-1-1-1-1+1+1+1+1$
"f"	$-1+1-1+1+1-1+1-1$
"g"	$-1-1+1+1+1+1-1-1$
"h"	$-1+1+1-1+1-1-1+1$

In the next section, we explain a two-step synchronization technique for high-speed highly multiplexed CDMA communication.

3. Synchronization Method

CDMA requires two types of correlation properties – a cross-correlation property and an auto-correlation property. The cross-correlation property shows interference (orthogonality) among spread codes and affects the bit error rate (BER). The auto-correlation property shows similarity based on the phase shift of a code and is convenient for synchronization.

It is difficult to choose optimum codes having these two properties in wired CDMA communication because these codes are short compared to that for radio communication and the type of code used is restricted, so we developed synchronization using Walsh codes with low auto-correlation. **Table 1** shows Walsh code as spread codes with a length of 8.

Consider the code composition in **Fig.3(a)** making synchronization convenient in the auto-correlation of Walsh codes. In "i" of the composite code obtained by multiplying codes "c" and "e," the positive maximum is obtained only if the shift becomes zero and the shape around the maximum is extremely sharp, which is convenient for synchronization. Code synchronization adjusts start timing for decoding and is done by determining the position at which the correlation becomes maximum.

Pulse timing should be adjusted and locked after code synchronization by using a delay locked loop (DLL) – a process termed chip synchronization. Consider auto-correlation functions "j" and "k" (**Fig.3(b)**) obtained by shifting auto-correlation function "i" to the left and right. As shown in **Fig.3(b)**, subtracting "k" from "j" becomes zero at the position where the shift is zero. The value of subtraction moves from positive to negative around zero, so by using the result of subtraction as the detected function for locking by DLL, the pulse timing is adjusted, attaining lock and chip synchronization.

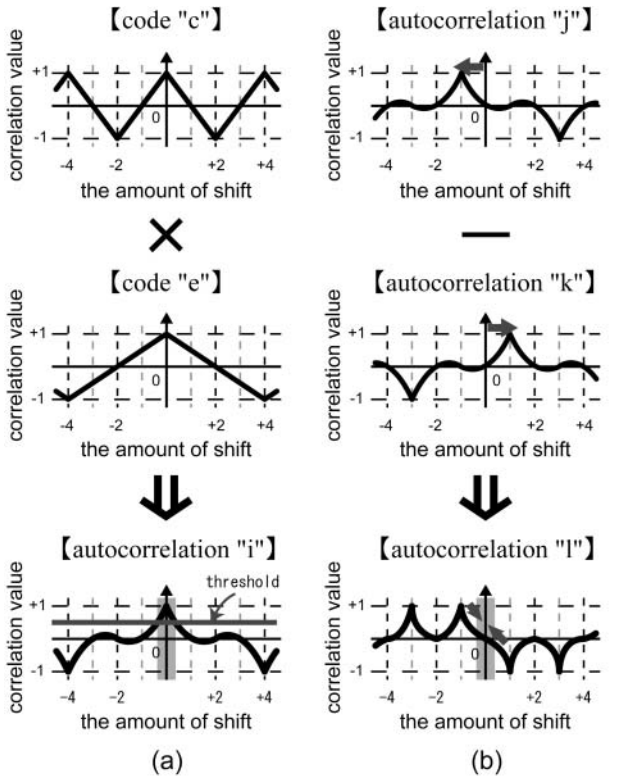

Fig. 3. Correlation function used for synchronization. (a) The auto-correlation function "i" is used for code synchronization. (b) The auto-correlation function "l" is used for chip synchronization.

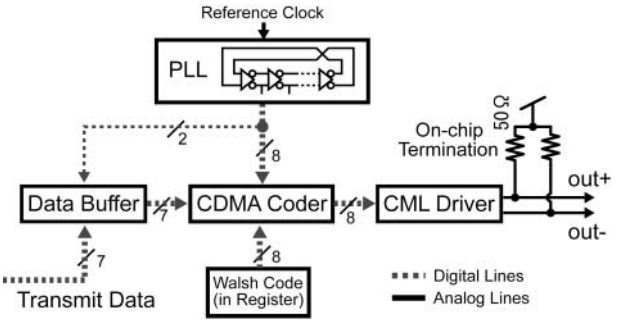

Fig. 4. A block diagram of the transmitter.

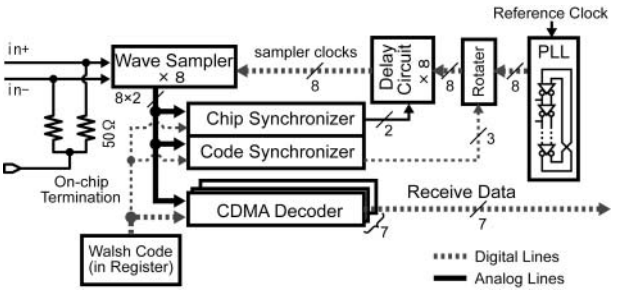

Fig. 5. A block diagram of the receiver.

4. Circuit Implementation

4.1. Transmitter

Figure 4 diagrams the transmitter. Input data is encoded in the CDMA coder by logical EXORing between bit data and spread codes. The current mode logic (CML) driver outputs the multiplexed wave. In the transmitter, the key technique of achieving a higher speed is using the CDMA coder. In particular, the output buffer is operated using the multi-phase clocks from a ring oscillator.

4.2. Receiver

Figure 5 diagrams the receiver circuit. The received differential signal is deinterleaved by wave samplers that consist of 3 stages of two sample and hold (S/H) circuits and source-follower buffers, and it synchronizes all phases of the input signals. The number of wave samplers equals the length of spread codes. Multiple clocks given by the ring oscillator control deinterleaved timing, although the rotator and voltage-controlled delay circuits exist between wave samplers and the ring oscillator. The rotator and voltage-controlled delay circuits are required for synchronization as explained below.

(A) CDMA Decoder

The decoder consists of 2×2 crossbar switches, a multiinput adder based on differential pairs, and a comparator. The number of crossbar switches and inputs of the adder equal the code length. Correlation is done on the multiinput adder by switching the crossbar based on codes "1" and "0." The comparator detects whether the result of correlation is positive or negative and outputs 1-bit data based on the decoder result. We explain circuit realization of synchronization below.

(B) Code synchronizer

The Gilbert cell (A) multiplies two outputs of correlators for Walsh code "c" and "e" (**Fig.6**). The result corresponds to the auto-correlation function "i" (**Fig.3(a)**) and a comparator compares it to a threshold. The comparison result is sent to the control unit, which is a logic circuit. If the auto-correlation function "i" does not exceed the threshold, the control unit shifts the order of clocks from the ring oscillator using the rotator. The frequency of the ring oscillator is locked by PLL. If the auto-correlation function "i" exceeds the threshold, the control unit concludes that code synchronization is completed and the synchronization phase moves to chip synchronization.

(C) Chip synchronizer

Two Gilbert cells (B) and (C) and four correlators generate auto-correlation functions "j" and "k" (**Figs.3(b)** and **6**). Since the outputs of the two Gilbert cells are differential current signals, a subtractor is implemented using simple wiring. These blocks function as a 2-delta delay discriminator. Outputs are filtered by loop filters and fed to voltage-controlled delay circuits as differential control signals Cnt+ and Cnt-. The loop consisting of wave samplers, chip synchronizer, and delay circuits operates as

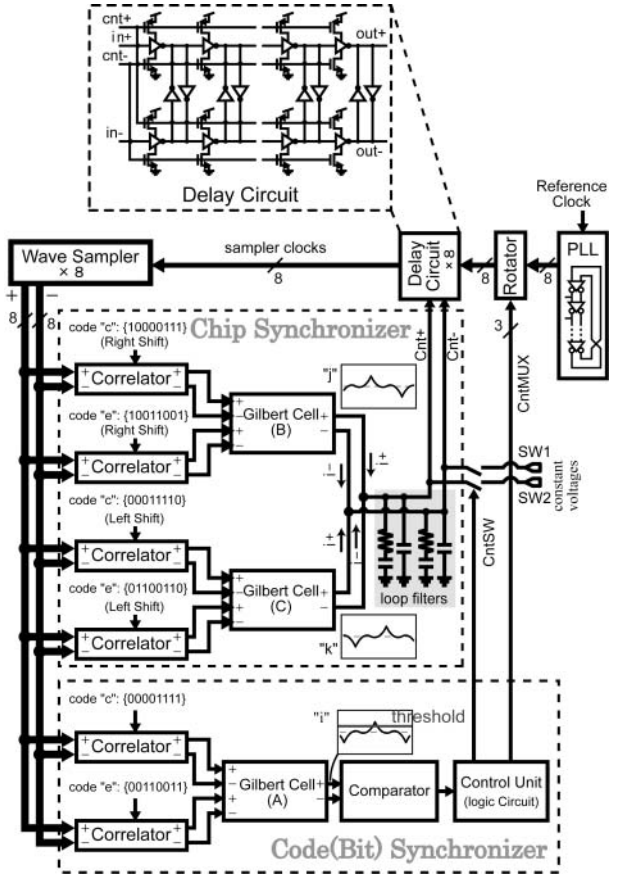

Fig. 6. A block diagram of the synchronization circuits code synchronization and chip synchronization.

a DLL. In the phase of code synchronization, Cnt+ and Cnt- are fixed at constant voltages by two switches (SW1, SW2). SW1 and SW2 are controlled by signal CntSW.

5. Design of Test Chip and Interface Board

The test chip was designed using a 0.25μm digital CMOS technology. The supply voltage is 2.5V and the reference clock frequency is 338MHz. Ring oscillators consist of eight stages. The transmitter and receiver operate at 2.7GHz. All capacitors are implemented by MOS capacitors and resistors are implemented by MOS transistors operating in the triode region, so resistance terminating at 50Ω is tuned by the gate voltage.

In the transmitter, the output amplitude of the differential signal for one code is set to 100mVp-p and the multiplexed wave has an 800mVp-p swing because the number of multiplexed codes is 8. The CDMA coder operates at 2.7GHz. Other circuits operate at 338MHz, which is the system clock frequency. In the receiver, decoders operate at 338MHz because the 2.7GHz signal is deinterleaved into 8 wave samplers. Circuit blocks operate easily by lowering the frequency.

The 4.0mm $\times$ 4.0mm die photo of the transmitter and receiver chip is shown in **Fig.7**. The chip is packaged in a 160 pin QFP plastic package. The size of the transmitter and receiver are 650μm $\times$ 1300μm and 3100μm $\times$ 980μm, respectively.

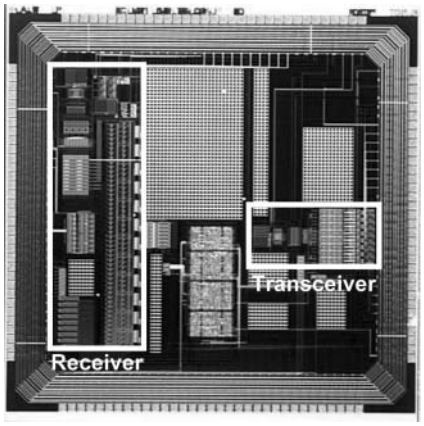

Fig. 7. Chip micrograph.

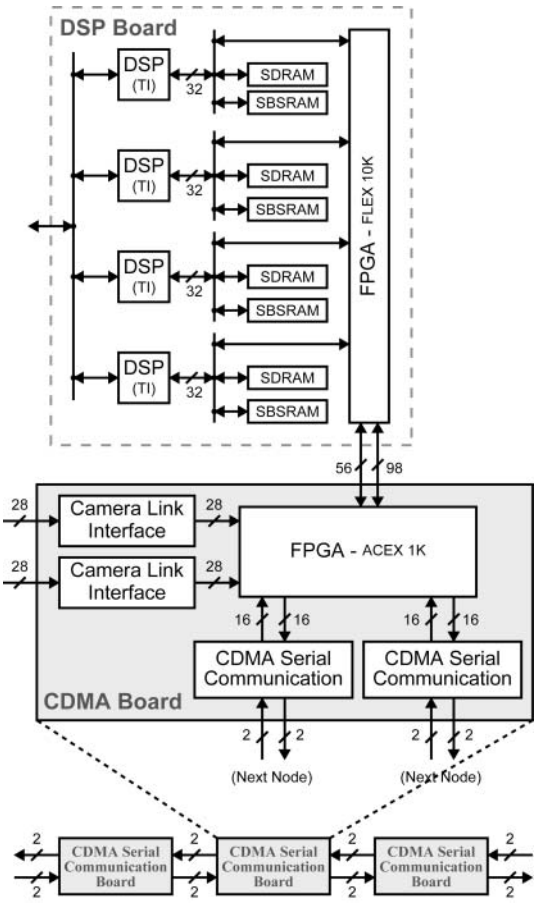

Fig. 8. Block diagram of the communication interface board.

We also designed the communication interface board using CDMA serial communication chips and multiple high-speed camera links. The block diagram and photograph are shown in **Figs.8** and **9**, respectively. The board has two CDMA serial communication chips and two the camera link interfaces, together with a connection port to

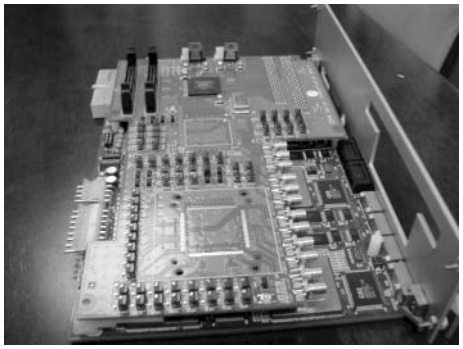

Fig. 9. Photograph of the communication interface board.

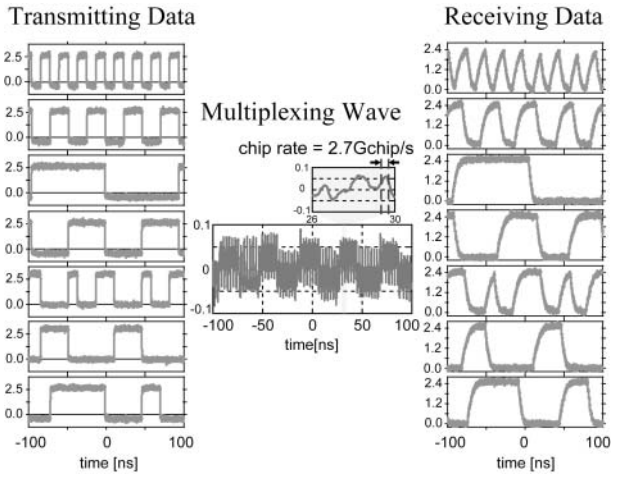

Fig. 10. Measurement results of the receiver.

a DSP board. With two CDMA communication ports, network topologies other than the daisy chain are configurable paths on the board and the control of CDMA serial communication chips is programmed by rewriting a field programmable gate-array (FPGA), which is used as an image processing circuit. The FPGA is operated from the DSP as memory, and CDMA serial communication chips are controlled using a DSP program. Data transfer of the memory interface between the DSP and FPGA is extremely slow compared to other interfaces.

6. Measurement

Figure 10 shows measurement results at a chip rate of 2.7Gcps. Waveforms at left represent input data. Those in the center represent the multiplexed CDMA signal. The measured amplitude of the multiplex wave is 0.1Vp-p – lower than the design value because the wire between the CML driver and MUX is 0.2mm long in the chip layout. Since its time constant is large and the voltage amplitude of driving signals is small, the MUX cannot completely switch the CML driver.

As shown at right, the receiver decoded the 7-multiplexed wave with spread codes and accurately output bit sequences identical to transmitted data. The 7-multiplexed input wave was generated by an arbitrary waveform generator AWG710. Its amplitude for one code is 100mVp-p and it is used as a design value. The transmitter and receiver consume 148mW and 264mW at a 2.5V supply voltage, respectively.

7. Conclusions

We developed a CDMA serial communication interface using original synchronization and a transceiver chip with 2.7Gcps and 7-multiplexing. Key techniques are two-step synchronization for multilevel signal receiving and circuit implementation. The transceiver chip was developed using 0.25μm digital CMOS technology; it achieved a 2.7Gcps and synchronization of 7-multiplex communication. We also developed a CDMA communication interface board with chips, FPGA, and camera link interfaces to demonstrate CDMA performance.

Acknowledgements

This research was supported by grants from Core Research for Evolutional Science and Technology (CREST), Japan Science Technology Corporation (JST). We thank Nassda Corporation for full-chip circuit verification and post-layout analysis provided in the University Program and conducted by HSIM.

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Name:
Mitsuru Shiozaki

Affiliation:
Graduate School of Advanced Sciences of Matter, Hiroshima University

Address:
1-3-1 Kagamiyama, HigashiHiroshima-shi, Hiroshima 739-8530, Japan

Brief Biographical History:
1998 B. E. degree from Ritsumeikan University
2000 M. E. degree from Ritsumeikan University
2000- Doctoral candidate, Hiroshima University

Main Works:
• "A 2.7 Gcps and 7-multiplexing CDMA Serial Communication Chip using Two-Step Synchronization Technique," IEICE Trans. Electronics, In press, 2005.

Membership in Learned Societies:
• The Institute of Electronics, Information and Communication Engineers (IEICE)
• The Robotics Society of Japan (RSJ)

Name:
Toru Mukai

Affiliation:
Graduate School of Advanced Sciences of Matter, Hiroshima University

Address:
1-3-1 Kagamiyama, HigashiHiroshima-shi, Hiroshima 739-8530, Japan

Brief Biographical History:
2003 B. S. degree from Hiroshima University
2005 M. E. degree from Hiroshima University
2005- Doctoral candidate, Hiroshima University

Name:
Masahiro Ono

Affiliation:
Graduate School of Advanced Sciences of Matter, Hiroshima University

Address:
1-3-1 Kagamiyama, HigashiHiroshima-shi, Hiroshima 739-8530, Japan

Brief Biographical History:
2001 B. S. degree from Hiroshima University
2003 M. E. degree from Hiroshima University
2003- Doctoral candidate, Hiroshima University

Membership in Learned Societies:
• The Institute of Electronics, Information and Communication Engineers (IEICE)
• The Robotics Society of Japan (RSJ)

Name:
Mamoru Sasaki

Affiliation:
Graduate School of Advanced Sciences of Matter, Hiroshima University

Address:
1-3-1 Kagamiyama, HigashiHiroshima-shi, Hiroshima 739-8530, Japan

Brief Biographical History:
1988 M. E. degree from Kumamoto University
1991 D. E. degree from Kumamoto University
1991- Research Associate, Kumamoto University
1994- Associate Professor, Kumamoto University
2002- Associate Professor, Hiroshima University

Main Works:
• M. Sasaki, and R. Haraguchi, "An Adiabatic Charging Pass-Transistor Logic Circuit with Bootstrap Switching," IEICE Trans. Electronics, Vol.J84-C, No.6, pp. 516-523, 2001.

Membership in Learned Societies:
• The Institute of Electronics, Information and Communication Engineers (IEICE)

Name:
Atsushi Iwata

Affiliation:
Graduate School of Advanced Sciences of Matter, Hiroshima University

Address:
1-3-1 Kagamiyama, HigashiHiroshima-shi, Hiroshima 739-8530, Japan

Brief Biographical History:
1970- Researcher/Manager, NTT Laboratories
1994 Ph.D. degree in electronics engineering from Nagoya University
1994- Professor, Hiroshima University
2001- Director of Research Center for Nano-devices and Systems at Hiroshima University

Main Works:
• A. Iwata, T. Morie, and M. Nagata, "Merged Analog-Digital Circuits Using Pulse Modulation for Intelligent SoC Applications," IEICE Trans. Fundamentals, Vol.E84-A, No.2, pp. 486-496, 2001.

Membership in Learned Societies:
• Institute of Electrical and Electronics Engineers (IEEE)
• Japanese Neural Network Society (JNNS)
• The Institute of Electronics, Information and Communication Engineers (IEICE)