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HiSIM2: Advanced MOSFET Model Valid for RF Circuit Simulation

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Invited Paper

***Abstract*—The compact MOSFET model development trend leads to models based on the channel surface potential, allowing higher accuracy and a reduced number of model parameters. Among these, the Hiroshima University Semiconductor Technology Academic Research Center IGFET Model (HiSIM) solves the surface potentials with an efficient physically correct iteration procedure, thus avoiding additional approximations without any computer run-time penalty. It is further demonstrated that excellent model accuracy for higher-order phenomena, which is a prerequisite for accurate RF circuit simulation, is achieved by HiSIM without any new model parameters in addition to those for describing the current–voltage characteristics.**

***Index Terms*—Compact MOSFET model, device physics, iterative solution, RF features, surface potentials.**

I. Introduction

MOSFET technology is leading semiconductor industries through aggressive size reduction on a short time scale. To achieve further downscaling, improvement of the device structure has been undertaken such as that in multigate MOSFETs [1], [2]. Application of advanced MOSFETs to circuits is an additional urgent task to meet the required high circuit performances. For this purpose, compact models of MOSFET devices are indispensable, and Berkeley short-channel IGFET model (BSIM) compact models, based on the threshold-voltage modeling approach, have served the semiconductor industry as standard models [3].

It is often believed by model users that compact models are not directly based on device physics, and many compact-model developers further believe that precise device physics is much too complicated to be applied to circuit models. However, as microscopic device phenomena are becoming dominant for device features [4], compact models cannot ignore the physics behind the phenomena any more. Otherwise, the model cannot predict device features accurately, and the enormous increase of the number of model parameters cannot be stopped. It has been shown that surface potential-based modeling is the first step to get a breakthrough toward an improved situation [5]. Hiroshima University Semiconductor Technology Academic Research Center (STARC) IGFET Model (HiSIM) is a complete MOSFET model for advanced technologies based on the surface potential concept [6]–[8], who's development history dates back to the beginning of the 1990s when the dc [9] and ac [5] model core, including short-channel effects, were initially reported.

Channel engineering is drawing advanced technologies to the aggressive scaling of MOSFETs. HiSIM considers the resulting impurity concentration distribution explicitly, which enables accurate prediction of technology scaling [10]. Measurements of higher-order device features, important for analog as well as RF circuits, are shown to provide insight of the microscopic carrier dynamics, which is very useful for developing accurate models [11].

II. Modeling of MOSFET Characteristics

To describe the MOSFET features, the following three basic equations have to be solved simultaneously [12]:

1) Poisson equation

$$\nabla^2\phi = -\frac{q}{\epsilon_{\mathrm{Si}}}(N_D - N_A + p - n)$$
$$n = n_i \exp\left[\frac{q(\phi - \phi_{fn})}{kT}\right]$$
$$p = n_i \exp\left[\frac{q(\phi_{fp} - \phi)}{kT}\right] \quad (1)$$

2) Current-density equations

$$j_n = -q\mu_n n\frac{\partial\phi}{\partial y} + qD_n\nabla n$$
$$j_p = -q\mu_p p\frac{\partial\phi}{\partial y} - qD_p\nabla p \quad (2)$$

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3) Continuity equations

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla j_n$$
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla j_p \tag{3}$$

where y is the direction along the channel, and ϕ, q, $\epsilon_{\rm Si}$, k, and T are the potential, the electron charge, the silicon permittivity, the Boltzmann constant, and the lattice temperature in kelvin, respectively. N_D, N_A, p, n, and n_i are the donor, acceptor, hole, electron, and intrinsic carrier concentration, respectively. The carrier mobility and the carrier diffusion constant are denoted by μ and D. However, different from bipolar transistors usually operating under high-carrier-injection conditions, electrostatic effects mostly determine the device features in MOSFETs. Due to this fact, couplings among equations are not strong and can be solved independently.

Circuit simulators solve the continuity equation in the form [13]

$$I_x(t) = I_{x0}(t) + \frac{dQ_x(t)}{dt}$$
$$x = S\ (\text{source}), D\ (\text{drain}), G\ (\text{gate}),\ \text{and}\ B\ (\text{bulk}) \tag{4}$$

which is obtained by integrating (3) along the channel under the assumption that the potential responds spontaneously to the voltage change. I_{x0} is the current at the steady-state condition. The circuit simulator solves (4) for an ensemble of transistors in a circuit at the same time [14].

The surface potential-based models solve the two remaining equations of the basic set of device equations. Here, the Poisson equation describes the relation between potential and carrier concentrations, and the current equation under the drift-diffusion approximation describes the mechanism of current flow [15].

A. Surface Potential Calculation

The surface potential ϕ_S is calculated by solving the Poisson equation with the Gauss law as

$$C_{\rm ox}\left(V_G' - \phi_S(y)\right) = \sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}}\Bigg[\exp\{-\beta(\phi_{\rm S}(y)-V_{\rm bs})\}+\beta(\phi_{\rm S}(y)-V_{\rm bs})-1 + \frac{n_{p0}}{p_{p0}}\left\{\exp\left(\beta\left(\phi_{\rm S}(y)-\phi_f(y)\right)\right) - \exp\left(\beta\left(V_{\rm bs}-\phi_f(y)\right)\right)\right\}\Bigg]^{\frac{1}{2}} \tag{5}$$

$$C_{\rm ox} = \frac{\epsilon_{\rm ox}}{T_{\rm ox}} \tag{6}$$
$$V_G' = V_{\rm gs} - V_{\rm FB} \tag{7}$$
$$\beta = \frac{q}{kT} \tag{8}$$
$$\phi_f(L_{\rm eff}) - \phi_f(0) = V_{\rm ds} \tag{9}$$
$$n_{p0} = \frac{n_i^2}{p_{p0}} \tag{10}$$

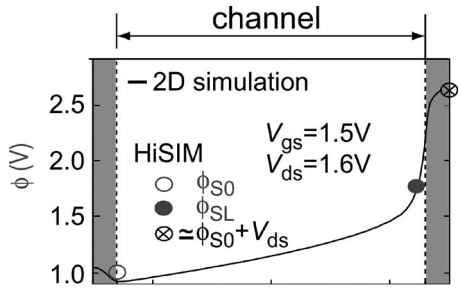

Fig. 1. Calculated surface potential by HiSIM at source side ϕ_{S0} and at drain $\phi_{\rm SL}$ under the saturation condition. Simulated surface potential distribution along the channel with a 2-D simulator is also depicted for comparison. (Color version available online at http://ieeexplore.ieee.org.)

where $V_{\rm FB}$ is the flat band voltage, $T_{\rm ox}$ is the physical gate-oxide thickness, and $L_{\rm eff}$ is the channel length

$$L_{\rm eff} = L_{\rm gate} - 2{\rm XLD}. \tag{11}$$

In (11), $L_{\rm gate}$ is the gate length, and XLD is the diffusion length underneath the gate oxide. The hole concentration at equilibrium condition p_{p0} is approximated to be the substrate impurity concentration $N_{\rm sub}$. The quasi-Fermi potential $\phi_f(y)$ together with $V_{\rm G}'$ determines the carrier concentration in the channel. The intrinsic carrier concentration n_i is

$$n_i = n_{i0} T^{\frac{3}{2}} \exp\left(-\frac{E_g}{2q}\beta\right) \tag{12}$$

$$n_{i0} = \frac{1}{4}\left(\frac{2k}{\pi\hbar^2}\right)^{\frac{3}{2}} \tag{13}$$

where E_g describes the temperature dependent bandgap [16]

$$E_g = E_{g0} - {\rm BGTM1}\cdot T - {\rm BGTM2}\cdot T^2 \tag{14}$$

where E_{g0} is a constant, and BGTM1 and BGTM2 are model parameters. To obtain a simplified equation for the potential distribution along the channel induced by applied voltages, we introduce two approximations. One is the charge-sheet approximation assuming zero thickness of the inversion charge, and the other is the gradual channel approximation assuming a smooth potential increase along the channel [17]. These approximations allow to derive an analytical formulation for all device performances as a function of surface potentials at the source side $\phi_{\rm S0}$ and the drain side $\phi_{\rm SL}$. The calculated surface potentials are compared with the two-dimensional (2-D) device simulation results in Fig. 1 [7], [8]. $\phi_{\rm SL}$ gives the value at the end of the gradual channel approximation. The remaining potential increase of $V_{\rm ds}-\phi_{\rm SL}$ in amount occurs both in the pinch-off region and the overlap region as indicated in Fig. 1.

HiSIM solves the Poisson equation iteratively in the same way as numerical device simulators. Other advanced surface potential models such as PSP (by Pennsylvania State University and Philips) approximate the surface potential by explicit

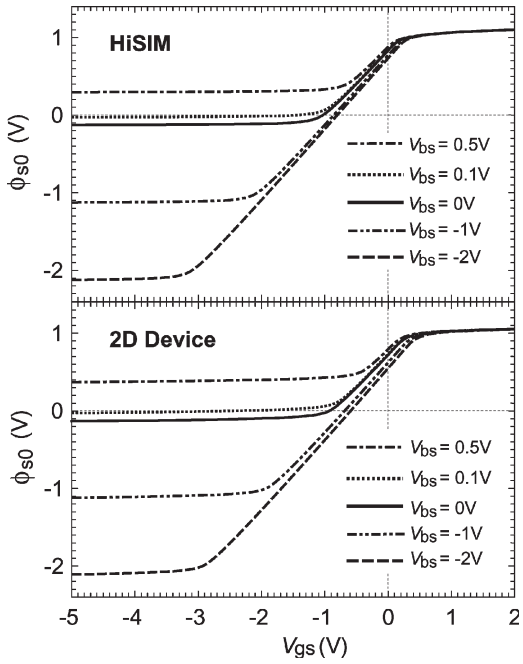

Fig. 2. Comparison of calculated surface potentials at source side ϕ_{S0} by HiSIM and a 2-D-device simulator for various substrate voltages V_{bs} at drain voltage of $V_{ds} = 0.1$ V. Gate length is fixed to 2 μm.

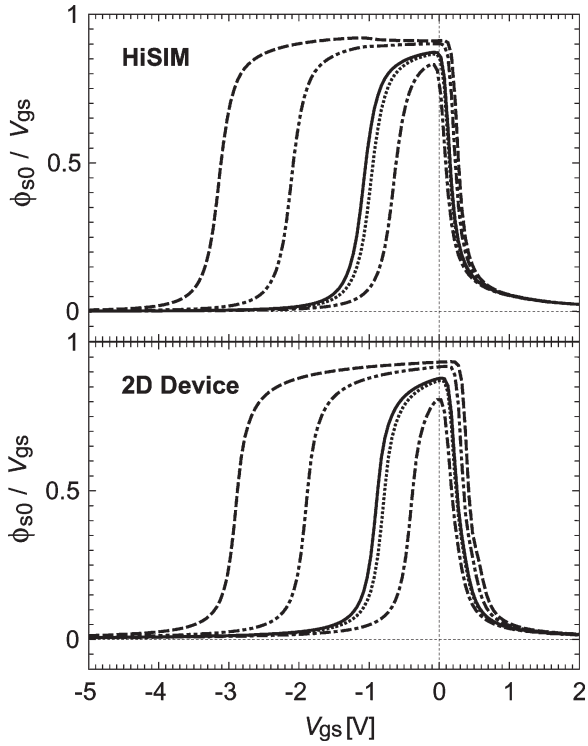

Fig. 3. Comparison of calculated derivatives of the surface potential at source side ϕ_{S0} by HiSIM and a 2-D-device simulator. Bias conditions are the same as given in Fig. 2.

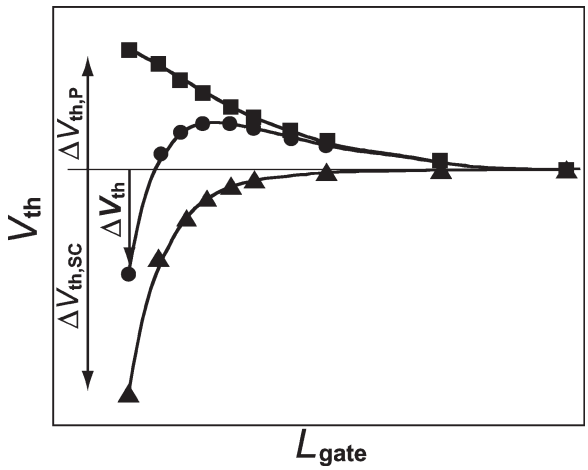

Fig. 4. Schematic plot of the separation of V_{th} into the contributions of the short-channel and the reverse-short-channel effect.

mathematical functions with the applied voltages as variables [18]. The reason for approximating with closed-form equations is to reduce the simulation time by eliminating otherwise unavoidable iterations. However, in practical applications, the simulation time of the iterative HiSIM approach turns out to be shorter than for an analytical approach [5], [19].

The derivatives of all device characteristics strongly influence analog as well as RF circuit performances. The features of those derivatives are mainly determined by the surface potential derivatives with respect to all possible applied voltages. Surface potential values of HiSIM are compared with the 2-D device simulation results in Fig. 2. The slight quantitative differences are explained by the fact that the impurity profile, used for 2-D device simulations, is not calibrated to the studied devices. Calculated surface potential derivatives from HiSIM are compared with the 2-D numerical device simulation results in Fig. 3. All the complicated features of these derivatives, which are not observable in usual surface potential versus voltage plots, are seen to be accurately preserved in the HiSIM results. The reason for this preservation of the physical essence is that HiSIM solves the Poisson equation iteratively without introducing any assumptions, similar to the 2-D numerical simulator.

B. Short-Channel Effects

Different from the drift approximation, the drift diffusion approximation does not require the threshold voltage V_{th} to be a model parameter for describing device characteristics. MOSFET device parameters T_{ox} and N_{sub} determine the complete MOSFET behavior including the subthreshold characteristics automatically and consistently. However, advanced technologies accompanied by the aggressive scaling down of device sizes cause various phenomena such as short-channel effects, which result in a shift ΔV_{th} of V_{th} for short-channel transistors in comparison to the threshold voltage of a long-channel transistor. The modeled ΔV_{th} can be viewed as consisting of two main effects [9], [20], [21], namely: 1) short-channel effect $\Delta V_{th,SC}$ and 2) reverse short-channel effect $\Delta V_{th,P}$.

The separation into these two components ($\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,R}$ (or $\Delta V_{th,P}$)) is schematically shown in Fig. 4.

1) Short-Channel Effect $\Delta V_{th,SC}$: All the observed short-channel effects are caused by the lateral electric field contribution in the MOSFET channel. Thus, $\Delta V_{th,SC}$ can be written as

a function of the lateral electric field E_y by applying the Gauss law as explained in [20], i.e.,

$$-\int_A^B E_{y1}(x)dx+\int_C^D E_{y2}(x)dx+\int_D^A E_x(x)dy=-\frac{Q_{\rm S}}{\epsilon_{\rm Si}} \tag{15}$$

$$\left(E_x+W_d\frac{dE_y}{dy}\right)\epsilon_{\rm Si}=(V_G'-\phi_{\rm S})\frac{\epsilon_{\rm Si}}{T_{\rm ox}} \tag{16}$$

which derives the relationship

$$\Delta V_{\rm th,SC}=\frac{\epsilon_{\rm Si}}{C_{\rm ox}}W_d\frac{dE_y}{dy} \tag{17}$$

where W_d is the depletion layer thickness written as

$$W_d=\sqrt{\frac{2\epsilon_{\rm Si}(2\Phi_{\rm B}-V_{\rm bs})}{qN_{\rm sub}}}. \tag{18}$$

A parabolic potential distribution along the channel is approximated, which results in a position-independent gradient of the lateral electric field dE_y/dy and is derived with model parameters of the form

$$\frac{dE_y}{dy}=\frac{2(V_{\rm BI}-2\Phi_{\rm B})}{(L_{\rm gate}-{\rm PARL2})^2} \tag{19}$$

$$\left({\rm SC1}+{\rm SC2}\cdot V_{\rm ds}+{\rm SC3}\cdot\frac{2\Phi_{\rm B}-V_{\rm bs}}{L_{\rm gate}}\right) \tag{20}$$

where

$$2\Phi_{\rm B}=\frac{2}{\beta}\ln\left(\frac{N_{\rm sub}}{n_i}\right) \tag{21}$$

is the surface potential giving the threshold condition. $V_{\rm BI}$ and PARL2 represent the built-in potential and the depletion width of the junction parallel to the channel, respectively. The model parameter SC1 determines the threshold voltage shift for small $V_{\rm ds}$ and $V_{\rm bs}$ and is expected to be unity. If the measured $V_{\rm th}$ is plotted as a function of $V_{\rm ds}$, it shows a nearly linear dependence. The gradient is proportional to SC2. SC3 implements a correction of the charge sheet approximation, which is expected to be small and can be viewed as a modification of $V_{\rm th}$ due to $V_{\rm bs}$ for inhomogeneous substrate impurity profiles.

2) Reverse Short-Channel Effect $\Delta V_{\rm th,P}$: The pocket implant technology causes inhomogeneity of the impurity concentration along the channel. Two obvious features are 1) $V_{\rm th}$ increase starts already from the relatively long $L_{\rm gate}$ and 2) short-channel effects such as the $V_{\rm ds}$ dependence on $V_{\rm th}$ appear even for long-channel transistors [22]. This is modeled by developing a new definition for the threshold voltage based on the idea that threshold condition is determined by the inversion carrier densities both in the nonpocket region and in the pocket region [23]. Two model parameters (LP: length of the pocket extension into the channel; $N_{\rm SUBP}$: peak of the pocket impurity concentration) are introduced as shown in Fig. 5. The impurity concentration in the substrate is distinguished with

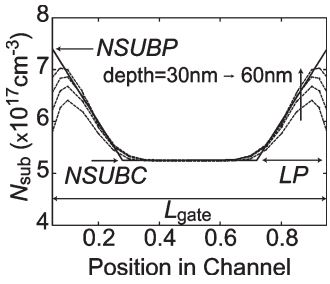

Fig. 5. Dashed curves are simulated impurity profiles by the 2-D-process simulator TSUPREM at various depths. The extracted pocket profile with the model is depicted by a solid line.

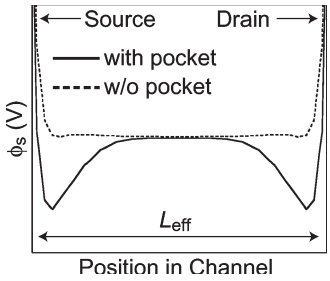

Fig. 6. Surface potential distribution along the channel simulated with a 2-D simulator.

$N_{\rm SUBC}$ from $N_{\rm SUBP}$. The resulting model equations for the $V_{\rm th}$ shift due to the pocket implant are [24]

$$\Delta V_{\rm th,P}=(V_{{\rm th},R}-V_{\rm th0})\frac{\epsilon_{\rm Si}}{C_{\rm ox}}W_d\frac{dE_{y,\rm P}}{dy} \tag{22}$$

$$V_{{\rm th},R}=V_{\rm FB}+2\Phi_{\rm B}+\frac{Q_{\rm B}}{C_{\rm ox}}+\ln\left(\frac{N_{\rm subb}}{N_{\rm SUBC}}\right) \tag{23}$$

$$V_{\rm th0}=V_{\rm FB}+2\Phi_{\rm BC}+\frac{\sqrt{2qN_{\rm SUBC}\epsilon_{\rm Si}(2\Phi_{\rm BC}-V_{\rm bs})}}{C_{\rm ox}} \tag{24}$$

$$\frac{dE_{y,\rm P}}{dy}=\frac{2(V_{\rm BI}-2\Phi_{\rm B})}{{\rm LP}^2}\times\left({\rm SCP1}+{\rm SCP2}\cdot V_{\rm ds}+{\rm SCP3}\frac{2\Phi_{\rm B}-V_{\rm bs}}{\rm LP}\right) \tag{25}$$

$$N_{\rm subb}=2N_{\rm SUBP}-\frac{(N_{\rm SUBP}-N_{\rm SUBC})L_{\rm gate}}{\rm LP}-N_{\rm SUBC} \tag{26}$$

where $Q_{\rm B}$ is the depletion charge. The parameters SCP1, SCP2, and SCP3 describe the short-channel effect caused by the potential minimum at higher impurity concentration of the pocket as shown in Fig. 6. $2\Phi_{\rm BC}$ is the potential giving threshold condition with $N_{\rm SUBC}$, and $2\Phi_{\rm B}$ is the equivalent potential giving threshold condition with $N_{\rm sub}$, i.e.,

$$2\Phi_{\rm BC}=\frac{2}{\beta}\ln\left(\frac{N_{\rm SUBC}}{n_i}\right) \tag{27}$$

$$N_{\rm sub}=\frac{N_{\rm SUBC}(L_{\rm gate}-{\rm LP})+N_{\rm SUBP}\cdot{\rm LP}}{L_{\rm gate}} \tag{28}$$

As defined in (28), $N_{\rm sub}$ is replaced with the averaged impurity concentration in the channel. $N_{\rm SUBP}$ describes the substantial

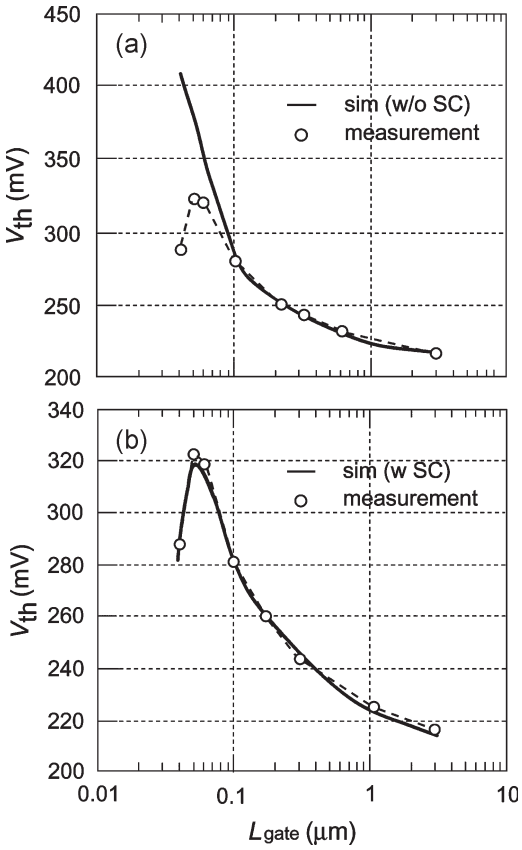

Fig. 7. Comparison of measurements and pocket-implant model for $V_{\rm th}$ as a function of $L_{\rm gate}$. Results (a) with and (b) without SC are shown.

increase of substrate concentration by overlapping pockets at the source and drain. $V_{\rm th,R}$ and $V_{\rm th0}$ are the threshold voltages for the cases with and without pocket implant, respectively. The starting of overlapping causes a steep increase of $V_{\rm th}$ as a function of decreasing $L_{\rm gate}$. This effect enables to extract LP from measurements. Fig. 7 compares the $V_{\rm th}$–$L_{\rm gate}$ characteristics of the developed pocket implant model with and without inclusion of the short-channel effects (SC). The steep increase at $L_{\rm gate} = 0.1$ μm in Fig. 7(a) means the starting of the pocket overlap, where LP $= 0.05$ μm.

In some cases, the pocket profile cannot be described by a single linearly decreasing form, but exhibits extensive tails as schematically shown in Fig. 8. Further, model parameters describing the extension of the pocket are included in HiSIM2 [10]. Thus, an important advantage of the HiSIM modeling approach is that detailed information about the fabrication technology of studied devices can be known, which is important for characterizing device variations precisely.

The short-channel and reverse short-channel effects are incorporated as the threshold voltage shift together with poly-depletion and narrow width effects

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R} + \Delta V_{\rm th,P} + \Delta V_{\rm th,W} - \phi_{\rm Spg}. \tag{29}$$

The Poisson equation is solved with $V'_{\rm G}$ including

$$V'_{\rm G} = V_{\rm gs} - V_{\rm FB} + \Delta V_{\rm th}. \tag{30}$$

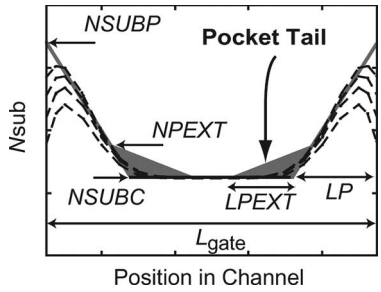

Fig. 8. Modeled pocket tail with NPEXT and LPEXT.

The obtained results are practically a parallel shift of the current–voltage (I–V) characteristics, because the effects are modeled with the potential value giving threshold condition $2\Phi_{\rm B}$. However, the subthreshold swing increase is also one of the important short-channel effects in advanced technologies. Extension to the correct inclusion of subthreshold swing is done in HiSIM by taking into account the $V_{\rm gs}$-dependent $2\Phi_{\rm B}$ instead of fixing it to the value giving threshold condition.

C. Mobility Model

Low field mobility is described with three independent mechanisms of coulomb, phonon, and surface roughness scattering [25], i.e.,

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \tag{31}$$

$$\mu_{\rm CB}({\rm coulomb}) = {\rm MUE}_{\rm CB0} + {\rm MUE}_{\rm CB1}\frac{Q_{\rm I}}{q \times 10^{11}} \tag{32}$$

$$\mu_{\rm PH}({\rm phonon}) = \frac{{\rm MUE}_{\rm PH1}}{(T/T_{\rm NOM})^{{\rm MUE}_{\rm TMP}} \times E_{\rm eff}^{{\rm MUE}_{\rm PH0}}} \tag{33}$$

$$\mu_{\rm SR}({\rm surface\ roughness}) = \frac{{\rm MUE}_{\rm SR1}}{E_{\rm eff}^{{\rm MUE}_{\rm SR0}}} \tag{34}$$

where ${\rm MUE}_{\rm CB0}$, ${\rm MUE}_{\rm CB1}$, ${\rm MUE}_{\rm PH1}$, ${\rm MUE}_{\rm TMP}$, ${\rm MUE}_{\rm SR1}$, and ${\rm MUE}_{\rm SR0}$ are model parameters. Here, $E_{\rm eff}$ is the effective field normal to the surface

$$E_{\rm eff} = \frac{1}{\epsilon_{\rm Si}}(\gamma \cdot Q_{\rm B} + \eta \cdot Q_{\rm I}) \tag{35}$$

where γ and η are model parameters, and $Q_{\rm B}$ and $Q_{\rm I}$ are the depletion charge and the inversion charge, respectively, as calculated with the surface potentials.

Mobility universality preserves conditions [26]–[28]

$${\rm MUE}_{\rm PH0} \simeq 0.3 \tag{36}$$

$${\rm MUE}_{\rm SR0} = 2.0 \tag{37}$$

$$\gamma = 1.0 \tag{38}$$

$$\eta = 0.5 \tag{39}$$

independent of the technologies applied, as illustrated in Fig. 9 [29]. However, these parameters can be used for fitting purposes [10], if necessary. In recent advanced technologies, the above values deviate from the universality condition of (31)–(34).

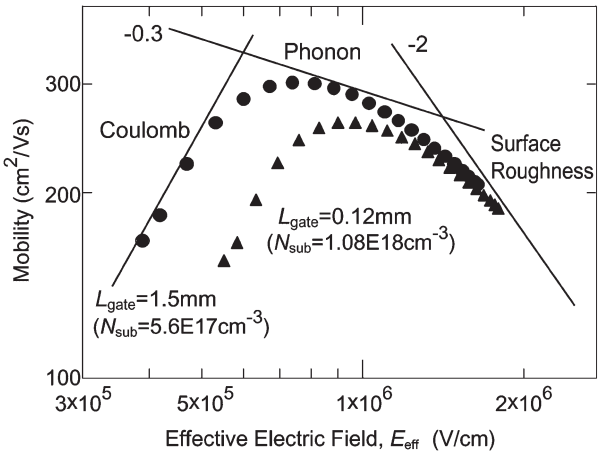

Fig. 9. Calculated mobility as a function of effective field for different MOSFET devices [29].

This can be understood as any inaccuracy of assumptions introduced to derive the closed form for mobility description. However, the deviation of extracted values from universality cannot be too large. Carrier distribution in two dimensions is enhanced in short-channel transistors and causes a modification of the carrier mobility. Our observation is that surface roughness scattering is reduced for short-channel transistors because of the carrier flow moving away from the surface. Due to the carrier flow at increasing distance from the surface with reducing $L_{\rm gate}$, the electric field experienced by the carriers is different from the field in the long $L_{\rm gate}$ case. This results in a modification of $\mathrm{MUE_{SR1}}$ as well as $\mathrm{MUE_{PH1}}$. Such channel-length-dependent secondary effects require additional model parameters.

High field mobility is modeled as [30]

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\rm y}}{V_{\rm max}}\right)^{\rm BB}\right)^{\frac{1}{\rm BB}}} \tag{40}$$

where the maximum velocity $V_{\rm max}$ is temperature dependent. BB is usually fixed to 2 for electrons and 1 for holes. E_y is calculated as a function of ϕ_S. The maximum velocity $V_{\rm max}$ should be the maximum electron saturation velocity in the inversion layer ($\simeq 6.5 \times 10^7$ cm/s [31]), which is, however, exceeded at reduced $L_{\rm gate}$. This phenomenon, called velocity overshoot, is included in the mobility model as

$$V_{\rm max} = V_{\rm MAX} \cdot \left(1 + \frac{\rm VOVER}{L_{\rm gate}^{\rm VOVERP}}\right) \tag{41}$$

where VOVER and VOVERP are model parameters.

Comparison of calculated I–V characteristics with measurements is shown in Fig. 10 for an advanced 40-nm CMOS technology. The model parameters are the same for all gate lengths.

III. Symmetry Aspects and Scalability

The $V_{\rm ds}$ sweep from positive to negative values changes the direction of drain–current flow. However, the derivatives must be the same, namely symmetry across $V_{\rm ds} = 0$ has to be preserved without discontinuity. Surface potential-based modeling, which includes both drift and diffusion contributions, in principle, preserves the symmetry automatically. However, the fundamental nature of the symmetry is destroyed by artifacts introduced in the modeling of phenomena observed in advanced MOSFET technologies such as short-channel effects. Instead of modeling a diminishing magnitude of the short-channel effect as $V_{\rm ds}$ approaches zero, efficient numerical smoothing is done to improve such unavoidable disturbances [10].

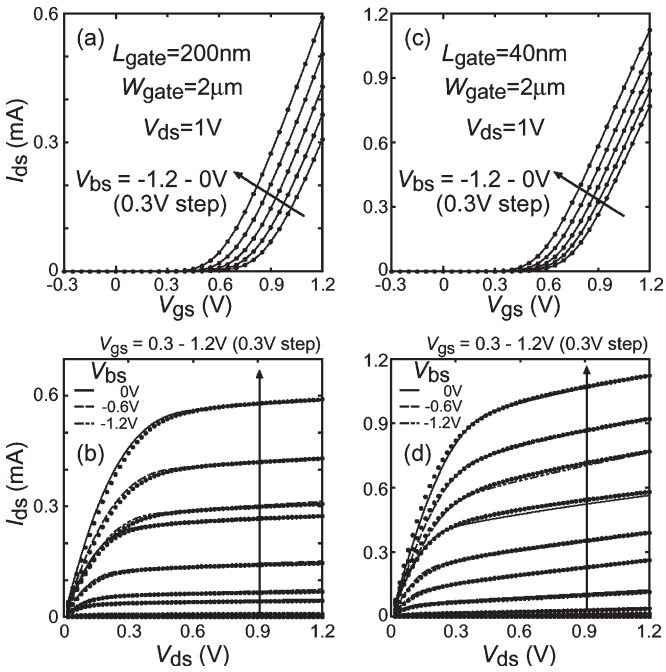

Fig. 10. Comparison of calculated I–V characteristics of a 40 nm CMOS technology with measurements for $L_{\rm gate} = 200$ nm (a) $I_{\rm ds}$ versus $V_{\rm gs}$ (b) $I_{\rm ds}$ versus $V_{\rm ds}$ and for $L_{\rm gate} = 40$ nm (c) $I_{\rm ds}$ versus $V_{\rm gs}$ (d) $I_{\rm ds}$ versus $V_{\rm ds}$.

Run-time statistics show that in spite of iteration procedures, the surface potential-based model provides good simulation time efficiency [5], [32] and is proved to provide stable circuit simulations for large-scale circuits with one million devices [32]. This will make the extension of SPICE simulation even to very large circuits possible. An important advantage of the evolutional modeling approach based on the surface potential description over the conventional $V_{\rm th}$-based description is that the surface potential concept is extendable to any advanced MOSFET technology. HiSIM-SOI has been successfully developed based on the same concept but solving three surfaces simultaneously. Calculating the three surface potentials requires about two times more simulation time than for the bulk case in the present development stage [33].

IV. Features Supporting RF Applications

Application of MOSFETs to analog as well as RF circuits is very tough due to the many undesired characteristics of MOSFETs [34]. Under high-frequency operation, higher-order phenomena of MOSFETs become obvious. Typical phenomena include harmonic distortion, noise, and carrier response delay. There are two main reasons why the surface potential-based

model is superior to the conventional threshold-voltage-based models, especially for analog and RF applications. The first reason is that accurate derivatives of surface potentials are preserved automatically. The other reason is that complete surface potential and carrier concentration information along the channel is known in HiSIM as can be seen in Fig. 1. The importance of this information for modeling the influential phenomena in RF circuits is demonstrated in the following.

A. Harmonic Distortion

Harmonic distortion originated from the nonlinearity of the device response to applied voltages, which induces additional outputs, which are integral multiples of the input frequency. If the model is consistent, and all model parameters are accurately extracted from measurements, other measured quantities should be reproduced without any additional model parameters. Harmonic distortion is one subject for verification of this statement. Fig. 11 verifies that the low frequency harmonic distortion is indeed correctly reproduced without additional parameters or adjustments [35]. The symbols are measurements, and solid lines are the calculated result with a parameter set extracted only from normal measured I–V characteristics. Dashed lines show the result with tuned mobility parameter values by 3%, which has an unobservable influence on the I–V characteristics. Singularities observed in the harmonic distortions can be attributed to those of the mobility for low $V_{\rm ds}$ values. At high frequencies, the harmonic distortion characteristics are governed by carrier dynamics rather than by mobility alone [36].

B. Noise

Advanced MOSFETs are suffering from two dominating noise contributions, namely: 1) $1/f$ noise and 2) thermal noise. Additionally, frequency-dependent-induced gate noise and cross-correlated noise are observed in high-frequency operation [37]. The $1/f$ noise is caused by the carrier fluctuation resulting from trap/detrap processes at the oxide/substrate interface [38] as well as the mobility fluctuation due to traps. Thus, modeling of the noise requires integrating the carrier distribution along the channel and leads to a formula that depends on the carrier concentration at source and drain. The final description for $1/f$ noise intensity is [39]

$$S_{\rm Id:1/f} = \frac{I_{\rm ds}^2 \rm NFTRP}{\beta f (L_{\rm eff} - \Delta L) W_{\rm eff}} N_{\rm fluct} \tag{42}$$

$$N_{\rm fluct} = \frac{1}{(N_0 + N^*)(N_{\rm L} + N^*)} + \frac{2\mu E_y \rm NFALP}{N_{\rm L} - N_0} \ln\left(\frac{N_{\rm L} + N^*}{N_0 + N^*}\right) + (\mu E_y \rm NFALP)^2 \tag{43}$$

where the parameters NFALP and NFTRP represent the contribution of mobility fluctuation and the ratio of trap density to attenuation coefficient, respectively. N_0 and $N_{\rm L}$ are carrier densities at source side and drain side or pinch-off point, respectively, as calculated in HiSIM. N^* is written as

$$N^* = \frac{C_{\rm ox} + C_{\rm dep} + \rm CIT}{q\beta} \tag{44}$$

where $C_{\rm dep}$ is the depletion capacitance calculated with ϕ_S, and CIT is the capacitance caused by the interface-trapped carriers and is normally fixed to zero. Simulation results are compared with measurements in Fig. 12. One model parameter, the trap density, is fitted to the measurements.

Modeling of thermal noise is based on the Nyquist theorem considering the noise source as resistance [40]. This theory is extended to the transistor by van der Ziel, where thermal noise is obtained from integration of the channel conductance along the channel [37]

$$S_{\rm Id:thermal} = \frac{4kT}{L_{\rm eff}} \int g_{\rm ds}(y) dy. \tag{45}$$

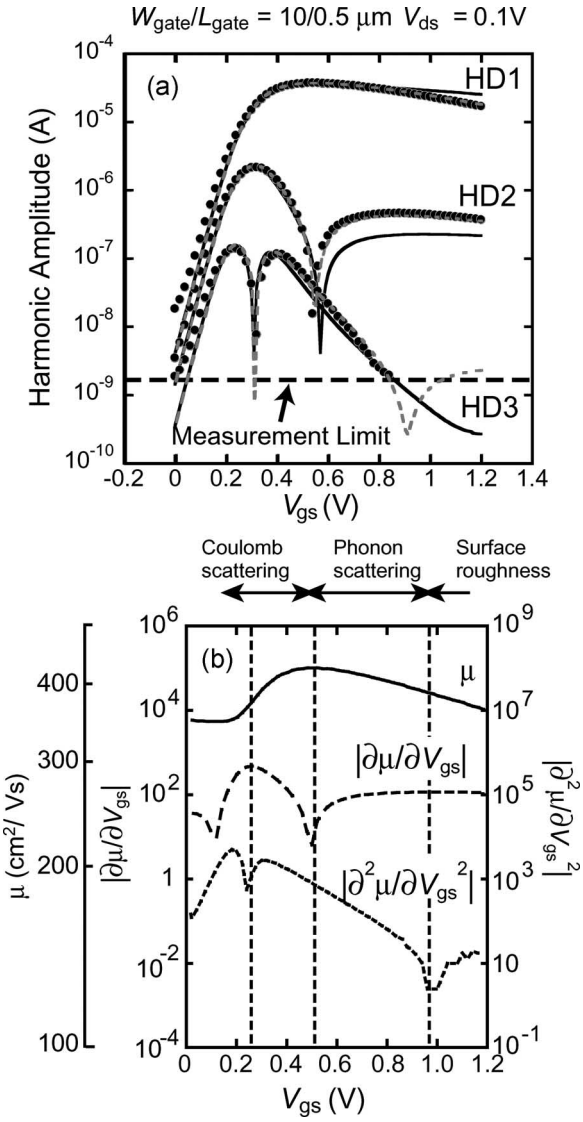

Fig. 11. (a) Simulated harmonic distortion characteristics at low drain bias and low frequency (1 kHz). (b) Mobility model of HiSIM and its derivatives. (Color version available online at http://ieeexplore.ieee.org.)

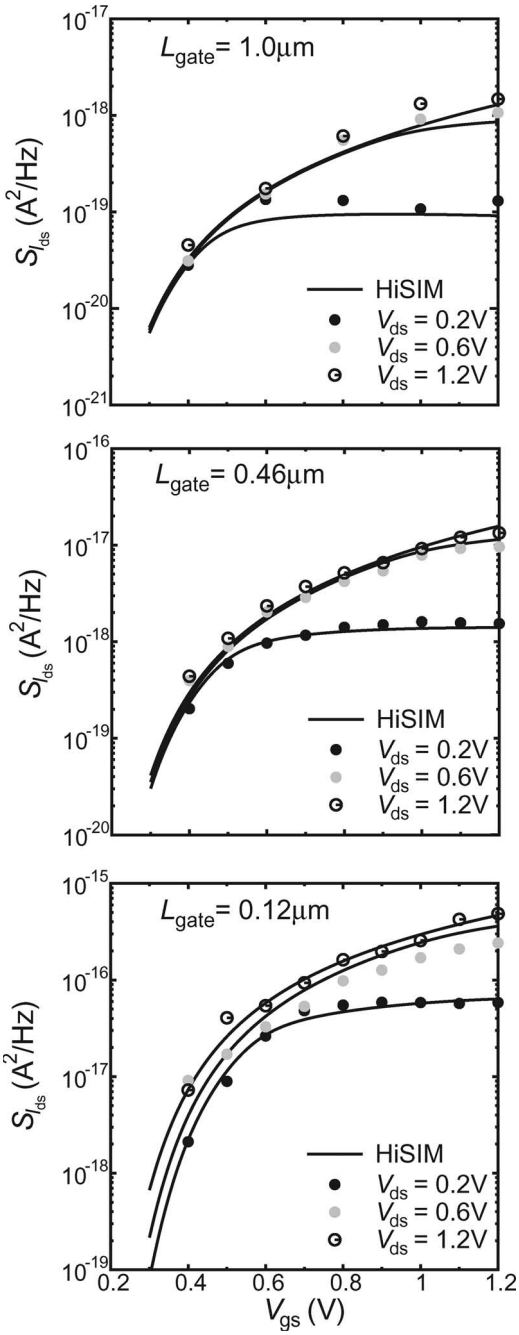

Fig. 12. Comparison of the bias dependence of measured and simulated drain current noise by HiSIM at a frequency of 100 HZ.

Here, $I_{\rm ds}$, $g_{\rm ds}(y)$, $g_{\rm ds0}$, and γ are the drain–current, position-dependent channel conductance, channel conductance at $V_{\rm ds}=0$, and drain noise coefficient, respectively. In HiSIM, integration is performed with the surface potential $\phi_{\rm S}$ instead of the channel position [41], [42]. The final equations for $S_{\rm Id:thermal}$ [shown in (46) at the bottom of the next page] in our compact modeling approach, obtained after solving the integral of (45), become functions of surface potentials as well as the surface potential derivatives at source and drain, where μ_s, μ_d, and $\mu_{\rm av}$ are mobilities at the source side, the drain side, and averaged along the channel, respectively, and η, χ, and $const0$ are expressed as that shown in (47)–(49) at the bottom of the next page.

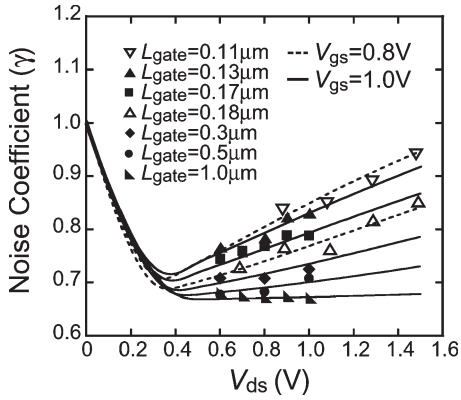

Fig. 13. Calculated noise coefficient γ with HiSIM as a function of drain voltage $V_{\rm ds}$ compared with measurements. Two different technologies are compared. For one technology measurements are represented by solid symbols and corresponding HiSIM results by solid lines, and for the other technology by open symbols and dashed lines.

VgV_t is equal to the carrier density at the source side divided by the oxide capacitance calculated with surface potentials. Thus, no additional model parameters are required for the thermal noise model.

Thermal noise is verified with the noise coefficient γ, which is defined as the noise value normalized with the channel conductance at $V_{\rm ds}=0$, i.e.,

$$\gamma = \frac{S_{\rm Id:thermal}}{4kTg_{\rm ds0}}. \tag{50}$$

Theoretically, it is predicted for long-channel transistors that γ reduces from 1 to 2/3 under the saturation condition. Fig. 13 shows predicted thermal noise coefficients with HiSIM in comparison to measurements [41], [42] for two different technologies. The increase of the noise coefficient under the saturation condition with reducing gate length is attributed to the potential increase along the channel. The potential increase along the channel causes enhanced carrier scattering, resulting in reduction of mobility along the channel. This is the main origin of the γ increase.

In addition to the two major noise contributions, induced gate noise and noise cross correlation are becoming important when operating MOSFETs in higher frequency regimes. This is also modeled in the same way as the other noises, namely by integrating gate conductance along the channel induced by capacitive coupling with the channel conductance [43].

Here, it is worthwhile to notice that the model parameters are required only for the $1/f$ noise to describe the trap density and the mobility fluctuation due to traps. These parameters are nearly universal if the technology is mature [39]. Thus, most of the higher-order phenomena can be predicted by the commonly measured I–V characteristics. This fact concludes that majority of the carrier dynamics, even in a microscopic aspect, is still governed by electrostatic effects, which are determined by the Poisson equation [11].

C. Nonquasi-Static (NQS) Effects

Under high-frequency operation, the current response is different from the predicted results with a conventional model as

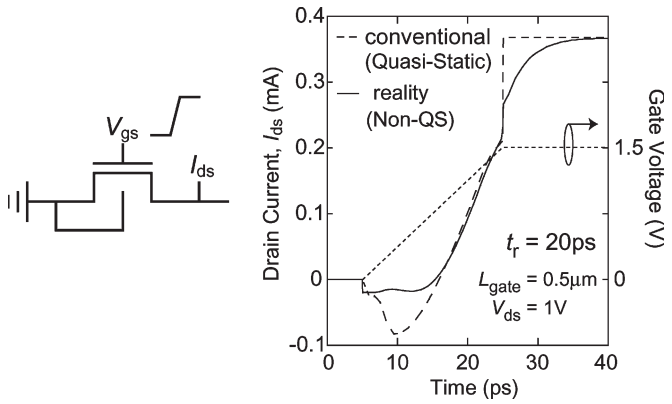

Fig. 14. Transient drain–current for 20-ps rising input. QS artifacts are eliminated with HiSIM's NQS model.

shown in Fig. 14. This is understood as a distributed effect along the channel and often modeled by dividing the channel into many small segments [44]. However, the phenomenological modeling approach by channel segmentation requires huge simulation time and an artificial device description.

The conventional model approximates that carriers respond instantaneously to the changes of applied voltages, called the quasi-static (QS) approximation. The unrealistic abrupt change of simulated current shown in Fig. 14 is an artifact of the modeling assuming instantaneous response of carrier dynamics to a voltage change [45]. The modeling, which takes account of the NQS effect, is done in HiSIM by including the carrier transit delay [35], [46], [47]. A simulation time increase of only about 3% in comparison with the QS approximation is achieved without sacrificing accuracy of the simulation result. For circuits where the NQS effect is obvious, even simulation time reduction has been observed [48]. The advantage of the HiSIM-NQS model is an easy to perform NQS simulation, just by selecting the model flag provided in HiSIM.

The most often used analysis for characterizing the high-frequency response of devices is with the admittance matrix, of which the elements are called Y-parameters [49]. For the investigation, a small signal with frequency ω and amplitude $V_{\rm p}$ is superimposed on the dc voltage

$$V(t) = V_{\rm dc} + V_{\rm p} \exp i\omega t. \tag{51}$$

Conventionally, a substrate network is introduced to reproduce the Y-parameter measurements. To derive a closed-form equation based on the origin of the high frequency response instead of using a network, the continuity equation can be solved together with the current density equation in an analytical way. The final description reduces to an expression of the Bessel functions [50], [51], which can be extended to the surface potential description including the drift and diffusion contributions [52], [53]. Comparisons of model calculation results and measurements are shown in Fig. 15. For the calculation, only the gate resistance is fitted to the measurements. Simulation results under the QS approximation are also depicted. The differences between NQS results and QS results are not as drastic as predicted previously [54]. To observe the NQS effect more clearly, the gate resistance contribution is eliminated from the simulation, and the result is shown in Fig. 16. The NQS effect becomes obvious at frequencies beyond 1/3 of the cutoff frequency.

A unified NQS model both for transient analysis and ac analysis is desired to extend the simulation capability. This enables high-frequency verification done for both the time domain and the frequency domain aspects at the same time without additional effort. For this purpose, Fourier transformation of the transient NQS model is the most straightforward approach. Therefore, we derived an analytical formulation for the frequency domain analysis based on Fourier transformation. The result is shown in Fig. 17 in comparison with the numerical Fourier transformation of the time-domain result. Good agreement of the two methods up to the frequencies of two times the cutoff frequency proves the validity of the method for real applications [55].

Thus, HiSIM includes the following options. One is to select the QS or NQS model, and the other is to select the time-domain or frequency-domain analysis. Here, it is emphasized again

$$S_{\rm Id:thermal} = 4kT\frac{W_{\rm eff}C_{\rm ox}VgVt\mu}{(L_{\rm eff}-\Delta L)}\frac{(1+3\eta+6\eta^2)\mu_d^2+(3+4\eta+3\eta^2)\mu_d\mu_s+(6+3\eta+\eta^2)\mu_s}{15(1+\eta)\mu_{\rm av}^2} \tag{46}$$

$$\eta = 1-\frac{(\phi_{\rm SL}-\phi_{\rm S0})+\chi(\phi_{\rm SL}-\phi_{\rm S0})}{V_gV_t} \tag{47}$$

$$\chi = 2\frac{cnst0}{C_{\rm ox}}\left(\left[\frac{2}{3}\frac{1}{\beta}\frac{\{\beta(\phi_{\rm SL}-V_{\rm bs})-1\}^{\frac{3}{2}}-\{\beta(\phi_{\rm S0}-V_{\rm bs})-1\}^{\frac{3}{2}}}{\phi_{\rm SL}-\phi_{\rm S0}}\right]-\sqrt{\beta(\phi_{\rm S0}-V_{\rm bs})-1}\right) \tag{48}$$

$$const0 = \sqrt{\frac{2\epsilon_{\rm Si}qN_{\rm sub}}{\beta}} \tag{49}$$

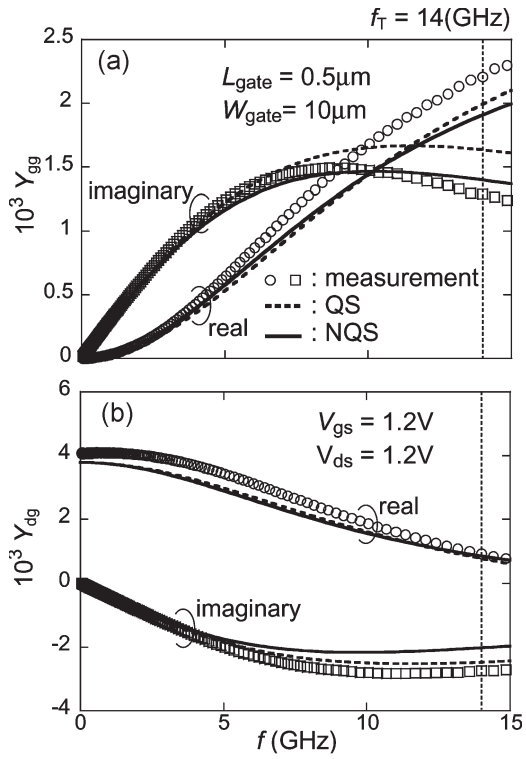

Fig. 15. Measured (open symbols) and calculated Y-parameters with the NQS model (solid lines) and the QS model (dashed lines). Model parameters are extracted by normal I–V measurements and no fitting parameters are introduced. As external contribution only the gate resistance was included.

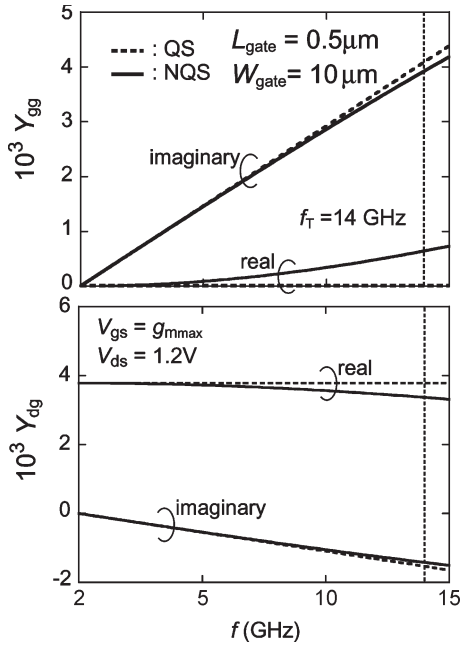

Fig. 16. Measured (open symbols) and calculated Y-parameters with the NQS model (solid lines) and the QS model (dashed lines) without the gate-resistance contribution.

that parameter extraction with only the I–V characteristics is sufficient for NQS simulation. It has to be noticed that HiSIM's NQS model allows to describe all MOSFET-related RF effects without any additional parameters, which was previously only possible by extracting the elements of a substrate-resistance network from Y-parameter measurements.

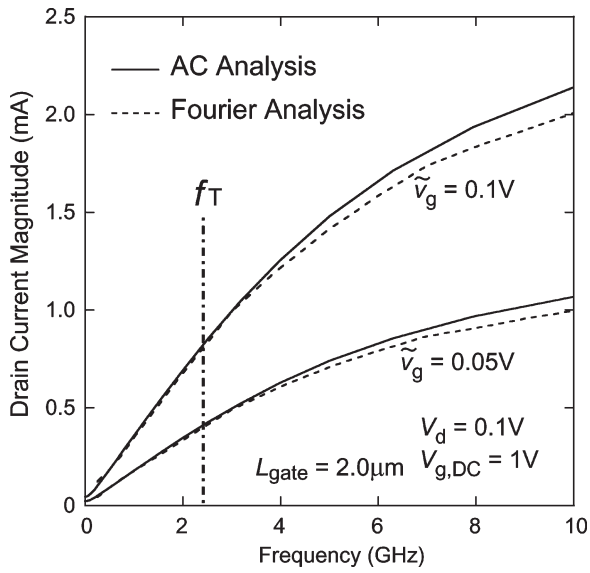

Fig. 17. Comparison of drain–current magnitude calculated with frequency-domain model and time-domain model.

V. Technology Variations

Important advantages of the size reduction of MOSFETs are the improvement of integration density as well as high-speed circuit operation. Logic circuits fully profit from this improvement by applying the smallest size transistors available. However, the reduction of device size enhances not only the noise as can be seen in Figs. 11 and 12 but also results in the loss of technology control causing increased variations of device performances. A model with less model parameters has bigger chances to extract the origins of these variations. Extraction of the technology variations has been performed with test circuits enabling separation of interchip and intrachip variations [56]–[58]. The test circuits are based on basic analog circuit elements consisting of either only n-MOSFETs or p-MOSFETs.

For previously studied CMOS technologies, the most critical parameter variations, which cause substantial variations of the device characteristics, were determined to come from $L_{\rm gate}$, $W_{\rm gate}$, and $N_{\rm SUBP}$. Additionally, it has been found that the intrachip variations amount to about 1/3 of the interchip variations [57].

VI. Modeled Phenomena

Table I summarizes all phenomena modeled in HiSIM2. Most of the phenomena are observed in any type of possible device geometries for advanced technologies.

VII. Parameter Extraction Procedure

HiSIM is a complete surface potential-based MOSFET model and does not include $V_{\rm th}$ as a model parameter. This means at the same time that basic device parameters such as $T_{\rm ox}$ and $N_{\rm sub}$ mostly determine the device features. These basic device parameters determine, in particular, the mobility

TABLE I
MODELED PHENOMENA IN HiSIM

Phenomena	Subjects
Short Channel	
Reverse-Short Channel	pile-up
	pocket
Poly-Depletion	
Quantum-Mechanical	
Channel-Length Modulation	
Narrow-Channel	
Non-Quasi-Static	Transient Time-Domain
	AC Frequency-Domain
Temperature Dependency	Thermal Voltage
	Bandgap
	Intrinsic-Carrier Concentration
	Phonon Scattering
	Maximum Velocity
Mobility Models	Universal Mobility
	High-Field Mobility
Shallow-Trench Isolation	Threshold Voltage
	Mobility
	Leakage Current
Capacitances	Intrinsic
	Overlap
	Lateral-Field Induced
	Fringing
Noise	1/f Noise
	Thermal Noise
	Induced Gate Noise
	Cross-Correlation Noise
Leakage Currents	Substrate Current
	Gate Current
	GIDL Current
Source/Drain Resistances	
Junction Diode	

and the short-channel effects through the surface potentials. Therefore, accurate extraction of these parameters is indispensable for the subsequent extraction of other model parameters. The extraction sequence is briefly summarized in Table II for I–V measurements. The second, third, and fourth columns describe the variable applied in the measurements, the range of the variable used for the extraction, and the parameters extracted, respectively. First, the basic device parameters are extracted with long-channel transistors. The measured $V_{\rm th}$ as a function of $L_{\rm gate}$ is used to extract short-channel parameters roughly. This step can be excluded if rough information about the short-channel parameters is already available. The measured $I_{\rm ds}$–$V_{\rm gs}$ in the subthreshold region is then efficiently applied to

TABLE II
BRIEF DOCUMENTATION FOR EXTRACTION PROCEDURE. SEE MAIN TEXT FOR MORE DETAILED EXPLANATION. (a) ROUGH EXTRACTION WITH $V_{\rm th}$. (b) FINE EXTRACTION WITH $I_{\rm ds} - V_{\rm gs}$ IN THE SUBTHRESHOLD REGION. (c) EXTRACTION WITH $I_{\rm ds} - V_{\rm gs}$ & $V_{\rm ds}$ IN THE LINEAR & SATURATION REGION. (d) EXTRACTION FOR TEMPERATURE DEPENDENCE

STEP	INPUT	EXTR. REGION	EXTRACTION
1	$L_{\rm gate}$	long	NSUBC, VFB
	$V_{\rm bs}$		
	$V_{\rm ds}$		
2	$L_{\rm gate}$	middle	NSUBP,SCP1
	$V_{\rm bs}$		SCP3
	$V_{\rm ds}$		SCP2
3	$L_{\rm gate}$		PARL2,SC1
	$V_{\rm bs}$		SC3
	$V_{\rm ds}$		SC2
(a)			
4	$V_{\rm bs}$	subthreshold	NSUBC,VFB
	$V_{\rm ds}$: low		MUECB0,MUECB
	$V_{\rm gs}$		
5	$V_{\rm bs}$	saturation	MUEPH1,MUESR1
	$V_{\rm ds}$: high		
	$V_{\rm gs}$		
6	$V_{\rm bs}$	subthreshold	NSUBP
	$V_{\rm ds}$: both		SCP1,SCP2,SCP3
	$V_{\rm gs}$		SC1,SC2,SC3
(b)			
7	$V_{\rm bs}$	saturation	VOVER,VOVERP
	$V_{\rm ds}$		XLD,VMAX
	$V_{\rm gs}$		
(c)			
8	$V_{\rm bs}$	subthreshold	BGTMP2
	$V_{\rm ds}$: high		
	$V_{\rm gs}$		
9	$V_{\rm bs}$	saturation	MUETMP
	$V_{\rm ds}$		
	$V_{\rm gs}$		
(d)			

refine the extraction of the model parameters for short-channel effects and the pocket implantation as well as to obtain the mobility parameters. For determining the gate overlap-related parameters and the carrier velocity, the saturation region data are then used. Finally, temperature-dependent parameters are extracted from the respective measurements. After the initial extraction of all parameters, it is recommended to repeat the extraction again, beginning with the basic device parameter determination from long-channel transistor data, in order to get a parameter fine tuning and a consistency check.

VIII. Conclusion

The development trend in compact modeling goes toward surface potential-based approaches and leads to models with high accuracy and less model parameters. The main motivation for this trend is to realize RF circuits with MOSFETs, where many higher-order phenomena affect the circuit performance. The surface potential-based description brings compact modeling for circuit simulation much closer to reality. This is because the surface potentials, solutions of the Poisson equation, provide the device physical basis for deriving all possible MOSFET features. HiSIM is an advanced MOSFET model that turns these principles into practical reality.

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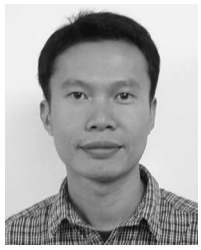

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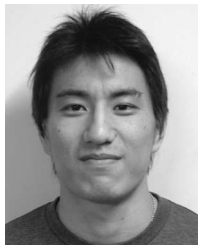

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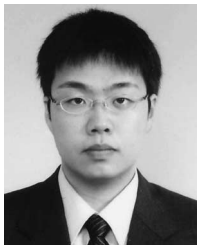

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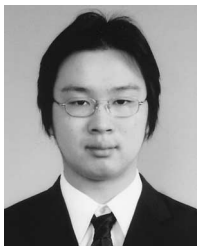

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