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Workfunction Tuning Using Various Impurities for Fully Silicided NiSi Gate

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Workfunction tuning by the implantation of various impurities and by changing silicidation conditions was investigated for a fully silicided NiSi gate. In the case of Sb implantation, it was found that the NiSi gate workfunction was decreased by 0.34 eV from 4.60 eV, for an undoped NiSi gate, to 4.26 eV due to the lowering of the silicidation temperature. Ge, which has not been used for workfunction tuning before, induced a decrease in NiSi gate workfunction in the same way. In the case of In implantation, a decrease in accumulation capacitance in capacitance–voltage (*C–V*) characteristics was observed. The origin of this problem was found to be void formation at the oxide interface. The voids were also found in NiSi predoped with Sb and silicided at 450°C or lower. [DOI: 10.1143/JJAP.44.3774]

KEYWORDS: nickel, silicide, workfunction, impurity, snowplow, pileup

1. Introduction

Metal gates are expected to replace poly-Si ones to solve problems such as a depletion effect and boron penetration for complementary metal oxide semiconductor (CMOS) devices. In order to maintain compatibility with the conventional CMOS fabrication process, the metal gates with dual workfunction values are demanded, 5.15 eV for p-MOS and 4.05 eV for n-MOS, comparable to present p^+- and n^+-poly-Si gates. For advanced CMOS devices, self-aligned silicide (SALICIDE) technology has been used[1] to obtain low sheet resistance for source, drain, and gate regions. Although the first salicide material to be used was $TiSi_2$, it was replaced by $CoSi_2$ and subsequently by NiSi to meet the demand for device scaling. Since Si consumption in the formation of a NiSi by silicidation is smaller than those in the formation of $TiSi_2$ and $CoSi_2$, it is suitable for scaled CMOS devices with a shallow junction.[2,3] Recently, fully silicided NiSi gates have been demonstrated with the extension of SALICIDE technology.[4–8] The workfunction of intrinsic NiSi is located near midgap of Si (4.6 eV). The NiSi workfunction can be tuned by the inducement of impurity pileup at the $NiSi/SiO_2$ interface. Impurities in poly-Si are swept out in the slicide growth direction by the silicidation (snowplow effect[9,10]) and pile up at the oxide interface.[6] The metal workfunction can be shifted if the impurities at the metal/oxide interface form high-density electric dipoles, as shown in Fig. 1.[11–13] Therefore, the impurity pileup at the $NiSi/SiO_2$ interface due to the snowplow effect is the key to tuning the NiSi workfunction. However, the NiSi workfunction shifts reported to date using P ($\Delta\Phi_{WF}$: -0.09 eV), As ($\Delta\Phi_{WF}$: -0.2 eV), Sb ($\Delta\Phi_{WF}$: -0.32 eV), and B ($\Delta\Phi_{WF}$: $+0.2$ eV)[6,7] are insufficient for both n-MOS and p-MOS devices. We have investigated the relationships among the NiSi workfunction, impurity species, and silicidation conditions. The impurities were used N, F, B, P, Sb, Ge, and In. In the case of Sb, the silicide formation temperature affected the modification of the workfunction. The relationship between impurity profile and workfunction shift is discussed for many impurities.

2. Experiments

The NiSi workfunction is extracted from the capacitance–voltage (*C–V*) characteristics of MOS diodes. The steps of the fabrication of fully silicided NiSi gate MOS diodes were as follows. Starting with p-Si substrates, LOCOS formation, gate oxidation, and gate poly-Si deposition were carried out, in turn. The thicknesses of the gate oxide and gate poly-Si were 10 nm and 100 nm, respectively. Then, impurities, N, F, Sb, As, P, B, Ge, or In, were implanted into the poly-Si gate. The implantation energy was in the range from 5 to 30 KeV. The implantation dose was 1.0×10^{15}, 2.5×10^{15}, or 5.0×10^{15} cm^{-2}. The implantation energy was adjusted so as not to implant the impurities directly into the gate oxide and the Si substrate. The combination of impurities and implantation condition are listed in Table I. After poly-Si gate patterning, Ni deposition by sputtering and full silicidation were carried out in the same vacuum chamber. The deposited Ni thickness was 60 nm. The standard silicidation temperature was 500°C. Lower-temperature silicidation at 450°C or

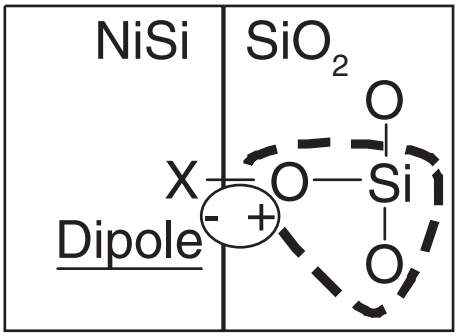

Fig. 1. Electric dipole model to explain workfunction shift at the NiSi/SiO_2 interface. X stands for impurity atoms that compose the pileup.

Table I. Impurity implantation conditions and V_{FB} shift.

	Dose (cm^{-2})	Energy (KeV)	ΔV_{FB} (V)
N	5.0×10^{15}	10	~0
F	2.5×10^{15}	10	~0
B	1.0×10^{15}	5	>0
P	5.0×10^{15}	15	<0
Sb	5.0×10^{15}	30	<0
Ge	5.0×10^{15}	30	<0
In	5.0×10^{15}	30	<0

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400°C was carried out for a limited number of cases. Silicidation time was changed depending on the silicidation temperature. Finally, the unreacted Ni removal using a wet etchant ($H_2SO_4 : H_2O_2 = 4 : 1$, or $H_3PO_4 : HNO_3 : CH_3COOH : H_2O = 3 : 3 : 1 : 1$) and post metallization annealing (PMA) were carried out to complete the MOS diode fabrication.

3. Flat-Band Voltage Shift and Various Impurities

Table I shows a brief summary of values of ΔV_{FB} for various impurity species. The *C–V* characteristics of NiSi MOS diodes predoped with Sb, As, P, B, and Ge showed a flat-band voltage shift, and those predoped with N and F showed no shift. N and F depth profiles in the NiSi MOS structure obtained by the back-side SIMS technique are shown in Fig. 2. Both F and N pileup at the oxide interface are seen, but the pileup peak concentrations at the oxide interface are approximately $1.0 \times 10^{20}\,cm^{-3}$, which are lower than those for Sb shown in Fig. 3. Therefore, the low amount of impurities at the oxide interface accounts for the lack of V_{FB} shift. Since the N and F peak concentrations in the NiSi film are higher than those at the interface, the snowplow effect dose not seem to be effective for pileup formation for these species. In the case of Sb, although a V_{FB} shift was observed as listed in Table I, the ΔV_{FB} value was affected by the silicidation conditions. On the basis of profile evaluation, the relationship between Sb pileup and ΔV_{FB} are discussed in the next section. It is noteworthy that Ge, which is not a dopant for Si, gave rise to a V_{FB} shift. This implies that the NiSi workfunction could be tuned with impurities other than the dopants for Si. In the case of In, complicated changes in *C–V* characteristics including a decrease in accumulation capacitance were observed. Concerning Ge and In, the details are described in another section.

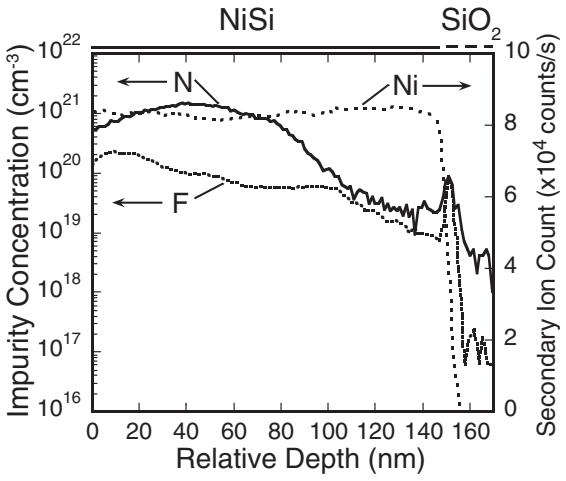

Fig. 2. F and N depth profiles obtained by back-side SIMS technique.

4. Pileup Formation and Flatband Voltage Shift with Sb Implantation

Detailed experimental results for Sb implantation are described in this section. Sb depth profiles in a NiSi MOS structure after full silicidation for various silicidation temperatures obtained by the back-side SIMS technique are shown in Fig. 3. The Sb profile for the silicidation temperature of 500°C shows a Gaussian-like profile that reflects an as-implanted profile. By lowering the silicidation temperature to 450°C, Sb concentration in NiSi was decreased. In contrast, Sb pileup at the oxide interface was increased by the lowering silicidation temperature. Sb pileup peak concentrations were $1.9 \times 10^{21}\,cm^{-3}$ and $3.0 \times 10^{21}\,cm^{-3}$ for 500°C and 450°C, respectively. Silicidation times were 5 min and 25 min, for the silicidation temperatures of 500°C, and 450°C, respectively. These results indicate that the probability of Sb segregation to the poly-Si side due to the snowplow effect is increased by lowering the silicidation temperature and silicidation rate, as reported by Ohdomari *et al.*[10] Figure 4 shows the *C–V* characteristics of NiSi:Sb fully silicided gate MOS diodes for various silicidation temperatures. Although silicidation at 500°C resulted in a small ΔV_{FB}, the V_{FB} shift for lower silicidation temperatures was larger than 0.3 V. It should be noted that ΔV_{FB} was not proportional to Sb concentration at the interface, as shown in Fig. 3. The workfunctions of undoped NiSi and NiSi:Sb were estimated to be 4.60 eV and 4.26 eV, respectively. The magnitude of the workfunction shift was nearly equal to the value reported by Kedzierski *et al.*,[7] despite the fact that the

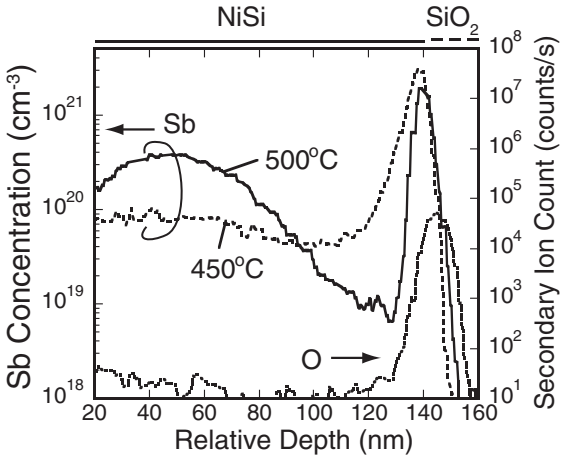

Fig. 3. Sb depth profiles obtained by back-side SIMS technique. The snowplow effect was promoted by silicidation temperature lowering that lead to pileup peak concentration increase.

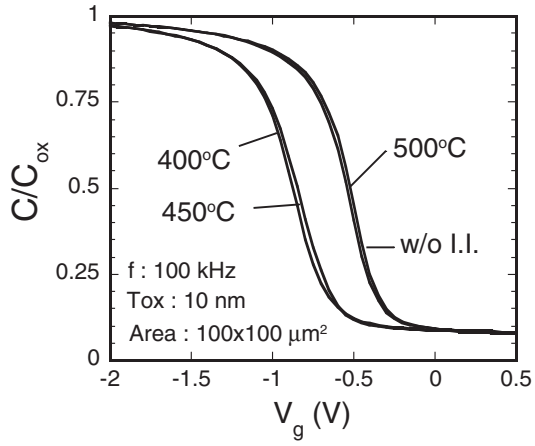

Fig. 4. *C–V* characteristics of NiSi gate diodes fabricated with Sb predoping. The V_{FB} shift changes according to the silicidation temperature.

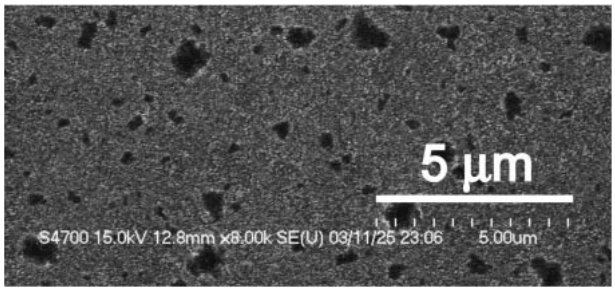

Fig. 5. Plan view SEM image for a NiSi:Sb film silicided at 400°C. Partial NiSi peeling off was found after unreacted Ni removal process.

Sb dose used in our work, $5 \times 10^{15}\,\mathrm{cm}^{-2}$, was twice that used in their experiment, $2.5 \times 10^{15}\,\mathrm{cm}^{-2}$. It was also reported by them that the workfunction was decreased by increasing P, As, and Sb doses, but its V_{FB} shift showed saturation for increasing P and As doses. On the basis of their results and our results, it is concluded that Sb also shows workfunction shift saturation against implantation dose. Pileup concentration could be increased by further reduction of the silicidation temperature or the introduction of annealing before silicidation to crystallize amorphized Si by Sb implantation.[9] However, pileup at the oxide interface may result in impurity precipitation at the oxide interface. Precipitation formation is one of the candidates that give rise to the workfunction shift saturation. In addition, silicidation at 450°C or lower showed NiSi film peeling, as shown in Fig. 5. The peeling is attributed to void formation at the interface. Since this void formation is severer for NiSi:In, this problem is discussed again in the next section. Consequentially, simply increasing the implantation dose and lowering the silicidation temperature to enhance the snowplow effect are not a valid solution for obtaining a larger V_{FB} shift.

5. Possibility of Workfunction Shift with Ge and In Implantation

It has been experimentally shown that the NiSi workfunction is increased with acceptor-type impurities, such as B and Al, and decreased with donor type impurities, such as P, As, and Sb. However, the mechanism for this behavior is not clear. Therefore, whether or not use of the group IV element Ge affects the workfunction, to date, was not known. As previously described, Ge implantation leads to a decrease in workfunction in the same way as donor impurities. Ge depth profiles in the NiSi MOS structure obtained by the back-side SIMS technique are shown in Fig. 6. The Ge implantation doses were $1.0 \times 10^{16}\,\mathrm{cm}^{-2}$ and $5.0 \times 10^{15}\,\mathrm{cm}^{-2}$. The silicidation temperature was 500°C. The Ge concentration at the oxide interface and in a NiSi film increased by approximately twice nearly proportionally to the Ge dose. The Ge pileup peak concentrations at the oxide interface are $2.0 \times 10^{21}\,\mathrm{cm}^{-3}$ and $5.0 \times 10^{21}\,\mathrm{cm}^{-3}$ for the implantation doses of $5.0 \times 10^{15}\,\mathrm{cm}^{-2}$ and $1.0 \times 10^{16}\,\mathrm{cm}^{-2}$, respectively. These Ge concentrations are comparable to Sb peak concentration shown in Fig. 3. However, ΔV_{FB}, as shown in Fig. 7, was approximately -0.1 V for both cases. This result means that the V_{FB} shift is not proportional to impurity concentration at the oxide interface, in the same way as shown above for NiSi:Sb and for Mo:N, as reported

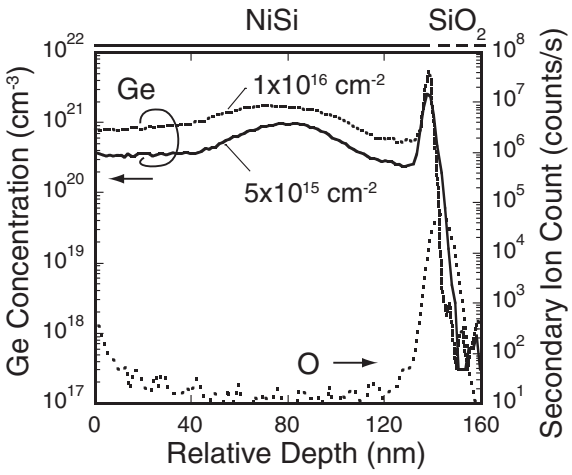

Fig. 6. Ge depth profiles obtained by back-side SIMS technique. The amount of Ge pileup was increased by increasing the Ge implantation dose.

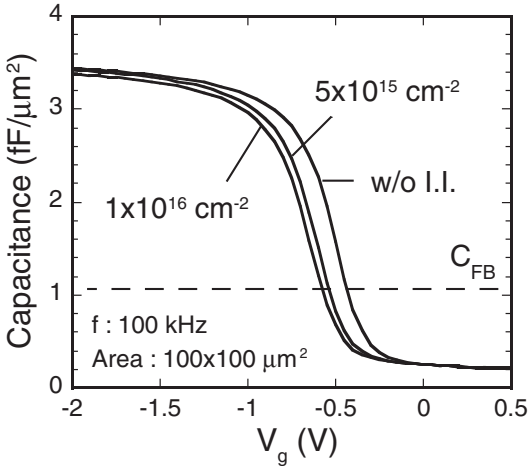

Fig. 7. *C–V* characteristics of NiSi gate diodes with Ge. V_{FB} shift induced by increasing the Ge implantation dose was approximately -0.1 V.

by Hino *et al.*[13] Although the fact that the Ge pileup gives rise to a workfunction shift is interesting, the shift value itself is too small to be of practical use. The lowering of the silicidation temperature was not as effective for Ge as it was for Sb. For some specimens, As, P or B was implanted in addition to Ge with the expectation of synergistic enhancement of the workfunction shift. However, this attempt did not markedly improve the shift magnitude.

Figure 8 shows the *C–V* characteristics of NiSi:In gate MOS diodes silicided at 500°C. A decrease in accumulation capacitance in *C–V* characteristics and a V_{FB} shift were observed. We speculate that In driven to the oxide interface formed a interfacial layer by reacting with the oxide, which lead to charge formation and an increase in insulator thickness. To judge the accuracy of this speculation, SiN was deposited on the gate oxide film to prevent the interfacial reaction. As a result, although the V_{FB} shift was suppressed, the accumulation capacitance reduction remained, as shown in Fig. 9. Cross-sectional observation by SEM revealed that the capacitance reduction is attributed to void formation at the interface, as shown in Fig. 10. The

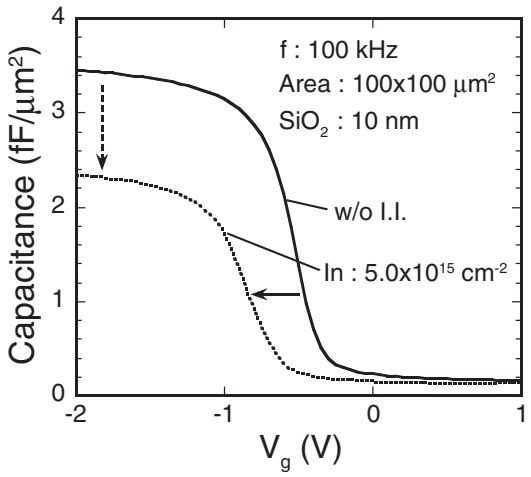

Fig. 8. *C–V* characteristics of NiSi gate diodes with In. Gate insulator was SiO_2.

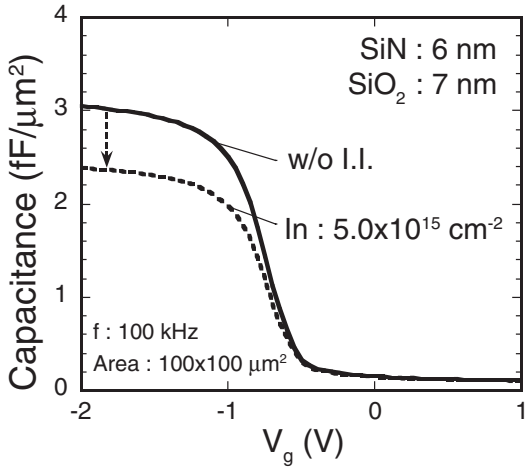

Fig. 9. *C–V* characteristics of NiSi gate diodes with In. Gate insulator was SiN/SiO_2. SiN was deposited on SiO_2 to prevent interfacial reaction.

voids were also found in the NiSi:Sb MOS structure. However, in the case of Sb, the void formation was limited to structures silicided at a temperature of 450°C or lower. Although the void formation mechanism is not yet clean, we are certain that impurity concentration in the vicinity of the interface is the key factor. This voiding should be noted as a potential problem against the practical use of a fully silicided NiSi gate.

6. Conclusion

The workfunction tuning of NiSi gate MOS diodes was investigated with predoping of various impurities and full silicidation technique. It was found that for Sb silicidation temperature is an important key factor for enhancing the snowplow effect and enlarging the workfunction shift. Ge,

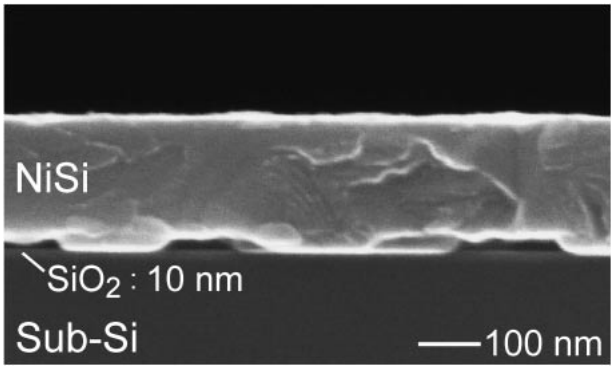

Fig. 10. SEM cross section of $NiSi:In/SiO_2/Si$ interface. Voids at the $NiSi/SiO_2$ interface were seen.

which is not a dopant for Si, was shown to induce a workfunction shift for the first time. However, the shift obtained with Ge implantation was too small to be of practical use. Side effects, such as interfacial reaction and void formation, were found for In. Not only the enlargement of the workfunction tunable range but also the classification of the origins of these side effects are necessary to raise the NiSi workfunction tuning technique to a practical level.

Acknowledgements

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