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Control of Subthreshold Characteristics of Narrow-Channel Silicon-on-Insulator n-Type Metal–Oxide–Semiconductor Transistor with Additional Side Gate Electrodes

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A silicon-on-insulator (SOI) n-type metal–oxide–semiconductor (MOS) transistor with additional side gate electrodes is fabricated and its subthreshold characteristics are discussed. Since its device structure provides independent biasing to gates, flexible device-characteristic control for the respective device is expected. The key fabrication process is the formation of transistor gates. Additional side gate electrodes are formed by reactive ion etching (RIE) with a SiO_2-covered top gate as an etching mask. Subthreshold characteristics are improved by negative side-gate biasing. In addition, the side-gate voltage V_{SG} required to decrease off-leakage current by one decade is around 100 mV. Since the sidewall oxide thickness is chosen to be 5 nm, which is the same as the top-oxide thickness, rather sensitive subthreshold-characteristic control compared with that of biasing through a thick buried-oxide layer is achieved in response to performance requirement. In the viewpoint of stand-by-power suppression, these provide a certain controllability to a circuit operation. [DOI: 10.1143/JJAP.46.dummy]

KEYWORDS: SOI, multigate, VTCMOS, DTMOS, three-dimensional structure

1. Introduction

The suppression of stand-by power is one of the key issues on very large scale integration (VLSI) circuits in the decananometer range in particular. Therefore, it has been studied to control the threshold voltage of a metal–oxide–semiconductor (MOS) transistor by various substrate biasing tequniques.[1,2] For multigate devices on silicon-on-insulator (SOI), there are possibilities to control respective device characteristics by independent voltage biasing for a respective gate electrode.[3] This device-characteristic control provides a certain controllability to a circuit operation. From this viewpoint, a narrow-channel SOI MOS transistor with additional side gate electrodes, as shown in Fig. 1, is fabricated and investigated for its subthreshold behavior to control its device characteristics. A gate electrode and side electrodes on both sidewalls are electrically separated by thermal oxide, leading to an independent biasing to an SOI channel. By choosing the thickness of sidewall oxide, sensitive subthreshold-characteristic control compared with that of biasing through a thick buried-oxide layer[4] can be expected.

Figure 2 shows the simulated I_D–V_G characteristics of the device.[5] Its gate-oxide thicknesses are 5 nm in both the top and side regions of the SOI channel. The improvement of subthreshold behavior and the suppression of off-leakage current are observed when additional gate electrodes are negatively biased. From these results, the sensitive control of threshold voltage and leakage current can be realized.

2. Device Fabrication

To realize device-characteristic control by additional side-gate biasing mentioned above, the formation of electrically separated electrodes in the top and side regions of the SOI channel is required. A novel technique utilizing the top gate as an etching mask for side-electrode formation shown in Fig. 3 is newly developed to realize the separation. The key process is the isolation-layer formation of these gate electrodes.

P-type, 10 Ω cm, (100) SOI wafers are used. An SOI channel of 300-nm height is formed by RIE. The channel width ranges from 200 to 1000 nm. After gate-oxide formation on the sidewall by thermal oxidation, polycrystalline silicon (poly-Si) for side gate electrodes is deposited by chemical vapor deposition at 635 °C and doped with phosphorus using a $POCl_3$ source at 1000 °C. Subsequent leveling for removing polycrystalline silicon in the top

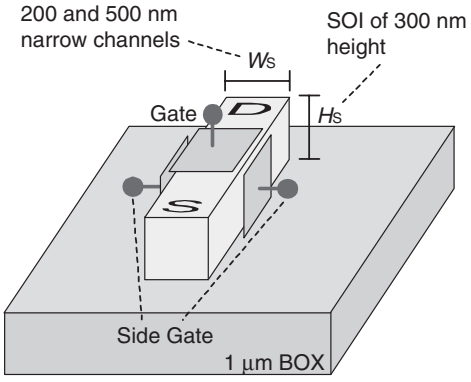

Fig. 1. Narrow-channel SOI MOSFET with additional gate electrodes. These gate electrodes are formed on both sides of an SOI channel.

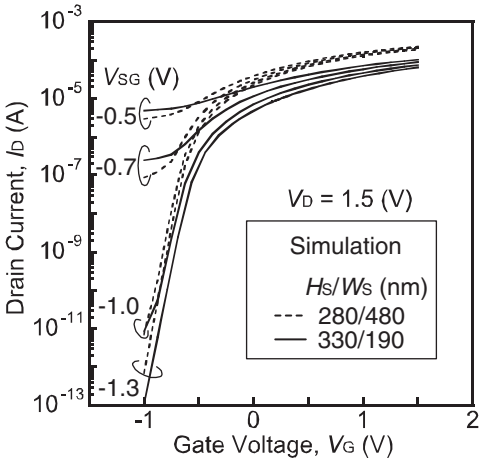

Fig. 2. Simulated I_D–V_G characteristics of device with gate oxide of 5-nm thickness. Subthreshold characteristics are improved in both devices when side-gate electrodes are negatively biased.

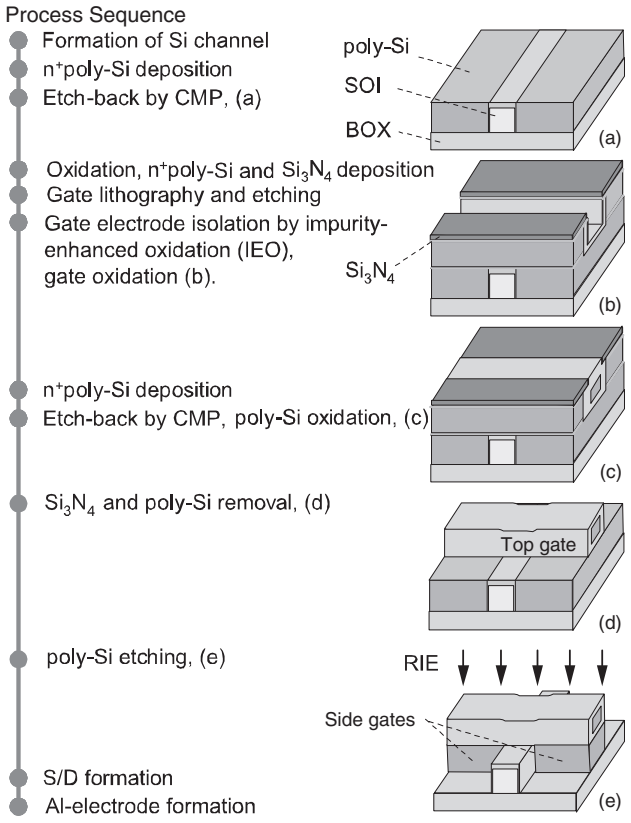

Fig. 3. Developed process sequence of the device. The top gate electrode is formed on a CMP etch-backed surface and covered with oxide (c). Two side gate electrodes are formed by RIE, utilizing the top gate electrode as an etching mask (e).

region of the channel is achieved by chemical mechanical polishing. A groove pattern that will be used afterwards to form gates is etched in a stencil polycrystalline silicon film, as shown in Fig. 3(b). Since top gate and isolation oxides are formed simultaneously, as shown in Fig. 4(a), it is required to increase the ratio of the oxide thickness on the side gate to that on the SOI channel. To meet the requirement, impurity

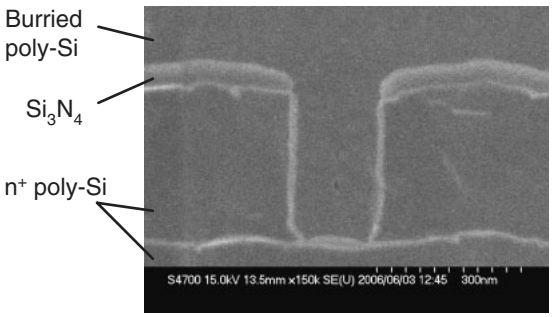

Fig. 5. SEM image of isolation layer formed by IEO at 850 °C. The thickness of the isolation oxide and the top gate oxide are 20 and 4.7 nm, respectively.

enhanced oxidation (IEO)[6] is performed. The oxidation characteristics of the phosphorous-doped poly-Si and boron-doped substrates are shown in Fig. 4(b). The ratio exceeds almost 4.4 at 850 °C when the oxide thickness on the silicon substrate becomes 5 nm. Figure 5 shows the isolation layer formed by IEO at 850 °C.

After IEO, poly-Si for top gate electrodes is deposited and doped with phosphorus using a $POCl_3$ source. The top of the electrode is leveled by chemical mechanical polishing and covered with its own thermal oxide. Side electrodes are formed by RIE with the SiO_2-covered top gate as an etching mask. The SEM image of the obtained structure is shown in Fig. 6. A separated gate structure is successfully fabricated. The source and drain formation is achieved by arsenic ion implantation and subsequent rapid thermal annealing at 900 °C. The gate-oxide thicknesses are 4.7 nm for the top electrode and 4.8 nm for side electrodes. To evaluate rude channel performance, no channel implantation is performed.

3. Results and Discussion

The device can be operated not only as a fixed-side-gate-biasing transistor but also as a typical trigate transistor, as shown in Fig. 7. The experimental I_D–V_G characteristics of devices in these operations with ratios of channel width to

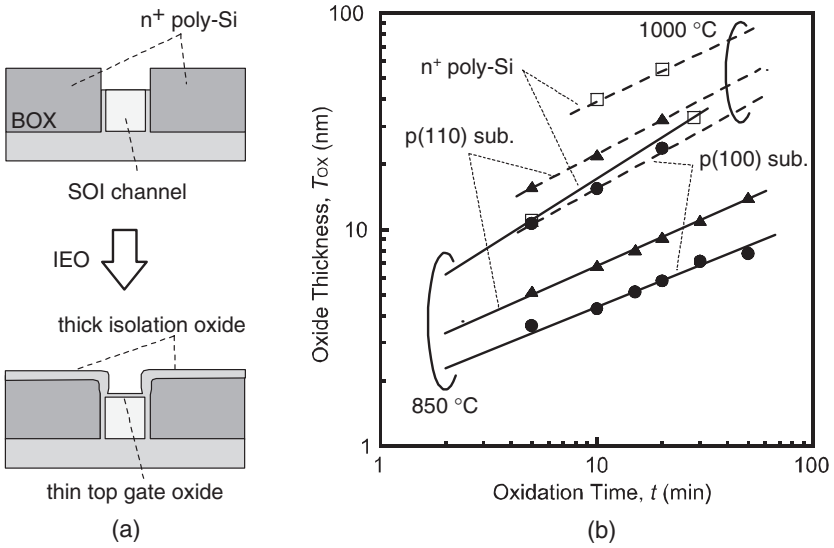

Fig. 4. Gate electrode isolation (a) and dry-oxidation characteristics of boron-doped Si substrates and n^+poly-Si film at 850 and 1000 °C (b). Resistivities of Si substrates and n^+poly-Si film are 10 and 5×10^{-4} Ω cm, respectively. The ratio of oxide thickness exceeds 4.4 at 850 °C.

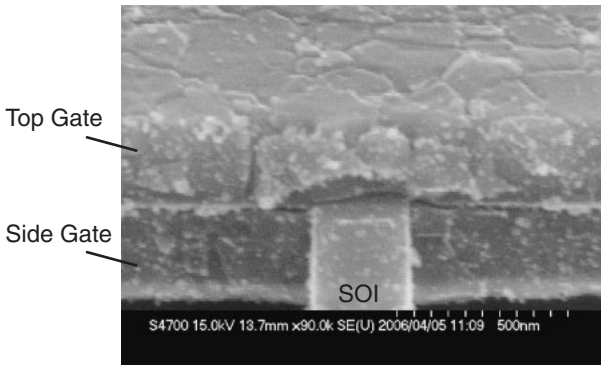

Fig. 6. SEM image of fabricated gate structure. Additional side gate electrodes are successfully formed on both sides of the narrow SOI channel.

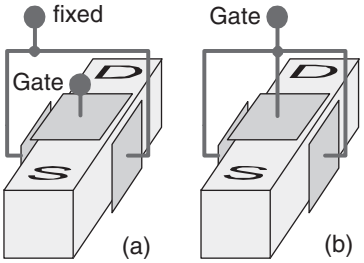

Fig. 7. Gate-biasing modes of the device. Fixed-side-gate-biasing (a) and trigate (b) operations.

height (H_S/W_S) of 190/330 and 480/280 are shown in Fig. 8. As clarified by device simulation, improvements in subthreshold-current characteristics by side-gate-biasing and threshold-voltage variations between operation modes are observed. These are summarized in Fig. 9. The *S*-parameter is 79.8 mV/decade in the trigate operation of both devices and varies from 95 to 150 mV/decade in the fixed-V_{SG} operation. The threshold-voltage variation from that of the trigate operation, ΔV_{TH}, achieves 170 mV at $V_{SG} = -1.0$ V in both devices, though their *S*-parameters are held at 95 and 117 mV/decade. At $V_{SG} = -0.5$ V, the $S/\Delta V_{TH}$ gradient increases rapidly compared with that at $V_{SG} = -1.0$ V. Subthreshold characteristics change sensitively in this V_{SG} region. The detailed behavior of subthreshold current according to the side-gate-biasing variation is shown in Fig. 10. Subthreshold currents change sensitively as side gate electrodes are negatively biased and these are suppressed in both devices with different H_S/W_S ratios effectively. Figure 11 shows the V_{SG} dependence of off-leakage current at a certain fixed gate voltage. Off-leakage current can be decreased by 100 and 125 mV V_{SG} biasing per one decade in both devices. These sensitive responses to the additional side-gate biasing can be realized because of the thin oxide layer of 4.8 nm thickness.

4. Conclusions

An SOI nMOSFET with self-aligned side gate electrodes is fabricated and its subthreshold characteristics are discussed. To form electrically separated gate electrodes in the top and side regions of an SOI channel, a novel technique utilizing the top gate as an etching mask for side-electrode formation is adopted. The device is successfully fabricated

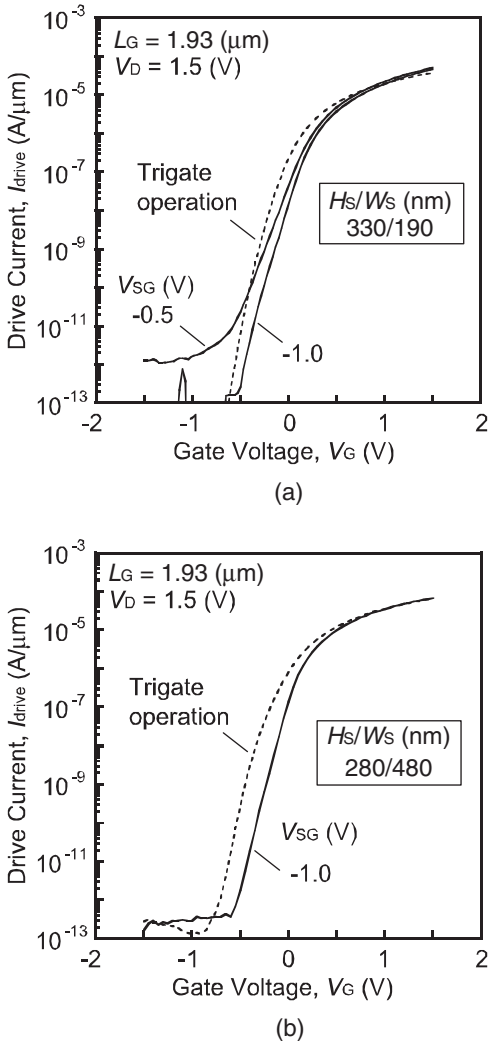

Fig. 8. Experimental I_D–V_G characteristics of the device. As clarified from device simulation, an improvement in subthreshold behavior by side-gate biasing (a) and a variation in threshold voltage are observed.

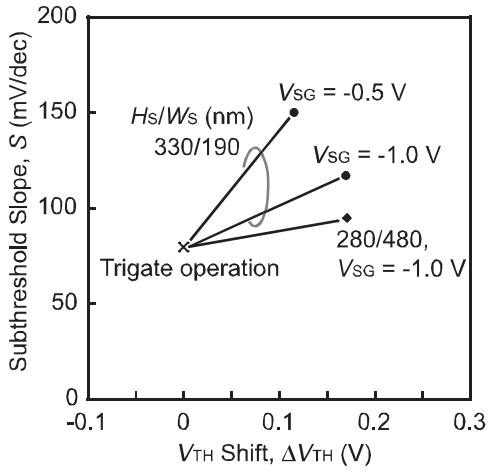

Fig. 9. Dependences of threshold voltage and subthreshold slope on side-gate biasing. V_{TH} is defined to be the gate voltage at the drive current, the drain current per unit gate width, achieve at 100 nA/μm and ΔV_{TH} is defined to be the V_{TH} difference from that of the trigate operation. It is observed that an increase in the *S*-parameter of the device with an H_S/W_S ratio of 280/480 is smaller than that with an H_S/W_S ratio of 330/190.

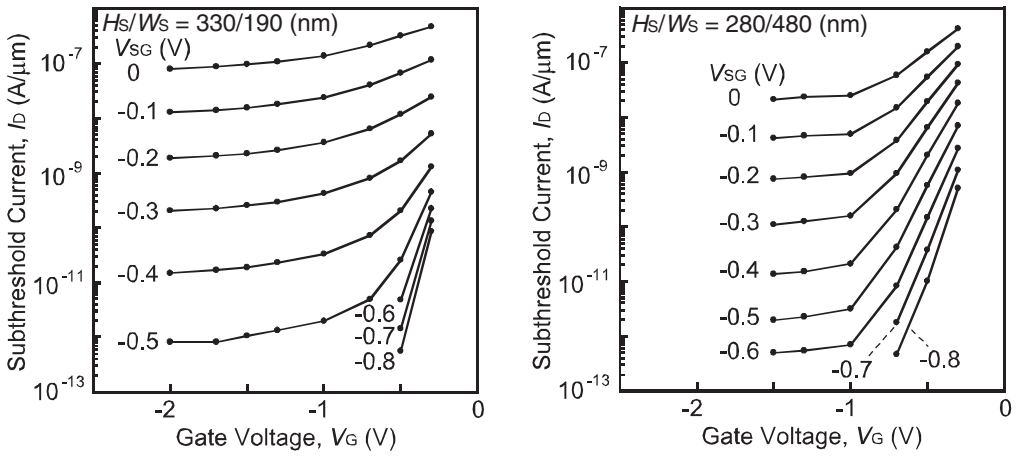

Fig. 10. Detailed subthreshold behavior of devices. Subthreshold-leakage current changes sensitively as additional gate electrodes are biased negatively and is suppressed effectively in both devices.

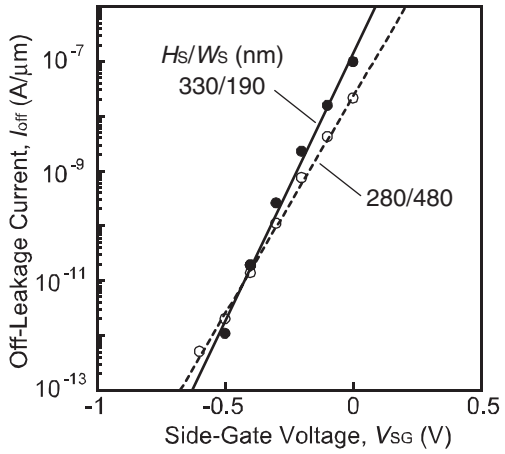

Fig. 11. Off-leakage current characteristics. The side-gate voltage V_{SG} required to decrease off-leakage current by one decade is around 100 mV.

by impurity-enhanced oxidation to isolate gate electrodes. Threshold-voltage variations are observed and leakage current is suppressed by a small side-gate voltage biasing. These sensitive responses are clarified by device simulation. From these results, this device structure can provide a realistic circuit application in response to performance requirement in the viewpoint of variable threshold-voltage control.

Acknowledgements

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