# 3. 開催したワークショップおよびシンポジウム概要

# 3.1 概要

**●第 1 回ワークショップ　2003 年 3 月 17 日　広島大学学士会館**

・中心テーマ：　拠点形成計画概要、MOS デバイスモデル HiSIM
・参加者：58 名（大学 45 名、産業界 13 名）
・招待講演：　Noll 教授（ドイツ Archen 大） Lee 教授（韓国 KAIST）
和田教授（米国 MIT） 廣瀬全孝センター長（次世代半導体技術研究センター）
竹本社長（半導体理工学研究センター）
・COE メンバー講演およびポスターによる発表 18 件

**●第 2 回ワークショップ　2004 年 1 月 30 日　広島大学学士会館**

・中心テーマ：　デバイスモデリング
・参加者 : 68 名（大学 57 名、産業界 11 名）
・招待講演：　Zhipping Yu 教授（中国 Tsinghua University）
Gerald Wachutka（ドイツ Munich University of Technology）
Mansun Chan 教授（香港大学）　石橋孝一郎氏（(STARC ）
・COE メンバー成果報告、ポスター発表 22 件

**●第 3 回ワークショップ　2004 年 12 月 6 日　広島大学学士会館**

・中心テーマ：　超 LSI 製造技術とワイヤレス通信技術の将来
・参加者 : 138 名（大学 129 名、産業界 9 名）
・招待講演：　Karen Maex 教授（ベルギー Leuven Catholic 大学）
Frank Chang 教授（米国 UCLA）Simon Wong 教授 ( 米国 Stanford 大学 )
K. O 教授（フロリ ダ大学）　河野修興教授（広島大学・医師薬学総合研究科）
・COE メンバー成果報告、ポスターによる研究発表 50 件

**●第 4 回ワークショップ　2005 年 9 月 16 日　広島大学学士会館**

・中心テーマ：　デバイスモデリング
・参加者 : 100 名（大学 88 名、産業界　12 名）
・招待講演：　T. P. Ma 教授（米国　Yale 大学）　J. C. S. Woo 教授（米国 UCLA）
S. Biesmans 博士（ベルギー IMEC）　Y. J. Park 教授（韓国ソウル大学）
F. Boeuf 博士（ST Microelectronics）　黒田忠弘教授 ( 慶応大学 )
丹羽正昭博士 ( 松下電器 )
・COE メンバー成果報告、ポスター発表 50 件

**●半導体シンポジウム　2006 年 6 月 26 日　キャンパスイノベーションセンター、東京都港区**

・中心テーマ：　インタコネクションと三次元集積
・参加者 : 93 名（大学 27 名、産業界 46 名）
・招待講演：　黒田忠広教授 ( 慶應義塾大学 )　和田一実教授 ( 東京大学 )
田中徹助教授（東北大学）　池田博明 ( エルピーダメモリ株式会社 )
・COE メンバー：6 テーマについての講演、ポスター発表 17 件
・パネルディスカション・テーマ：インタコネクションと三次元集積

**●第 5 回ワークショップ　2007 年 1 月 29、30 日　キャンパスイノベーションセンター、東京都港区**

・中心テーマ：　ＣＯＥ最終成果報告
・参加者 : 107 名（大学 46 名、産業界 61 名）
・招待講演：　D. Antoniadis 教授（米国 MIT）
廣瀬全孝センター長（次世代半導体技術研究センター）
小柳光正教授（東北大学）　平本俊郎教授（東京大学）
・COE メンバー成果報告、ポスター発表 22 件

## 3.2　各ワークショップおよびシンポジウムのプログラム

●第１回ワークショップ　2003 年 3 月 17 日　　広島大学学士会館

第１回ワークショップ招待講演者および参加者

9:00　Openning Address
　　Univ. President, Prof. Taizo Muta
9:05　[Overview & Keynote]　"Targets and research plan of 21st century COE"
　　Profs. A. Iwata, H-J. Mattausch, M. Miura-Mattausch and H. Sunami
10:00　[Invited]　"Prospects of the 21st Century COE Program"
　　Dr. Masataka Hirose (AIST, MIRAI)

11:00　[Invited]　"Prospects　of the 21st Century COE Program"
　　Dr. Toyoki Takemoto (STARC)
12:00　Lunch
13:30　[Invited]　"Challenges and opportunities in the design of future systems on chip"
　　Prof. Tobias G. Noll　(Aachen Univ. of Technol.)"
14:30　[Invited]　"The impact of nm CMOS technology on wireless circuit and system"
　　Prof. Kwyro Lee　(KAIST)
15:30　[Invited]　"Silicon microphotonics - Photons meet LSIs" ]
　　Prof. Kazumi Wada（MIT)
16:30　"HiSIM: Present status and perspective"
　　Prof. Mitiko Miura-Mattausch

17:00　[Poster Presentations by COE Members]
"Advanced design for analog-digital mixed LSIs-Crosstalk noise evaluation and reduction-"
　　Atsushi Iwata, Mamoru Sasaki and Makoto Nagata
"Image segmentation/extraction using nonlinear pixel-parallel networks and thier VLSI implementation"
　　Hiroshi Ando, Takashi Morie and Atsushi Iwata"
"An analog VLSI chip calculating high-precision spatial and temporal derivatives of the vertebrate retina"
　　Seiji Kameda and Tetsuya Yagi

"Fully-parallel associative memory for fast pattern matching"
Yuji Yano, Minoru Honda, Masahiro MIZOKAMI, Tetsushi Koide and Hans Juergen Mattausch

"Digital-CMOS-Based Real-Time Color-Motion Picture Segmentation"
Takashi Morimoto, Youmei Harada, Tetsushi Koide and Hans Juergen Mattausch

"HiSIM-SOI: The First SOI-MOSFET Model for Circuit Simulation Based on the Complete Surface-Potential Description "
Daisuke Kitamaru, Yasuhito Uetsuji, Hiroaki Ueno and Mitiko Miura-Mattausch"

"High-Electric-Field Electron Transport at Silicon/Silicon-Dioxide Interface Inversion Layer"
Masayasu Tanaka, Osamu. Matsushima, Hiroaki Ueno and Mitiko Miura-Mattausch

"Optical Interconnection Technology at RCNS Hiroshima University"
Shin Yokoyama

"Silicon Integrated Antennas for Wireless Interconnects"
Takamaro Kikkawa

"Proposal of a Three-Dimensional MOS Transistor with High Drivability for Area-Efficient Applications"
Hideo Sunami

"Atomic-Layer Deposition of ZrO2 Gate Dielectrics with a Si Nitride Barrier Layer"
Anri Nakajima

"Workfunction Tuning Technique for Dual-Gate CMOS with Single Metal Gate"
Kentaro Shibarara

"Self-Assembling of Nanometer Si Dots and Their Application to Memory Devices"
Seiichi Miyazaki

"Multiple step electron charging in Si quantum-dot floating-gate MOS FETs "
Yusuke Shimizu, Mitsuhisa Ikeda, Hideki Murakami and Seiichi Miyazaki

"Electronic charged states of single Si quantum-dots with and without Ge core as detected by AFM/Kelvin probe technique"
Yudu Darma, Kohei Takeuchi, Hideki Murakami and Seiichi Miyazaki

18:30 Closing Remarks Prof. Hideo Sunami

18:45 Banquet

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## ●第２回ワークショップ　2004年1月30日　広島大学学士会館

第２回ワークショップ／ 招待講演者との会食

9:00 Recent Progress of the COE
A. Iwata
9:10 Low Power SoC Technology Development at STARC
K. Ishibashi (STARC)
10:10 "Ballistic MOS Model with Full 2D QM Correction"
Z. Yu (Tsinghua Univ.)
11:10 "Wireless Interconnection on Si LSI using Integrated Antenna"
T. Kikkawa
11:30 "Physics-Based Modeling of Electro-Magnetic Parasitic Effects in Interconnects"
G. Wachutka (TU Muenchen)
12:30 Lunch Break
14:00 "Modeling CMOS Non-Quasi-Static Effects in a Quasi-Static Simulation Engine"
M. Chan (Hong Kong Univ. ST)
15:00 "MOSFET Modeling for RF-CMOS Design"
M. Miura-Mattausch
16:00-18:00 [Poster Session]
18:30-20:00 Dinner (Cotton Club)

**[Posters]**

1. 1/f and Non-1/f Low Frequency Noise Measurements and their Modeling with HiSIM
H. Ueno, S. Matsumoto, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama
2. Toward Current-Characteristics Simulation for p-i-n Photodiodes Based on Spectral Method
K. Konno, O. Matsushima, K. Hara, G. Suzuki, and M. Miura-Mattausch
3. Optical properties of ring resonators on Si chips
Y. Tanushi, M. Wake, K. Wakushima, and S. Yokoyama
4. Etching Properties and Optical Emission Spectroscopy of NH3 Added C5F8 Pulse-Modulated ICP Plasma
M. Ooka and S. Yokoyama
5. Study in Structure and Fabrication Process of 3-Dimensional CMOS Transistor
K. Okuyama, K. Kobayashi, and H. Sunami
6. Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search with Large Reference Pattern Number
Y. Yano, T. Koide, H. J. Mattausch
7. Chip-architecture for automatic learning based on associative Memory and Short/LongTerm Storage Concept
M. Mizokami, Y. Shirakawa, T. Koide, and H. J. Mattausch
8. Improved Mixed Digital-Analog Nearest-Match Circuit for Fully-Parallel Assosiative Memories
K. M. Rahman, K. Kamimura, T. Koide, and H. J. Mattausch
9. Low-Power Digital Image Segmentation of Real-Time VGA-Size Motion Pictures
T. Morimoto, Y. Harada, O. Kiriyama, H. Adachi, T. Koide, and H. J. Mattausch
10. Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs
M. Ikeda, Y. Shimizu, T. Shibaguchi, H. Murakami, and S. Miyazaki.
11. Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by an AFM/Kelvin Probe Technique
Y. Darma, K. Takeuchi, and S. Miyazaki
12. Local Characterization of Electronic Transport in Microcrystalline Germanium Thin Films by Atomic Force Microscopy Using a Conducting Probe
K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki
13. Workfunction Tuning for Single-Metal Dual-Gate with Mo and NiSi Electrodes
T. Sano, M. Hino, and K. Shibahara

14. Wireless Chip Interconnect Using Resonant Coupling between Spiral Inductors
M. Sasaki, D. Arizono, and A. Iwata
15. Human Face Detection and Recognition Using Principle Component Analysis
H. Ando, N. Fuchigami, M. Sasaki, and A. Iwata
16. A Multi-chip Vision System with a PWM-based Line Parallel Interconnection
S. Kameda, M. Sasaki, and A. Iwata
17. Neural Sensing LSI with Wireless Interface
T. Yoshida, T. Mashimo, M. Akagi, and A. Iwata
18. CDMA Communication Chips for Highly Flexible Robot Brain
M. Shiozaki, T. Mukai, M. Sasaki, and A. Iwata
19. A Strategy Learning Model for Robot Brain
M. Ono, M. Sasaki, and A. Iwata
20. A Single Chip UWB Transmitter based on 0.18μm CMOS Technology for Wireless Interconnection
P. K. Saha, N. Sasaki, and T. Kikkawa
21. A Single Chip UWB Receiver based on 0.18μm CMOS Technology for Wireless Interconnection
N. Sasaki, P. K. Saha, and T. Kikkawa
22. Atomic layer deposition of $HfO_2$ for gate dielectrics
Y. Yokoyama, H. Ishii, and A. Nakajima

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## ●第３回ワークショップ　2004 年 12 月 6 日　広島大学学士会館


第３回ワークショップ招待講演者および COE 教員

**PLENARY SESSION 9:00 – 15:20**

9:00 Welcome Remarks
9:20 Opening Address
Taizo Muta, President, Hiroshima University
9:40 Recent Progress of the COE
Atsushi Iwata, COE Leader
10:00 [Invited] Characterization and optimization of Cu-Low k for 45nm and beyond
Karen Maex, IMEC, Katholik University, Leuven, Belgium

10:40 [Invited] Design with On-Chip Interconnect Inductance
S. Simon Wong, Stanford University, CA, USA

11:20 [Invited] Recent Advances of Diagnoses and Therapeutics in Practical Medicine
Nobuoki Kohno, Graduate School of Biomedical Sciences, Hiroshima University

12:00 – 13:30 Lunch Break

13:30 [Invited] Advanced RF/Baseband Interconnects for Future ULSI Communications..
Mau-Chung Frank Chang, University of California, Los Angeles, CA, USA

14:10 [Invited] Wireless Communications Using Integrated Antennas
Kenneth K O, University of Florida, FL, USA

14:50 ULSI Wireless Interconnection using Integrated Antennas for UWB Signal Transmission
Takamaro Kikkawa, RCNS, Hiroshima University

**[POSTER SESSION] 15:30 – 17:00**

P-01 Three Dimensional Integration Architecture for Tera-bit Information processing
A. Iwata, M. Sasaki, T. Yoshida, S. Kameda, H. Ando, M. Shiozaki, M. Ono and K.Sasaki

P-02 A Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors
Mamoru Sasaki, Daishuke Arizono and Atsushi Iwata

P-03 A Low-Noise Circuit Technique for Sensing the Nerve Signals
T. Yoshida, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu

P-04 A Brain-type Multi-chip Vision System with a PWM-based Line Parallel Interconnection
Seiji Kameda, Masaki Odahara and Atsushi Iwata

P-05 A Prototype Software System for Multi-object Recognition and its FPGA Implementation
H. Ando, N. Fuchigami, M. Sasaki and A. Iwata

P-06 A 2.7Gcps and 7-multiplexing CDMA Serial Communication Chip for Real-time Robot Control
Mitsuru Shiozaki, Toru Mukai, Masahiro Ono, Mamoru Sasaki and Atsushi Iwata

P-07 A Module based Robust Learning System to Environmental Change for Robot Brain
Masahiro Ono, Mamoru Sasaki and Atsushi Iwata

P-08 A Stereoscopic System with Integration of Multiple Features
Kan'ya Sasaki, Seiji Kameda, Hiroshi Ando, Mamoru Sasaki and Atsushi Iwata

P-09 Associative Memory-Based Systems with Recognition and Learning Capability
H. J. Mattausch, T. Koide

P-10 Real-Time Character Recognition System Using Associative Memory Based Hardware
A. Ahmadi, Y. Shirakawa, M. A. Abedin, K. Takemura, K. Kamimura, H. J. Mattausch, and T. Koide

P-11 Low-Power Video Segmentation by Pipeline Processing of Tiled Images
T. Morimoto, H. Adachi, O. Kiriyama, Z. Zhu, T. Koide, and H. J. Mattausch

P-12 Efficient Object Tracking Algorithm using Image Segmentation and Pattern Matching
O. Kiriyama, T. Morimoto, H. Adachi, Z. Zhu, T. Koide, and H. J. Mattausch

P-13 Multi-view Face Detection and Recognition using Haar-like Features
Z. Zhu, T. Morimoto, H. Adachi, O. Kiriyama, T. Koide, and H. J. Mattausch

P-14 Unified Data/Instruction Cache with Bank-Based Multi-Port Architecture
K. Johguchi, Z. Zhu, H. J. Mattausch, T. Koide, and T. Hironaka

P-15 Multi-bank based Switch Architecture with Flexible Scheduled Buffering of Packets
T. Fujii, K. Kobayashi, T. Koide, H. J. Mattausch, and T. Hironaka

P-16 A Carrier Transit Time Delay-Based Non-Quasi-Static MOSFET Model for Circuit-Simulation
Dondee Navarro, N. Nakayama, Y. Takeda, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro,T. Iizuka, M. Taguchi and S. Miyamoto

P-17 Frequency-Domain-Based Carrier Transport Model for a Lateral p-i-n photodiode
K. Konno, O. Matsushima, K. Hara, G. Suzuki, D. Navarro and M.Miura-Mattausch

P-18 Fully-Depleted SOI-MOSFET Model for Circuit Simulation and its Application to 1/f Noise Analysis
N. Sadachika, Y. Uetsuji, D. Kitamaru, L. Weiss, U. Feldmann, S. Baba, H. J. Mattausch and M. Miura-Mattausch

P-19 A TH-UWB Transmitter and its Pulse Generation Circuit for Intra/Interchip Wireless Interconnection
Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa

P-20 Design and Measurement of On-Chip CMOS UWB Receiver
Nobuo Sasaki, Pran Kanai Saha and Takamaro Kikkawa

P-21 Transmission characteristics of Gaussian monocycle pulse for inter-chip wireless interconnection using integrated antenna
K. Kimoto and T. Kikkawa

P-22 RF Measurement of Permittivity of Low-k films on Si
K. Isari and T. Kikkawa

P-23 Photosensitive porous low-k interlayer dielectric film
Shin-Ichiro Kuroki and Takamaro Kikkawa

P-24 Effect of Hexamethyldisilazane on Moisture Adsorption of Porous Silica Films
Shin-Ichiro Kuroki and Takamaro Kikkawa

P-25 Single-Metal Tunable-Workfunction Technology with NiSi and Mo Gate Electrode
T. Hosoi, K. Sano, M. Hino, N. Ooishi and K. Shibahara

P-26 Green laser annealing with metal absorber
K. Shibahara, A. Matsuno, E. Takii, K. Kurobe and T. Eto

P-27 Low-Resistive and Low Leak Current Ultra-Shallow n+/p Junction Formed by Heat- Assisted Excimer Laser Annealing
Ken-ichi Kurobe, Yoshinori Ishikawa, Takanori Eto, Akira Matsuno, and Kentaro Shibahara

P-28 Study in 3-D MOS Transistor Formation
K. Okuyama, K. Kobayashi, S. Matsumura, K. Yoshikawa and H. Sunami

P-29 Novel Doping Profile Evaluation for 3-D MOS Transistor .
K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara, and H.Sunami

P-30 Characterization of 1.55-μm Infrared Light Propagation in SOI Waveguide
Masato Kawai, Tetsuo Tabei, and Hideo Sunami

P-31 Characterization of Charged States of Silicon-Based Quantum Dots and Its Application to Floating Gate MOS Memories
S. Miyazaki

P-32 Characterization of Atom Diffusion in Polycrystalline Si/SiGe/Si Stacked Gate
H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi and S. Miyazaki

P-33 Crystallization of Amorphous Si films on Glass Substrate Using Plasma Jet and Its Application to Thin Film Transistor Fabrication
S. Higashi, H. Kaku, T. Okada, H. Taniguchi, H. Murakami and S. Miyazaki

P-34 Local Electronic Transport through Si Dot with Ge Core as Detected by AFM Conductive Probe
Yudi Darma and Seiichi Miyazaki

P-35 Fabrication of Multiply-Stacked Structures of Si Quantum-Dots Embedded in SiO2 by Combination of Low-Pressure CVD with Remote Plasma Treatments
K. Makihara, H. Nakagawa, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki

P-36 High-Rate Growth of Highly-Crystallized Si Films from VHF Inductively-Coupled Plasma CVD
Nihan Kosku and Seiichi Miyazaki

P-37 Electrical characterization of HfAlOx/SiON dielectric gate capacitors
Yanli Pei, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki

P-38 Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on $NH_3$-nitrided Si(100)
H. Nakagawa, A. Ohta, F. Takeno, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki

P-39 Charging and Discharging Characteristics of Stacked Floating Gates of Silicon Quantum Dots
T. Shibaguchi, M. Ikeda, H. Murakami and S. Miyazaki

P-40 Photo-Induced Electron Charging to Silicon-Quantum-Dot Floating Gate in Metal-Oxide-Semiconductor Memories
T. Nagai, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki

P-41 Technology for Optical Interconnection in LSI
Shin Yokoyama, Yuichiro Tanushi, Zhimou Xu, Masato Suzuki, and Keita Wakushima
P-42 Simulation of Ring Resonator Optical Switches
Yuichiro Tanushi and Shin Yokoyama
P-43 Effect of annealing on the structural properties of spin-coated $Ba_{0.7}Sr_{0.3}TiO_3$ films
Zhimou Xu, Yuichiro Tanushi, Masato Suzuki, Keita Wakushima and Shin Yokoyama
P-44 Effect of $H_2$ adding and substrate bias to Cu sputtering
Masahiro Ooka and Shin Yokoyama
P-45 Anomalous Behavior of Interface Traps of Si MOS Capacitors Contaminated with Organic Molecules
Masato Suzuki and Shin Yokoyama
P-46 Development of nano-size mask for diamond emitter
Tetsuo Tabei, Tomihito Miyazaki, Yoshiki Nishibayashi and Shin Yokoyama
P-47 Interface Trap Generation on MOSFETs with Thin $SiO_2$ and Plasma-Nitrided $SiO_2$ Gate Dielectrics under Static and Dynamic Stresses
Shiyang Zhu, Anri Nakajima, Takuo Ohashi and Hideharu Miyake
P-48 Room Temperature Operation of an Exclusive-OR Circuit Using a Highly-Doped Si Single-Electron Transistor
Tetsuya Kitade, Kensaku Ohkura and Anri Nakajima
P-49 Atomic-layer deposition of ultrathin gate dielectrics and Si new functional devices
Anri Nakajima
P-50 [Invited] Non-Contact Impedance Sensor
Makoto Kaneko, Tomohiro Kawahara and Yukio Hosaka

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## ●第４回ワークショップ　2005年9月16日　広島大学学士会館

第４回ワークショップ招待講演者およびCOE教員

9:00 Welcome Remarks
9:10 Opening Address
Masaki Taniguchi, Vice President, Hiroshima University
9:30 Recent Progress of the COE
Atsushi Iwata, COE Leader, Hiroshima University
9:50 [Invited] System LSI: Challenges and Opportunities
Tadahiro Kuroda, Keio University

10:30 [Invited] High-k Gate Dielectrics for Future CMOS Technology
T. P. Ma, Yale University

11:10 [Invited] Sub-20 nm Novel Silicon-Based Transistors
J.C.S. Woo, UCLA

11:50 Lunch Break

13:10 [Invited] Scaling Challenges for Sub-45 nm Technologies
S. Biesemans, IMEC

13:50 [Invited] Device Simulation for Nano MOSFET and Scaling Issues
Y. J. Park, Seoul National University

14:30 [Invited] Conventional Bulk and Bulk+ Architectures for 45 nm Node
F. Boeuf, ST Microelectronics

15:10 Break

15:20 [Invited] Current Status of PVD Hf-Based High-*k* Gate Stack-Process Improvement on Drive Current
Masaaki Niwa, Matsushita Electric

16:00 Current Activities in Device and Process R & D of the COE
H. Sunami, S. Miyazaki, K. Shibahara, A. Nakajima, S. Yokoyama, and T. Kikkawa, Hiroshima University

**[POSTER SESSION]** 16:40 –18:00

P-01 A 3D Integration Architecture utilizing Wireless Interconnections for Implementing Hyper Brains
Atsushi Iwata, Mamoru Sasaki, Takeshi Yoshida, Seiji Kameda, Hiroshi Ando, Masahiro Ono,Kanya Sasaki, Daisuke Arizono, and Takamaro Kikkawa

P-02 A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication Scheme
Mamoru Sasaki and Atsushi Iwata

P-03 A brain-type vision system using a 3-dimensional integration with local and global wireless interconnections]
Seiji Kameda, Nobuo Sasaki, Daisuke Arizono, Masaki Odahara, Mamoru Sasaki, Takamaro Kikkawa and Atsushi Iwata

P-04 Robust Face Recognition Methods under Illumination Variations toward Hardware Implementation on 3DCSS"
H. Ando, N. Fuchigami, M. Sasaki and A. Iwata

P-05 A Layout Method of 20GHz Global Clock Distribution
Mitsuru Shiozaki, Atsushi Mori, Atsushi Iwata, Mamoru Sasaki

P-06 A Robust Modular Learning Model with Addition and Integration of Modules
Masahiro Ono, Mamoru Sasaki and Atsushi Iwata

P-07 A window-based stereoscopic system using a weighted average of costs aggregated with window size reduction
Kan'ya Sasaki, Seiji Kameda, Atsushi Iwata

P-08 A CMOS RF Front-End using Radiation Oscillator for Short-RangeWireless Communication
Toru Mukai, Atsushi Iwata and Mamoru Sasaki

P-09 A 1V Supply Low noise CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization
Yoshihiro Masui, Takeshi Yoshida, Takayuki Mashimo, Mamoru Sasaki and Atsushi Iwata

P-10 Systems with Recognition and Learning Capability Based on Associative Memory
Hans Juergen Mattausch, Tetsushi Koide

P-11 Real-Time Multi-Object Tracking Based on Highly Parallel Image Segmentation and Pattern Matching
Tetsushi Koide, Hans Juergen Mattausch, Takashi Morimoto, Hidekazu Adachi, Kosuke Yamaoka

P-12 Associative Memory Based Hardware Design for an OCR System and Prototyping with FPGA
Ali Ahmadi, Md. Anwarul Abedin, Kazuhiro Kamimura, Yoshinori Shirakawa, Kazuhiro Takemura, Hans Juergen Mattausch, Tetsushi Koide

P-13 Fully-Parallel Associative Memory Architecture Realizing Minimum Euclidean Distance Search
Md. Anwarul Abedin, Kazuhiro Kamimura, Ali Ahmadi, Hans Juergen Mattausch, Tetsushi Koide

P-14 Image-Scan Video Segmentation Architecture Based on Embedded Memory Technology
Takashi Morimoto, Hidekazu Adachi, Kosuke Yamaoka, Tetsushi Koide, Hans Juergen Mattausch

P-15 CAM-Based Huffman Coding Architecture for Real-Time Applications
Takeshi Kumaki, Yasuto Kuroda, Tetsushi Koide, Hans Juergen Mattausch, Hideyuki Noda, Katsumi Dosaka, Kazutami Arimoto, Kazunori Saito

P-16 Unified Data/Instruction Cache with Distributed Crossbar, Hidden Precharge Pipeline and Dynamic CMOS Logic
Koh Johguchi, Zhaomin Zhu, Ken-ichi Aoyama, Yuya Mukuda, Hans Juergen Mattausch, Testushi Koide, Tetsuo Hironaka

P-17 Time-Domain-Based Modeling of Carrier Transport in Lateral p-i-n Photodiode
G. Suzuki, K. Konno, D. Navarro, N. Sadachika Y. Mizukane, O. Matsushima, T. Ezaki, Mitiko Miura-Mattausch, and S. Yokoyama

P-18 Shot Noise Modeling in MOSFETs under Sub-threshold Condition
Y. Isobe, D.Navarro, Y. Takeda, K. Hara, T. Ezaki and M. Miura-Mattausch

P-19 Wireless interconnects for UWB signal transmission in ULSI s Interconnection
T. Kikkawa

P-20 The Development of UWB Gaussian Monocycle Pulse Synchronization Circuit based on 0.18μm CMOS Technology
Nobuo Sasaki, Pran Kanai Saha, and Takamaro Kikkawa

P-21 Effect of Supercritical Fluid Extraction Process on Self-assembled Porous Silica Films
Kouji Isari, Nobuyuki Kawakami , Yoshito Fukumoto and Takamaro Kikkawa

P-22 Impulse-based UWB transmitter in 0.18 μm CMOS for wireless interconnect in future ULSI
P.K. Saha, N. Sasaki, and T. Kikkawa

P-23 Data Transmission Characteristics of Integrated Linear Dipole Antennas for UWB Communication in Si ULSI
K. Kimoto, N. Sasaki, M. Nitta and T. Kikkawa

P-24 Interference of Digital Noise with Integrated Dipole Antenna for Inter-chip Signal Transmission in ULSI
M. Nitta and T. Kikkawa

P-25 Front-End Technologies for nano-scale MOSFETs
Kentaro Shibahara

P-26 Workfunction Tuning of Fully-Silicided NiSi Gate with Poly-Si Predoping
Takuji Hosoi, Kousuke Sano, Masaki Hino, Norihiro Ooishi, and Kentaro Shibahara

P-27 Current Activities in Device and Process R&D of the COE
H. Sunami, S. Miyazaki, K. Shibahara, A. Nakajima, S. Yokoyama, and T. Kikkawa

P-28 Development of Three-Dimensional Beam-Channel MOS Transistors
Hideo Sunami, Kei Kobayashi, Shunpei Matsumura, Koji Yoshikawa, and Kiyoshi Okuyama

P-29 Constraint of Source/Drain Formation with Plasma Doping Applied for Beam Channel Transistor on SOI
Kei Kobayashi, Kiyoshi Okuyama, Koji Yoshikawa, and Hideo Sunami

P-30 Characterization of Newly Developed 3-D Parallel-Triple Gate MOS Transistor
Kiyoshi Okuyama, Koji Yoshikawa, and Hideo Sunami

P-31 Control of Charged States of Silicon Quantum Dots and Their Application to Floating Gate MOS Memories and Light Emitting Diodes
Seiichi Miyazaki

P-32 Impact of Rapid Thermal Annealing on ALCVD-$Al_2O_3$/$Si_3N_4$/Si(100) Stack Structures --Photoelectron Spectroscopy
H. Murakami, F. Takeno, A. Ohta, S. Higashi , S. Miyazaki, K. Komeda, M. Horikawa and K. Koyama

P-33 Formation of Si Nano-crystals by Millisecond Annealing of SiOx Films using Thermal Plasma Jet
Seiichiro Higashi, Tatsuya Okada, Noto Fujii, Naohiro Koba, Hideki Murakami and Seiichi Miyazaki

P-34 Fabrication of Multiply-Stacked Structures Consisting of Si-QDs with Ultrathin SiO2 and Its Application of Light Emitting Diodes
Katsunori Makihira, Yoshihiro Kawaguchi, Hideki Murakami, Seiichiro Higashi and Seiichi Miyazaki

P-35 Characterization of Electronic Charged States of P-doped Si Quantum Dots Using AFM/Kelvin Probe
Katsunori Makihira, Hideki Murakami, Seiichiro Higashi and Seiichi Miyazaki

P-36 Characterization of Charge Trapping and Dielectric Breakdown of $HfAlO_x$/SiON Dielectric Gate Stack
Yanli Pei, Satoru Nagamachi, Hideki Murakami, Seiichiro Higashi, Seiichi Miyazaki, Takaaki Kawahara, Kazuyoshi Torii, Yasuo Nara

P-37 Characterization of Chemical Bonding Features of $NH_3$-Annealed Hafnium Oxides Formed on Si(100)
H. Nakagawa, A. Ohta, H. Murakami, S. Higashi and S. Miyazaki

P-37 Characterization of Chemical Bonding Features of $NH_3$-Annealed Hafnium Oxides Formed on Si(100)
H. Nakagawa, A. Ohta, H. Murakami, S. Higashi and S. Miyazaki

P-38 XPS Study of Ultrathin $GeO_2$/Ge System
Akio Ohta, Hiroaki Furukawa, Hiroshi Nakagawa, Hideki Murakami, Seiichirou Higashi, Seiichi Miyazaki

P-39 Phase Transformation of Amorphous Si Films in Millisecond Time Domain Induced by Thermal Plasma Jet Irratiation
H. Kaku, S. Higashi, T. Okada, H. Murakami and S. Miyazaki

P-39 Characterization of Multi Step Electron Charging to Silicon-Quantum-Dot Floating Gate by Applying Pulsed Gate Biases
T. Nagai, M. Ikeda, Y. Shimizu, S. Higashi and S. Miyazaki

P-40 Decay Characteristics of Electronic Charged States of Si Quantum Dots as Evaluated by an AFM/Kelvin Probe Technique
Junichiro Nishitani, Katsunori Makihara, Mitsuhisa Ikeda, Hideki Murakami, Seiichiro Higashi and Seiichi Miyazaki

P-41 Analysis of Transient Temperature Profile During Thermal Plasma Jet Annealing of Si Films on Quartz Substrate
T. Okada, S. Higashi, H. Kaku, N. Koba, H. Murakami and S. Miyazaki

P-42 Status of Research on Optical Interconnection in LSI
Shin Yokoyama

P-43 Design and Simulation of Ring Resonator Optical Switches using Electro- and Magneto-Optic Materials
Yuichiro Tanushi and Shin Yokoyama

P-44 Groove-Buried Optical Waveguides Based on Metal Organic Solution-Derived $Ba_{0.7}Sr_{0.3}TiO_3$ Thin Films
Zhimou Xu, Masato Suzuki, Yuichiro Tanushi, Keita Wakushima and Shin Yokoyama

P-45 Smooth Cu Thin Film Fabricated by $H_2$ Addition Sputtering
Masahiro Ooka and Shin Yokoyama

P-46 Structural and Optical Properties of Electro-Optic Material: Sputtered (Ba,Sr)$TiO_3$
Masato Suzuki, Zhimou Xu, Yuichiro Tanushi and Shin Yokoyama

P-47 Fabrication of Spin-Coat Optical Waveguides for Optically Interconnected LSI and Influence of Fabrication Process on Lower Layer MOS Capacitors
Tetsuo Tabei, Kazuhiko Maeda, Shin Yokoyama and Hideo Sunami

P-48 Integration of High-Speed Photodetectors on Si LSI
Masayuki Kitaura, Yoshio Mizukane, Shin Yokoyama and Mitiko Miura-Mattausch

P-49 Development of Photodetectors using Si Quantum Dots
Mitsuhisa Ikeda, Masayuki Kitaura, Seiichi Miyazaki and Shin Yokoyama

P-50 Characterization and application of SiON gate dielectrics
Anri Nakajima, Shiyang Zhu, Takuo Ohashi, and Hideharu Miyake

P-51 Infuence of Bulk Bias on Negative Bias Temperature Instability of pMOSFETs with Ultrathin Plasma-Nitrided Gate Oxide
Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake

P-52 [Invited] Dynamic Behavior of Human Eye
Roland Kempf, Yuichi Kurita, Yoshichika Iida, Makoto Kaneko, Hiromu Mishima, Hidetoshi Tsukamoto, and Eiichiro Sugimoto

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## ●半導体シンポジウム　2006 年 6 月 26 日　キャンパスイノベーションセンター、東京都港区


半導体シンポジウム・パネルディスカッション

[ プログラム ]

| | | |
|---|---|---|
| 10:00-10:10 | 挨拶 | 興　直孝（広大副学長） |
| 10:10-10:40 | 広大における半導体技術の研究・教育 | 岩田　穆（広大） |
| 10:40-11:20 | ＭＯＳデバイスモデル HiSIM | 三浦道子（広大） |
| 11:20-12:00 | メモリベース情報処理システム | マタウシュ H. J.（広大） |
| | 昼食　　展示 | |
| 13:00-13:40 | 無線インタコネクトと三次元集積 | 吉川公麿（広大） |
| 13:40-14:20 | 集積化光インタケネクション | 横山　新（広大） |
| 14:20-15:00 | 量子ドット形成とデバイス応用 | 宮崎誠一（広大） |
| | 休憩　展示 | |

15:30-17:30　　パネル討論「インタコネクションと三次元集積」
パネラー：黒田忠広（慶応大）
和田一実（東大）
田中　徹（東北大）
池田博明（エルピーダメモリ）
吉川公麿（広大）
司会：岩田　穆
18:00-20:00　　懇親会

[ ポスター発表 ]

・HiSIM　（三浦　道子・江崎　達也）
・文部科学省総合ナノテク支援事業　（横山　新）
・経済産業省中核人事育成事業　（久保　征治）
・Minimum Euclidean Distance Associative Memory Architecture with xFully-Parallel Search Capability
（Abedin Md.Anwarul）
・Development of fabrication process for new triple-gate MOS transistor　（奥山　清）
・シリコン集積化アンテナを用いた CMOS UWB 受信回路の研究　（佐々木　信雄）
・Ring Resonator Optical Switches using Electro- and Magneto-Optic Materials　（田主　裕一朗）
・MonolithicMach-Zehnder Optical Modulator on Silicon using (Ba,Sr)Ti0$_3$Sputter-Deposited at 450℃
（鈴木　昌人）
・Hardware Prototyping for A Learning Model and Application in An OCR System（Ali Ahmadi）
・Workfunction Tunadle NiSi FUSI Metal Gate　（細井　卓治）
・照明変動にロバストな顔認識手法と三次元集積に向けたハードウェア実現　（安藤　博士）
・ローカルおよびグローバルワイヤレスインターコネクションを利用した三次元集積技術の脳型視覚システムへの応用　（亀田　成司）
・Interface trap and oxide charge generation under NBTI of pMOSFETs with ultrathin plasma-nitrided
・SiON gate dielectrics　（Zhu Shiyang）
・Multi-Object Tracking VLSI Architecture Using Image-Scan Based Region Growing and Feature Matching　（山岡　功佑）
・階層型多ポートメモリによるマルチプロセッサ用エンベディッドメモリの研究　（上口　光）
・Real-Time Huffman Encoder Encoder with Pipelined CAM-Based Date Path and Code-Word-Table Optimizer　（熊木　武志）

## ●第 5 回ワークショップ　　2007 年 1 月 29、30 日　キャンパスイノベーションセンター、東京都港区


第 5 回ワークショップ招待講演者および COE 教員

**MONDAY, JANUARY 29**

OPENING SESSION

9:00 Welcome Remarks

9:10 Opening Address
Taizo Muta, President, Hiroshima University

9:30 [Invited] Technology Challenges for Future CMOS
Masataka Hirose, Director, MIRAI, Advanced Semiconductor Research Center, Advanced Industrial Science and Technology

10:15 Break

10:30 Summary of the 21st Century COE Program on Nanoelectronics for Tera-Bit Information Processing
Atsushi Iwata, COE Leader, Hiroshima University

11:15 [Invited] Trends and Requirements of Future FETs Based on a Simple Physical Device Model
Dimitri A. Antoniadis and Ali Khakifirooz, Massachusetts Institute of Technology

12:00 Lunch Break

SYSTEM & DEVICE SESSION 13:30 – 17:15

13:30 [Invited] Reconfigurable Parallel Image Processing System Using Three-Dimensional LSI
Mitsumasa Koyanagi, Takeaki Sugimura, and Tetsu Tanaka, Tohoku University

14:15 Inductor based Circuit Techniques for Chip-to-Chip Interconnect and Standing Wave Clock Generation
Mamoru Sasaki, Bin Yan, Daisuke Arizono, Mitsuru Shiozaki, Atsushi Mori, and Atsushi Iwata, Graduate School of Advanced Sciences of the Matter, Hiroshima University

14:45 Low-Noise and Low-Voltage Circuit Techniques for CMOS Analog Design
Takeshi Yoshida, Yoshihiro Masui, Mamoru Sasaki, and Atsushi Iwata, Graduate School of Advanced Sciences of the Matter, Hiroshima University

15:15 Break

15:30 [Invited] Nanoscale Silicon Devices Using Nanostructure Physics for VLSI Applications
Toshiro Hiramoto, Kousuke Miyaji, and Masaharu Kobayashi, The University of Tokyo

16:15 Characterization of Electronic Charged States of Si-based Quantum Dots for Multi-valued MOS Memories
Seiichi Miyazaki, Graduate School of Advanced Sciences of the Matter, Hiroshima University

16:45 Formation Techniques for Three-Dimensional MOS Beam-Channel Transistor
Hideo Sunami and Kiyoshi Okuyama, RCNS, Hiroshima University

CLOSING REMARKS 17:15 – 17:20

POSTER SESSION 17:30 – 18:30

BANQUET 18:30 – 20:00

**TUESDAY, JANUARY 30**

CIRCUITS & MODELING SESSION

9:00 Functional-Memory Architectures for Information-Processing Systems
Hans Jürgen Mattausch, Tetsushi Koide, M. Anwarul Abedin, and Koh Johguchi, RCNS, Hiroshima University

9:30 Functional-Memory-Based Systems Enabling Recognition and Learning
Tetsushi Koide, Hans Jürgen Mattausch, Ali Ahmadi, Takashi Morimoto, and Kousuke Yamaoka, RCNS, Hiroshima University

10:00 Physics-Based Photodiode Model Enabling Consistent Opto-Electronic Circuit Simulation
Mitiko Miura-Mattausch, Kohkichi Konno, Gaku Suzuki, Tatsuya Ezaki, Osamu Matsushima, Yoshio Mizukane, Dondee Navarro, Masataka Miyake, Norio Sadachika, and Hans Jürgen Mattausch, Graduate School of Advanced Sciences of the Matter, Hiroshima University

10:30 Break

10:45 A Single-chip Gaussian Monocycle Pulse Transmitter using 0.18 μm CMOS Technology for Intra/Interchip UWB Communication
Takamaro Kikkawa, Pran Kanai Saha, Nobuo Sasaki, and Kentaro Kimoto, RCNS, Hiroshima University

11:15 Optical Interconnection in Silicon LSI
Shin Yokoyama, Yuichiro Tanushi, and Masato Suzuki, RCNS, Hiroshima University

11:45 Lunch Break

DEVICE & PROCESS SESSION 13:15-15:30

13:15 Ultrarapid Thermal Annealing Induced by DC Arc Discharge Plasma Jet Irradiation
Seiichiro Higashi, Hirotaka Kaku, Tatsuya Okada, Takuya Yorimoto, Hideki Murakami, and Seiichi Miyazaki, Graduate School of Advanced Sciences of the Matter, Hiroshima University

13:45 Evaluation of Chemical Structures and Work Function of NiSi near the Interface between NiSi and $SiO_2$
Hideki Murakami, Hiromichi Yoshinaga, Daisuke Azuma, Akio Ohta, Yuuki Munetaka, Seiichiro Higashi, Seiichi Miyazaki, Takayuki Aoyama, Kimihiko Hosaka, and Kentaro Shibahara, Graduate School of Advanced Sciences of the Matter, Hiroshima University

14:15 Break

14:30 Development of Reliable High-$k$ Gate Dielectrics for Scaled MOSFETs
Anri Nakajima, Research Center for Nanodevices and Systems, Hiroshima University

15:00 Metal Gate and Junction Technologies for Leading Edge Devices
Kentaro Shibahara, Research Center for Nanodevices and Systems, Hiroshima University

CLOSING REMARKS 15:30-15:45

**[POSTER SESSION]**

P-01 An Object Detection/Recognition System using a 3-Dimensional Integration with Local and Global Wireless Interconnections
Hiroshi Ando, Seiji Kameda, Nobuo Sasaki, Daisuke Arizono, Kentaro Kimoto, Norimitsu Fuchigami, Kouta Kaya, Mamoru Sasaki, Takamaro Kikkawa, and Atsushi Iwata

P-02 A Vision System using a 3-Dimensional Integration with Local and Global Wireless Interconnections
Seiji Kameda, Nobuo Sasaki, Daisuke Arizono, Kentaro Kimoto, Masaki Odahara, Mamoru Sasaki, Takamaro Kikkawa, and Atsushi Iwata

P-03 Learning Algorithms for Robots Behaving Flexibly in Dynamic Environments
Masahiro Ono, Hiroshi Ando, Mamoru Sasaki, and Atsushi Iwata

P-04 Window-based Stereo Matching Algorithm Using a Weighted Average of Costs Aggregated with Window Size Reduction
Kan'ya Sasaki, Seiji Kameda, Hiroshi Ando, Mamoru Sasaki, and Atsushi Iwata

P-05 A 0.6 V Supply CMOS Amplifier Using Noise Reduction Techniques of Autozeroing and Chopper Stabilization
Yoshihiro Masui, Takeshi Yoshida, Mamoru Sasaki, and Atsushi Iwata

P-06 Evaluation of Digital Crosstalk Noise to Fully Differential VCO
Akihiro Toya, Yoshitaka Murasaka, Takafumi Ohmoto, and Atsushi Iwata

P-07 HiSIM-SOI: Complete Surface-Potential-Based Fully-Depleted SOI-MOSFET Model for Circuit Simulation
Norio Sadachika, Daisuke Kitamaru, Yasuhito Uetsuji, Dondee Navarro, Marmee Mohd Yusoff, Tatsuya Ezaki, Hans Jürgen Mattausch, Shunsuke Baba, and Mitiko Miura-Mattausch

P-08 Photoemission Study of $HfO_2$/Ge(100) Stacked Structures
Hiroshi Nakagawa, Akio Ohta, Hideki Murakami, Seiichiro Higashi, and Seiichi Miyazaki

P-09 Photoemission Study of Ultrathin N incorporated Hf-Silicates on Si(100) Systems
Akio Ohta, Hiroshi Nakagawa, Hideki Murakami, Seiichirou Higashi, Seiichi Miyazaki, Seiji Ie Inumiya, and Yasuo Nara

P-10 Developement of Fabrication Processes for New SOI MOS Transistor and a Silicidation Technique for Source and Drain of Vertical Channel Devices
Kiyoshi Okuyama, Koji Yoshikawa, Shunpei Matsumura, Atsushi Sugimura, and Hideo Sunami

P-11 A Human-memory Based Learning Model and Hardware Prototyping in FPGA
Ali Ahmadi, M. Anwarul Abedin, Hans Jürgen Mattausch, Tetsushi Koide, Yoshinori Shirakawa, and M. Arifin Ritonga

P-12 Application of Fully Parallel Associative Memory in Two-stage Pattern Matching
M. Anwarul Abedin, Ali Ahmadi, Yuuki Tanaka, Shogo Sakakibara, Tetsushi Koide, and Hans Jürgen Mattausch

P-13 Highly-Parallel Table-Lookup-Coding with Scalable Architecture using Flexible Multi-Ported Content Addressable Memory
Takeshi Kumaki, Yutaka Kono, Masakatsu Ishizaki, Tetsushi Koide, and Hans Jürgen Mattausch

P-14 Multi-Bank Register File for Increased Performance of Highly-Parallel Processors
Koh Johguchi, Ken-ichi Aoyama, Tetsuya Sueyoshi, Moto Maeda, Hans Jürgen Mattausch, Tetsushi Koide, Tetsuo Hironaka, and Kazuya Tanigawa

P-15 FPGA Implementation of Object-Based Real-Time Object Tracking Architecture
Kousuke Yamaoka, Takashi Morimoto, Hidekazu Adachi, Kazutoshi Awane, Tetsushi Koide, and Hans Jürgen Mattausch

P-16 A Single-chip Ultra-Wideband Receiver using Silicon Integrated Antennas for Inter-chip Wireless Interconnection
Nobuo Sasaki, Masashi Fukuda, Masakazu Nitta, Kentaro Kimoto, and Takamaro Kikkawa

P-17 On-Chip Wireless Signal Transmission using Si Integrated Antennas
Kentaro Kimoto, Masakazu Nitta, Nobuo Sasaki, and Takamaro Kikkawa

P-18 Workfunction Tuning of NiSi and $Pd_2Si$ Fully-Silicided Gates by Predoping
Takuji Hosoi, Kosuke Sano, Masaki Hino, and Kentaro Shibahara

P-19 Ring Resonator Optical Switches for Interconnection on Si Chips
Yuichiro Tanushi and Shin Yokoyama

P-20 Monolithic Mach-Zehnder Optical Modulator Using Electro-Optic Material: $(Ba,Sr)TiO_3$ Film Sputter Deposited at Low Temperature on Silicon
Masato Suzuki, Yuichiro Tanushi, Kazuma Nagata, and Shin Yokoyama

P-21 Atomic-Layer-Deposition of $HfO_2$ on Si and Ge Substrates from Hafnium Tetrakis(ethylmethyl-amino) and Water
Shiyang Zhu and Anri Nakajima