NTIP

Hiroshima University

21st Century COE, Nanoelectronics for Tera-bit Information Processing

The Fourth Hiroshima International Workshop on Nanoelectronics for Tera-bit Information Processing

– Ultra Small Device and Process Technology –

Date: September 16 (Friday), 2005
Place: Faculty Club, Hiroshima University

Program

9:00-9:10	Welcome Remarks
9:10-9:30	Opening Address Taizo Muta, President, Hiroshima University
9:30-9:50	Recent Progress of the COE Atsushi Iwata, Hiroshima University
9:50-10:30	[Invited] Tadahiro Kuroda, Keio University "System LSI: Challenges and Opportunities"
10:30-11:10	[Invited] T. P. Ma, Yale University "High-k Gate Dielectrics for Future CMOS Technology"
11:10-11:50	[Invited] J.C.S. Woo, UCLA "Sub-20 nm Novel Silicon-Based Transistors"
11:50-13:10	Lunch Break
13:10-13:50	[Invited] S. Biesemans, IMEC "Perspective on Emerging Devices and their Impact on Scaling Technologies"
13:50-14:30	[Invited] Y. J. Park, Seoul National University "Device Simulation for Nano MOSFET and Scaling Issues"
14:30-15:10	[Invited] F. Boeuf, ST Microelectronics "Conventional Bulk and Bulk+ Architectures for 45 nm Node"
15:10-15:20	Break
15:20-16:00	[Invited] Masaaki Niwa, Matsushita Electric "Current Status of PVD Hf-Based High-k Gate Stack-Process Improvement on Drive Current"
16:00-16:40	Hideo Sunami *et al.*, Hiroshima University "Current Activities in Device and Process R & D of the COE"
16:40-18:00	POSTER SESSION
18:00	BANQUET

Research Center for Nanodevices and Systems, Hiroshima University
Super Clean Room (0.1 μm, Class 10)

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