Si Microphotonics
-Photons meet LSIs-

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In the past three decades, the performance of integrated circuits has depended primarily on device properties. To enhance the circuit and system speed, the major effort has focused on improving the device speed through scaling of device dimensions. The decrease in minimum feature size of devices has led to a proportional decrease in interconnect cross sectional area and pitch. The parasitic resistance, capacitance and inductance associated with interconnections are beginning to influence the circuit performance and have increasingly become one of the primary show stoppers in the evolution of deep submicron ULSI technology. With a shrinkage of the design rule the switching delay of a transistor decreases, while the propagation delay between transistors increases.

To realize optical interconnection, the first step is to establish optical clock distribution. We have to device the three fundamental elements being used in fiber communication: a light source, waveguides and detectors. The long interconnection path should be replaced by these optical components while the short path remains the electronics. At present, an off-chip light source is advantageous to avoid so called "heat penalty". The size-limiting component is waveguide bends. High-index contrast materials systems such as Si/SiO_2, and Si_3N_4/SiO_2 are advantageous over the systems with low-index contrast called Silica Optical Bench. Another important progress on the right angle bends is "High Transmission Cavity, HTC". The two-dimensional FDTD simulation achieves nearly 100% transmission under a proper design. It is prototyped and shows the bend area is as small as 0.5 μm^2 and the loss was 0.32 dB/turn. 0.1 dB/turn should be achievable.

The device building block of optical clock distribution is photodetectors. We have established Ge hetero-epitaxy directly on Si. Two-step growth and successive cyclic annealing dramatically improves Ge quality and the discrete photodetector showed high internal quantum efficiency and 6 GHz operation. Tensile strain induced in Ge layers enhances detector characteristics in terms of the light hole valence band top. It is shown that our Ge photodetectors are nearly equivalent to InGaAs photodetectors in characteristics.

On-chip WDM is an attractive concept since signal messenger with various wavelength, i.e., color, helps one waveguide being used to exchange signals without interference. This will reduce the interconnect layer levels in Si-LSIs. The device for WDM is multiplexer/demultiplexer (MUX/DEMUX) in addition to the optical clock distribution. 1x4 DEMUX has been built based on microring resonators and the cascade rings demonstrate its potential for Dense WDM interconnection.

Si-LSIs can be faster as predicted by the Moore's law when photons are used as the signal messengers in the long distance interconnects.

Nanoelectronics for Terra-Bit Information Processing
3/17/03

Si Microphotonics
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- Electronic Photonic Convergence

Outline

- Silicon CMOS platform for monolithic integration of electronics and photonics
- Current status of optical interconnections: Optical clock distribution and on-chip wavelength division multiplexing
- Conclusion

Monolithic Integration of Electronics and Photonics

Undeveloped
Lab
Commercial

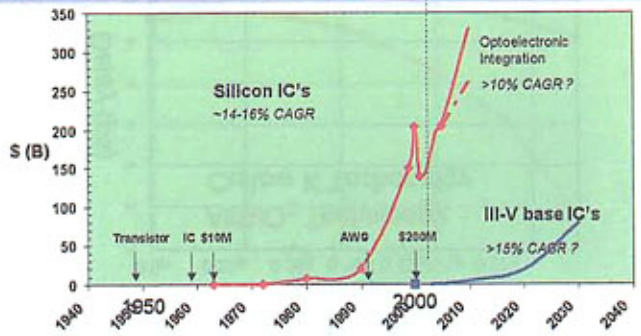
Si CMOS Platform

PASSIVE DEVICES	ACTIVE DEVICES	ELECTRONICS
Ring resonators	Diode laser	Memory
Isolator/Circulator	OAs	Flip-flops/MUX
Coupler	Modulators	TIAs
	Photodetectors	Bias circuitry

III-V based Platform

PASSIVE DEVICES	ACTIVE DEVICES	ELECTRONICS
AWGs	Diode laser	Memory
Isolator/Circulator	SOAs	Flip-flops/MUX
Coupler	Modulators	TIAs
	Photodetectors	Bias circuitry

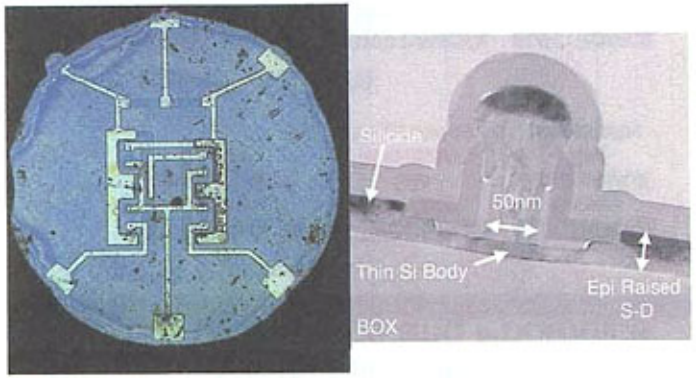
Silicon for Photonics



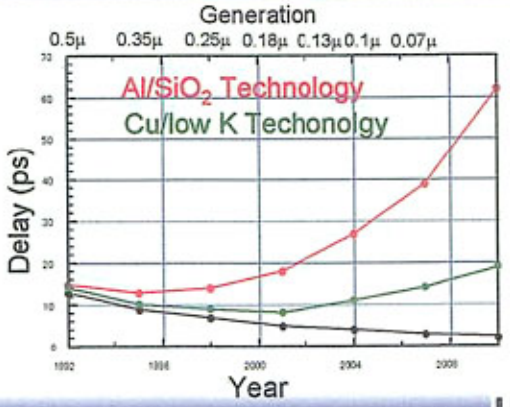
Electronic-Photonic convergence: extending IC's or a new platform?

Sources:Silicon IC's to 2005 - WSTS,
OEIC's 2000 - RHK,

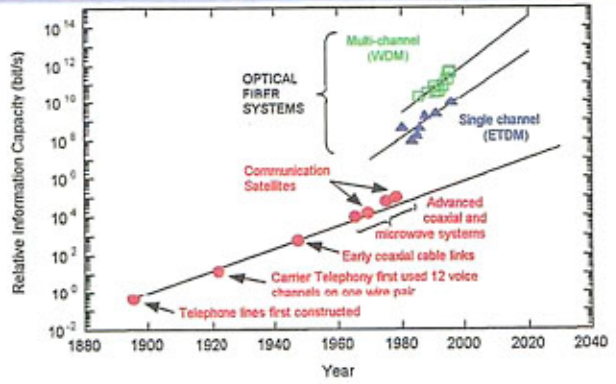
First ICs with Current Technology



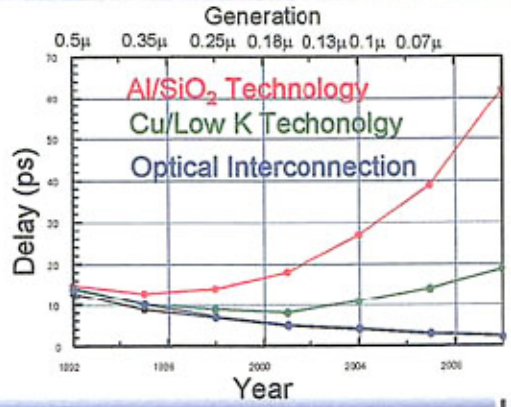
Interconnection Beyond Cu-low k technology



Information Capacity Evolution



Technology Roadmap Beyond Cu/low K



Fundamental Limits in Metal Interconnection

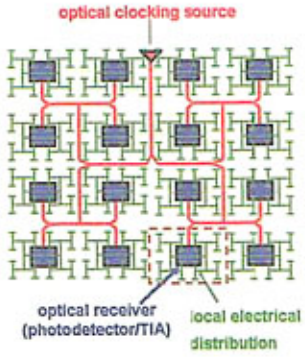
	1999	2006
Interconnect Length	1.5 km/chip	10 km/chip
• Clock Frequency	1 GHz	6 GHz
• Levels of Metal	6 layers	8 layers
• Power/Chip	90 W	170 W

Semiconductor Industry Association Roadmap

Optical Interconnection on Si-LSI Chips

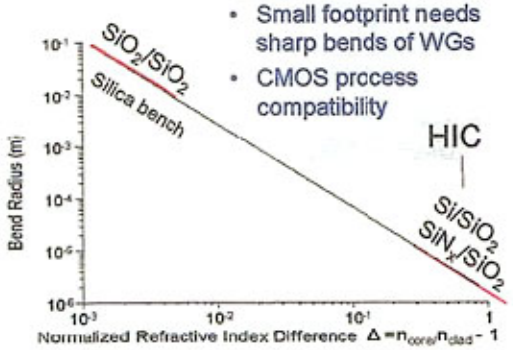
- Optical clock: long distance
- Electric clock: short distance

Key issues
- Small bending radius
- Equal power distribution
- Efficient coupling of light (source/waveguide & waveguide/detector)
- High detector responsivity and fast rise time



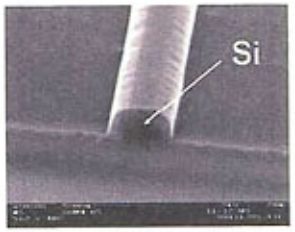
High-index Contrast (HIC) Platform

- Small footprint needs sharp bends of WGs
- CMOS process compatibility



HIC (Si/SiO_2) Waveguides

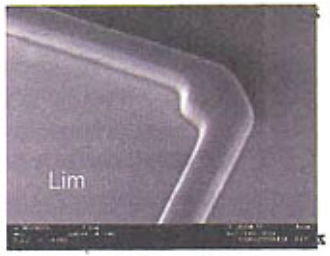
- Si waveguide on SOI substrate.
- Si core and SiO_2 (or air) cladding.
- Core size 0.2 x 0.5 μm^2.



Fabricated at MIT Lincoln Labs

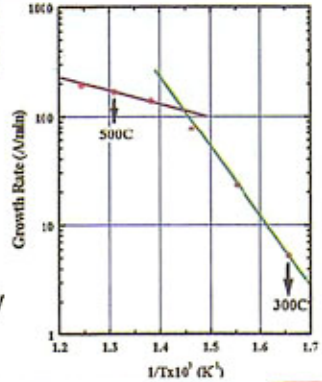
High Transmission Cavity Bends

- HTC (High Transmission Cavity) for right angle bends -- 2D simulation
- Design simplicity
  - T- splitter, crossing
- Process flexibility
  - <110> facets
- Size: 0.5 μm^2
- SOI structure
- Bending Loss: 0.32 dB/turn
- Core: 0.5 x 0.2 μm^2



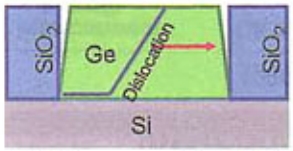
Flat Ge Epitaxy on Si

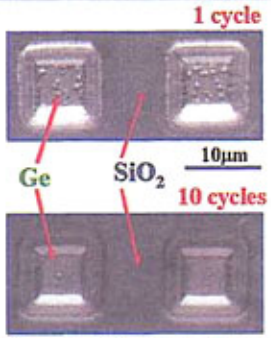
Deposit flat Ge epilayer directly on Si by a two-step CVD process.



Ge Photodetectors

- Ge growth on Si without SiGe buffer
- Dislocation glide by thermal stress





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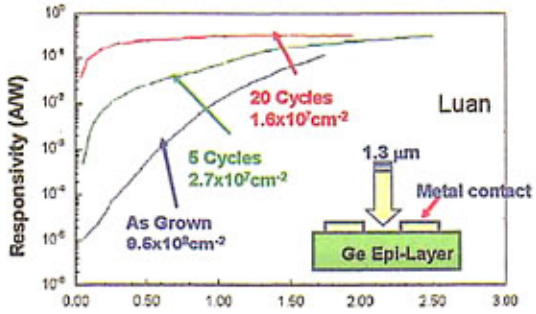
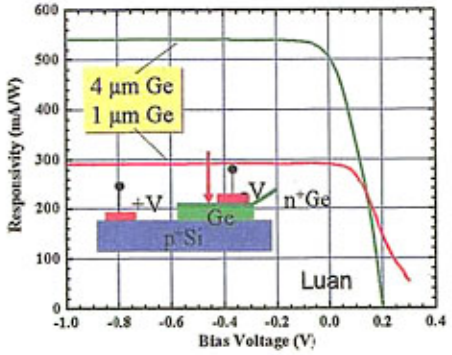
Threading Dislocation-free Ge on Si

MSM Photodetector Performance

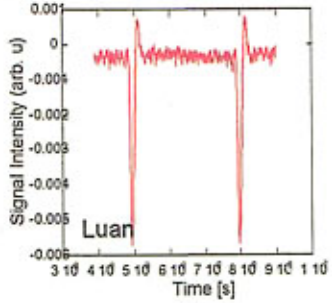


PIN Ge Photodetectors: Responsivity

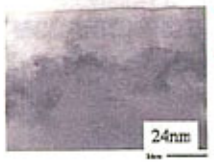


Speed

- RC delay dominant
  - 6GHz at 80 μm mesa



Ge Surface Passivation

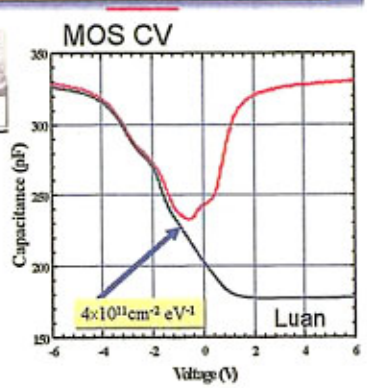


SiO_2

Si

Ge

Thermal oxide



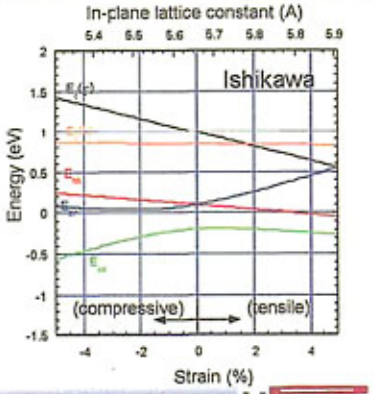
Growth Cooling and Strain

- Thermal expansion coefficient: Ge > Si
- Bi-metal effect introduces tensile strain.
  - 0.2% tensile strain.
- Stress-induced bandgap shrinkage.

Ishikawa

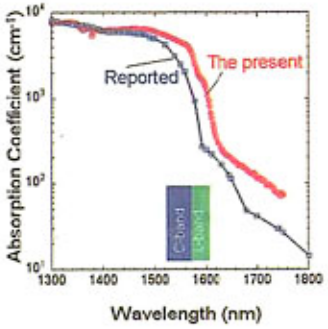
Stress v.s. Bandgap

- Tensile stress accumulation during cooling.
- Bandgap shrinkage
  - Shifts in light hole band and Γ valley.



Absorption Coefficient of Ge

- Shift of the absorption edge to longer wavelength.
- Beneficial for detection of L-band as well as C-band.
- Stress-induced bandgap shrinkage.



Challenges in Optical Interconnection

- High Speed Operation
  - Optical clock distribution
  - Monolithic Integration
  - Avoid power penalty
    - Off-chip light source
- Next: High Density Interconnects
  - WDM (Wavelength Division Multiplexing)

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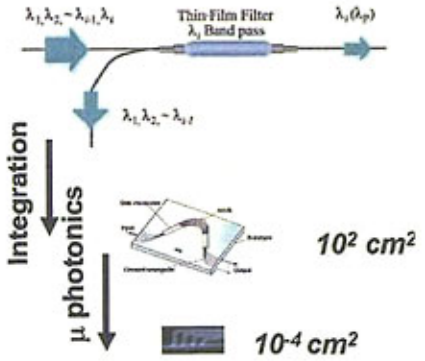
On-chip WDM

Color

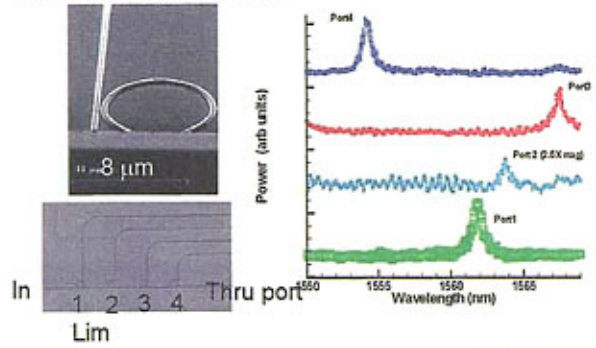
- Multi-wavelengths potentially eliminate multi-layer interconnects to open ultrahigh density interconnection.
- Challenge: Multiplexer (MUX) and DEMUX besides H-tree on a chip.

Technology Evolution for WDM



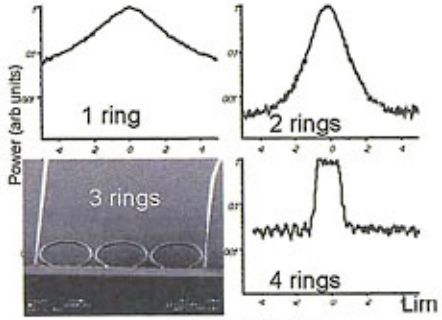
World's Smallest MUX/DEMUX

1x4 WDM in Silicon

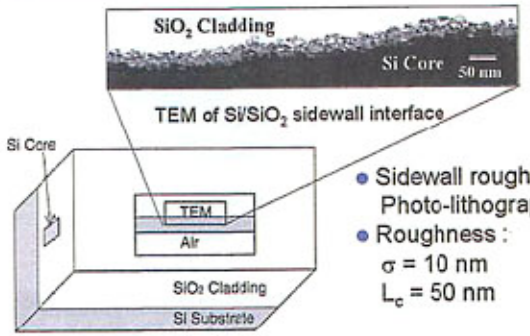


Coupled Microring Resonators

- Flat top and narrow channel MUX/DEMUX.



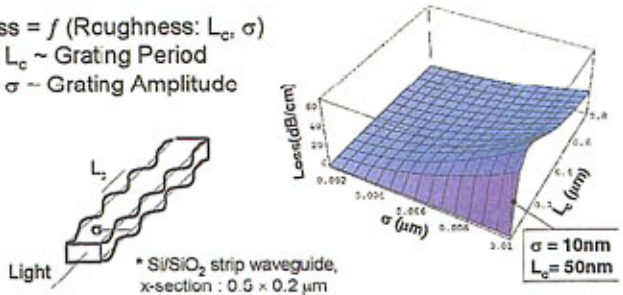
Challenges for Low Loss



- Sidewall roughness from: Photo-lithography & RIE
- Roughness :
  σ = 10 nm
  L_c = 50 nm

Waveguide Loss v.s. Roughness

- Scattering loss theory due to grating
- Loss = f (Roughness: L_c, σ)
  - L_c ~ Grating Period
  - σ ~ Grating Amplitude



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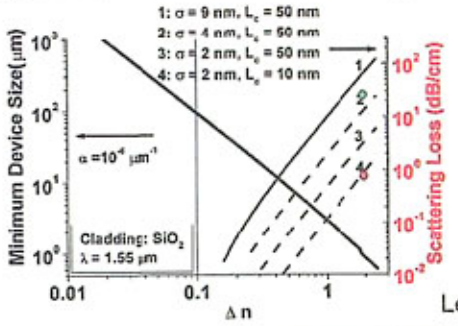
Bend Radii vs. Index Difference

High Δn induces loss via wall roughness.



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Electronic/Photonic Convergence in Silicon

a possible roadmap template

	1990	2000	2010	2020	2030
PHOTONICS					
Component	Fiber, lasers, detectors	MUX, EDFA	Metro-fiber, PLC	Mph ICs, FTTH	Pervasive, Mph ICs
Network fn	ETDM	DWDM	B-PON, Gb/s Ethernet	1Gb/saccess 10Tb/s WAN	Fiber circuit architecture
Network target	WAN	WAN	METRO, LAN	ACCESS	
Interconnect Hierarchy	Fiber	Fiber pigtail	Optical MCM, Circuit Boards		
ELECTRONICS					
Technology	IC: Al/SiO_2	IC: Cu/SiO_2	O-MCM,SiOB	On-chip optical interconnects	Optical signal processing
Function	DRAM, SRAM, mProc	DSP mProc	LS parallel processing		
Constraint	Yield	Shrink	Optical interconnects	Photonic design	Photonic logic

timeline for pervasive deployment

Summary

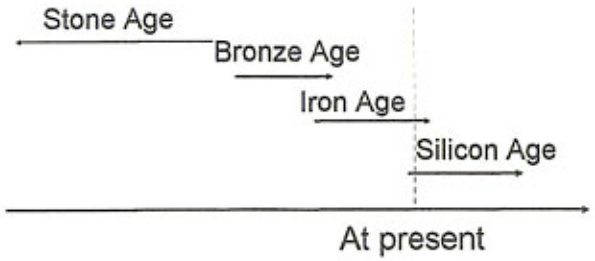
- Photons need to meet LSIs.
  - Speed: Optical clock distribution for high speed MPU.
  - Color: WDM for high density of interconnects.
- *Compact* and *monolithic* WGs, T-splitters, Ge PDs, MUX/DEMUX proto-typed.
  - High-index contrast (HIC) optics is a unique solution.

Summary (continued)

Current status of optical interconnetion:

- Designs
  - HTC for H-tree and Waveguides
  - High Q MUX/DEMUX by micro-ring resonators
- Materials: CMOS compatibility
  - High Δn (Si/SiO_2) or Medium Δn (Si_3N_4/SiO_2)
  - Ge photodetectors for C+L band detection
- Processes
  - Ultrafine lithgraphy, roughness minimization, thermal budget.

Age



A few **MILLENIA** left for Silicon Age