3-dimensional global/local wireless interconnection for hierarchical processing systems

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One of the project's aims is implementation of brain type processor with high-level recognition capability. Such system has hierarchical structures and global/local connections, and the structure realizes massive parallel processing and high fault-tolerance. For example, Figure 1 shows a diagram of prediction and planning base robot brain. The system predicts a surrounding motion and/or environmental change, and elaborates an action strategy from the information of visions and/or sensors. Learning scheme for acquisition of strategy model is embedded into the system. In addition, the system requires vision processing with high flexibility and high reliability. Figure 2 shows the vision system for an autonomous robot. It detects object position and moving objects, based on stereo matching and optical flow calculation. The system can evaluate and compensate the scene fluctuation caused by movement and can acquire the correct vision information to control the next movement.

In order to implement such system, many chips fabricated by various technologies are merged, e.g. imagers, analog circuits for preprocessing the sensor signal, massive memory systems, power circuit for actuators, etc. In the system, high-speed and high-density I/O's are becoming important to fill an increasing gap between the communication bandwidth inside a VLSI and the bandwidth among chips. To overcome the I/O bottleneck, we propose 3-Dimensional Custom-Stack System (3DCSS). Figure 3 shows a concept of the 3-Dimensional Custom-Stack System. It has the following features. (1) 3-dimensional integration. (2) Integration of multiple chips fabricated by various technologies. (3) Custom stack and reconfigurable inter-connection. First feature becomes a breakthrough against the limitation of system integration. Second feature realizes massive learning and recognition system with many sensors such as the above mentioned brain type processor. Final feature brings the high flexibility to system configuration.

As shown in Figure 3, two types of wireless connection are prepared for the data communication. One is global connection, which communicates beyond neighboring chips using microwave. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. The global connection is useful for broadcasting, global control, etc. On the other hand, the local connection can handle huge data volumes due to the massive parallel structure, and it is useful for communication of 2D vision information. For providing power supply, metal connection using embedded bumps is prepared. The conventional 3-dimensional stack is also shown in Figure 3. It has the following drawbacks. (1) Less flexibility of system configuration. (2) Increase of thermal resistance. (3) Via through substrate. (4) Precise adjustment of chip positions. (5) High cost for mounting. The proposed stack structure overcomes the drawbacks. Indeed, it has the following advantages. (1) High flexibility due to no physical connections. (2) Decrease of thermal resistance due to existence of gap between chips. (3) No via through substrate. (4) Rough positioning. (5) Low cost for mounting.

Figure 4 shows a sketch of the global connection. Microwave communication realizes the connection beyond neighboring chips, utilizing the integrated dipole antennas on silicon chips. The bandwidth is 10GHz – 20GHz, and the length of the antenna becomes 4mm on silicon chip, although the length becomes 15mm in air.

Figure 5 shows a sketch of local connection. Inductive coupling on spiral line pair realizes the local connection. Although the gap between the chips suppresses the increase of thermal resistance, it unfortunately reduces the coupling strength. The drawback is overcome by resonating the spiral inductor with parasitic capacitor. It enhances the coupling strength on the resonant frequency. Furthermore, it is expected to suppress cross talk by varying resonant frequencies in the neighboring pairs.

The ITRS roadmap predicts that VLSI pin count will exceed 7000 in the future. Thus, low-power and small size are essential for the transmitter (TX) and the receiver (RX) for both global and local connections. The transceiver based on traditional super-heterodyne architecture has issues to overcome to be a realistic solution for 3DCSS. Therefore, it is very important to develop new communication system suitable for the wireless communication between chips. Although ultra wideband (UWB) is one of candidates, the bandwidth is too spread to utilize the integrated dipole antenna and the resonant coupling. We will develop a novel communication scheme for 3DCSS during the project. The features to be target are as follows. (1) Wireless communication without carrier like UWB. (2) Moderate bandwidth in comparison with UWB. (3) Multi-channel communication using CDMA. First feature makes hardware configuration very simple. Indeed, it requires neither mixer nor PLL for channel selection. Second feature makes it possible to utilize the integrated dipole antenna and the resonant coupling. Final feature realizes multi-channel communication and dynamic reconfigurability on the wireless connections.

In the next decade, analog-RF mixed System-on-a-Chips will be developed as key devices utilizing scaled-down CMOS devices which operate at a low operation voltage and low-power dissipation. Design for these LSIs have to solve many problems. Especially substrate cross talk or coupling noise between digital and analog circuits through a chip substrate is most difficult. Of course, the design of the TX and RX for 3DCSS has same difficulty. Figure 6 shows the developed system level simulation model for substrate noise analysis[1]. It includes (1) logic noise generation and injection models as elements, (2) chip-level substrate modeling using F-matrix computation, (3) wire inductance, resistance, capacitance and mutual inductance caused by packaging and PCB assembly.

The high-speed communication systems require high-performance voltage-controlled oscillators (VCOs) suppressed to very low phase noise. A circuit design technique for VCOs has been presented in Reference [2].

It reduces the phase noise by optimizing the operating point. A 10GHz VCO has been designed and fabricated by using silicon bipolar technology with f_T=45GHz. As a result, the phase noise at 100kHz offset from center frequency was -80dBc/Hz. The technique is useful for designing VCOs in the TX and the RX for 3DCSS. Although the TX and RX for 3DCSS require no PLL for channel selection, it requires simple PLL without fractional divider for bit synchronization.

In the project, we will develop and evaluate a prototype of the 3DCSS in order to confirm the high-performance. In the development of the prototype, the TX and the RX will be designed using the new RF device models developed in the modeling group. Furthermore, the antenna and spiral line pair will be integrated with the circuit on same silicon chip and the chips will be assembled so that the 3DCSS is formed. In the design, a key process is 3-dimensional electromagnetic analysis of the dipole antenna on silicon and spiral line pair. In addition, antenna and front-end co-design is necessary.

References

[1] A. Iwata, SASIM 2003 (will be published).
[2] T. Maeda et al., SSDM, pp. 370-371, (2002).

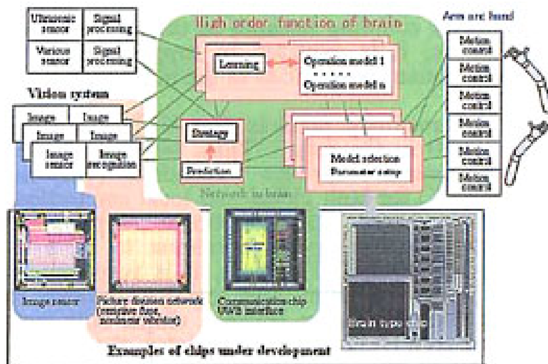


Figure 1 A prediction and planning base robot brain.

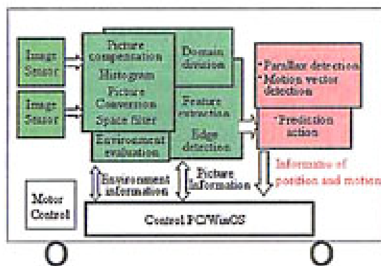


Figure 2 A vision system.

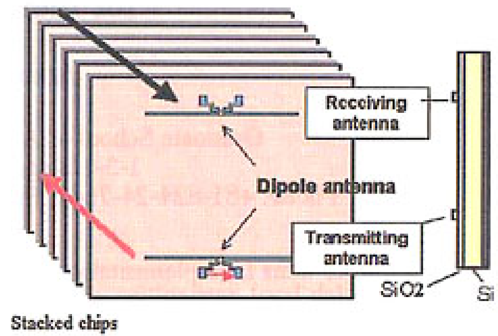


Figure 4 Global connection.

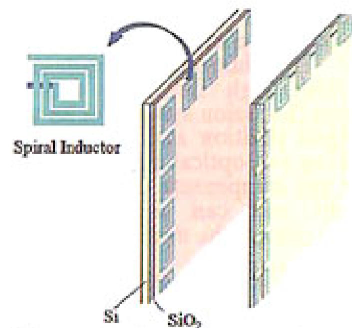


Figure 5 Local connection.

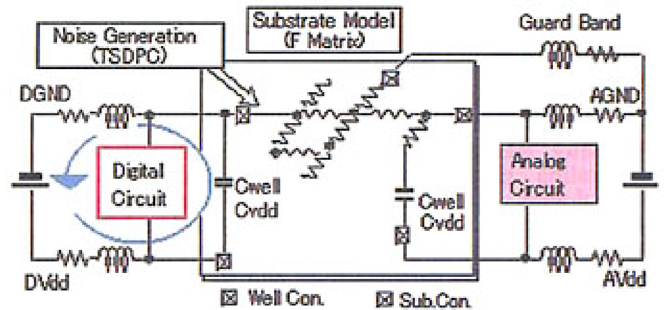
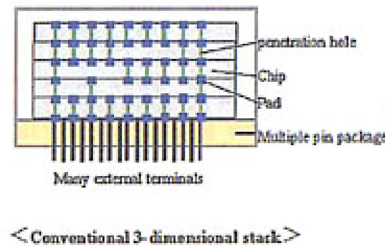


Figure 6 System level simulation model for substrate noise.



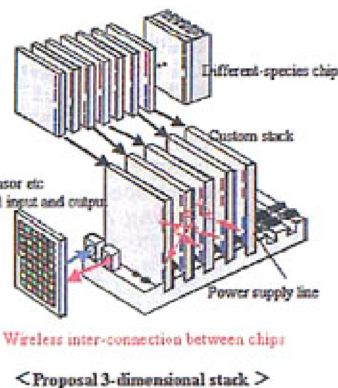


Figure 3 3-Dimensional Custom-Stack System.

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Brain type processor

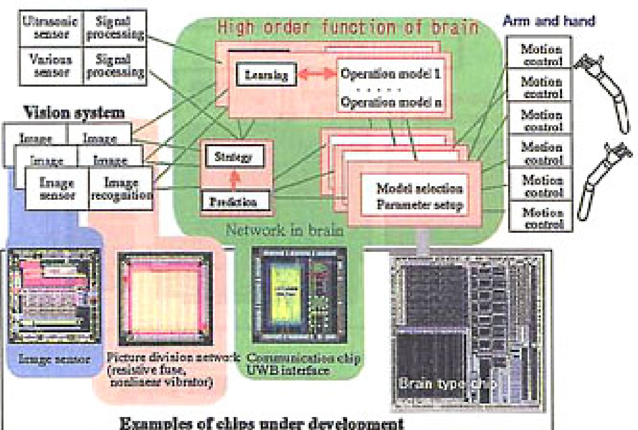
- High-level recognition capability
- **Hierarchical structures with global/local connections**
- Massive parallel processing
- High fault-tolerance

For example,

Prediction and planning base robot brain

- It predicts a surrounding motion and/or environmental change.
- It elaborates an action strategy from the information of visions and/or sensors.
- Learning scheme for acquisition of strategy model is embedded into the system.

Prediction and planning base robot brain



Examples of chips under development

Vision processing system

- High flexibility and high reliability

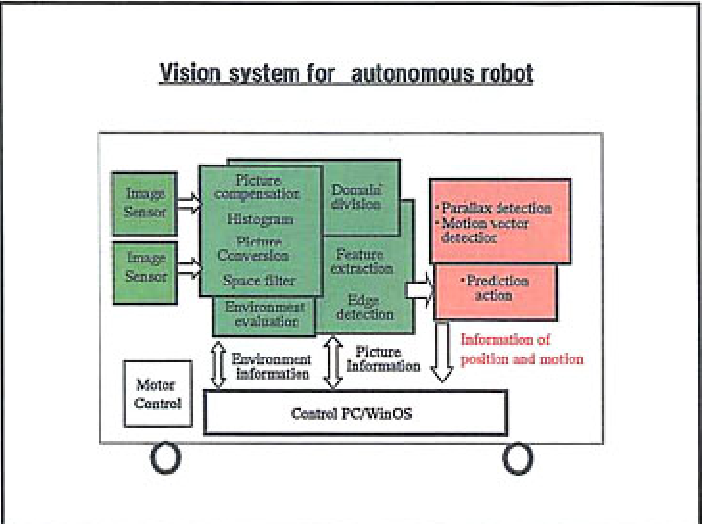
For example,

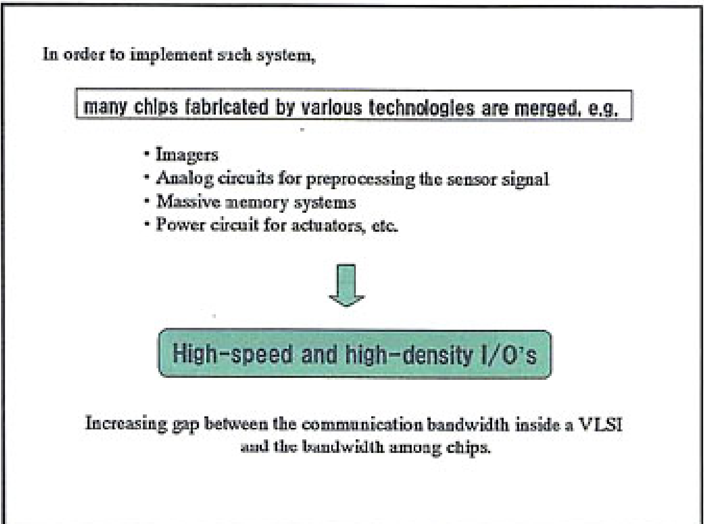
Vision system for autonomous robot

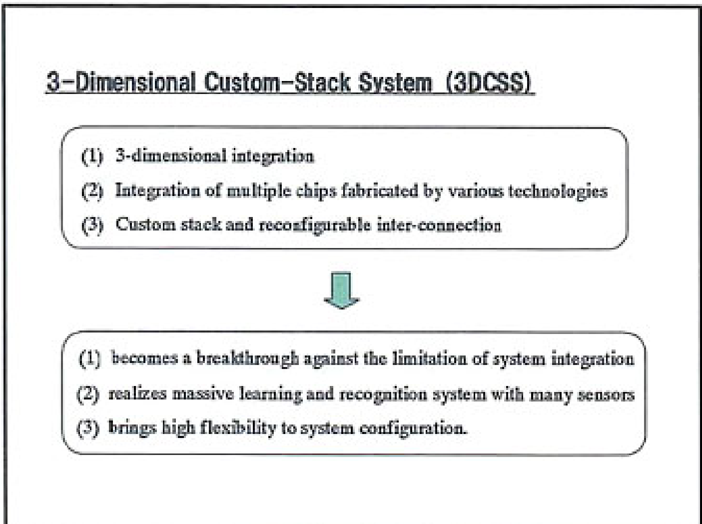
- It detects object position and moving objects,

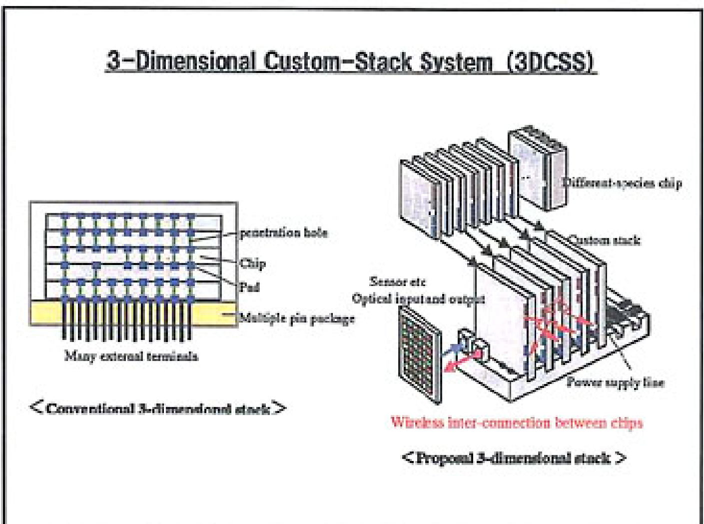
  based on
  - stereo matching
  - optical flow calculation.

- It evaluates and compensates the scene fluctuation caused by movement.
- It acquires the correct vision information to control the next movement.


Vision system for autonomous robot
Image Sensor
Image Sensor
Picture compensation
Histogram
Picture Conversion
Space filter
Environment evaluation
Domain division
Feature extraction
Edge detection
・Parallax detection
・Motion vector detection
・Prediction action
Environment information
Picture information
Information of position and motion
Motor Control
Control PC/WinOS


In order to implement such system,
many chips fabricated by various technologies are merged, e.g.
・Imagers
・Analog circuits for preprocessing the sensor signal
・Massive memory systems
・Power circuit for actuators, etc.
High-speed and high-density I/O's
Increasing gap between the communication bandwidth inside a VLSI and the bandwidth among chips.


3-Dimensional Custom-Stack System (3DCSS)
(1) 3-dimensional integration
(2) Integration of multiple chips fabricated by various technologies
(3) Custom stack and reconfigurable inter-connection
(1) becomes a breakthrough against the limitation of system integration
(2) realizes massive learning and recognition system with many sensors
(3) brings high flexibility to system configuration.


3-Dimensional Custom-Stack System (3DCSS)
penetration hole
Chip
Pad
Multiple pin package
Many external terminals
<Conventional 3-dimensional stack>
Different-species chip
Custom stack
Sensor etc
Optical input and output
Power supply line
Wireless inter-connection between chips
<Proposal 3-dimensional stack>

Conventional 3-dimensional stack

(1) Less flexibility of system configuration.
(2) Increase of thermal resistance.
(3) Via through substrate.
(4) Precise adjustment of chip positions.
(5) High cost for mounting.

Proposed stack structure

(1) High flexibility due to no physical connections.
(2) Decrease of thermal resistance due to existence of gap between chips.
(3) No via through substrate.
(4) Rough positioning.
(5) Low cost for mounting.

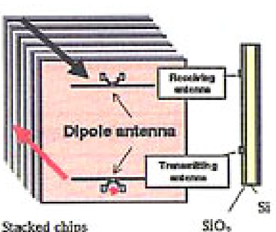
Global connection

- It communicates beyond neighboring chips using microwave.
- It is useful for broadcasting, global control, etc.
- It utilizes the integrated dipole antennas on silicon chips.

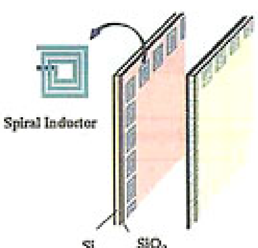
Local connection

- It is massively parallel pass between two chips placed in face-to-face.
- It can handle huge data volumes due to the massive parallel structure.
- It is useful for communication of 2D vision information.
- It utilizes inductive coupling on spiral line pair.
- It resonates the spiral inductor with parasitic capacitor to enhances the coupling strength.

Global connection



Local connection



VLSI pin count will exceed 7000 ⇨ **low-power and small size**

× super-heterodyne (large power consumption, large size)
× UWB (the bandwidth is too spread)

New communication system

(1) Wireless communication without carrier like UWB
→ very simple hardware configuration (no mixer, no PLL)

(2) Moderate bandwidth in comparison with UWB
→ utilization of integrated dipole antenna and resonant coupling

(3) Multi-channel communication using CDMA
→ dynamic reconfigurability

Analog-RF mixed system-on-chip
- sealed-down CMOS devices
- low operation voltage
- low-power dissipation.

Key devices

Problem : Substrate coupling noise between digital and analog circuits

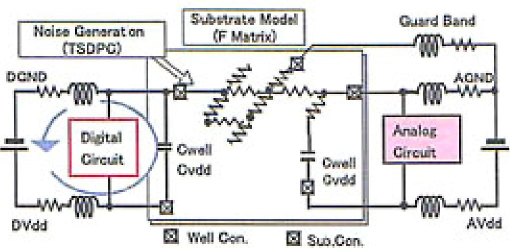
System level simulation model

(1) Logic noise generation and injection models

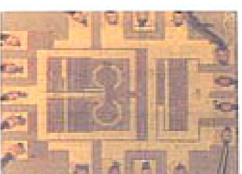
(2) Chip-level substrate modeling using F-matrix computation

(3) Wire inductance, resistance, capacitance and mutual inductance caused by packaging and PCB assembly.

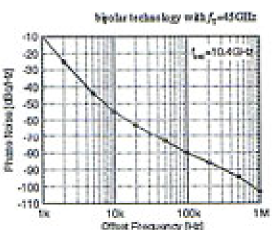
System level simulation model



High-performance VCO



Micrograph of the VCO test chip



Measured phase noise of the AC-coupled VCO
(Phase noise at 100kHz offset was -80dBc/Hz)

The technique is useful for simple PLL without fractional divider for bit synchronization in 3DCSS

3DCSS prototype development

(1) TX and RX will be designed using the new RF device models developed in the modeling group.

(2) Antenna and spiral line pair will be integated with the circuit on same silicon chip.

(3) Chips will be assembled so that the 3DCSS is formed.

key :
- **3-dimensional electromagnetic analysis of dipole antenna on silicon and spiral line pair**
- **Antenna and front-end co-design**