Digital-CMOS-Based Real-Time Color-Motion Picture Segmentation

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1. Introduction

Image segmentation is the process by which the original natural image is partitioned into meaningful regions and is an important initial task for higher-level image processing such as object recognition or object tracking. Several image segmentation algorithms have been proposed [1,2]. However, due to their complexity, compact digital VLSI implementation is impossible. For previously proposed analog VLSI approaches [3,4] the scalability to future sub-100nm, low-voltage CMOS technologies is questionable. In this paper, we present a low-complexity digital algorithm, offering high-density VLSI-implementation, comparable for gray-scale and color motion-picture segmentation.

2. Color Motion-Picture Segmentation Architecture

The proposed segmentation algorithm [5] uses a region-growing approach, which can be viewed as a simplified digital version of a locally-excitatory globally-inhibitory oscillator network (LEGION) [6]. Color and gray-scale picture segmentation differ only in the expressions for the connection-weight calculation between the network cells. The proposed VLSI-implementation architecture [7, 8] (Fig. 1) consists of 4 functional stages for connection-weight calculation, leader-cell determination, image segmentation and segmentation-result restoring, respectively.

In the 1st stage the pixel data, i. e. luminance data ($I(L)_i$) for gray-scale and RGB-data ($I(R)_i$, $I(G)_i$, $I(B)_i$) for color pictures, are used to determine the connection weights W_{ij} between pixels according to the expressions proposed in [5] for picture columns in parallel. The block diagram of the 1st stage (Fig. 2, color case) shows that always 2 neighboring columns are needed for the calculation process. The calculated connection weights are transferred to the 2nd stage for determining leader pixels ($p_i=1$) and ordinary pixels ($p_i=0$). Leader pixels represent the seed pixels in the subsequent region-growing mechanism and require that the sum of the connection weights with their 8 nearest neighbors is larger than a predetermined threshold. The stages for connection-weight (W_{ij}) and leader/ordinary-pixel (p_i) calculation perform the initialization step in the algorithm and transmit W_{ij}, p_i to the cell-network of the image-segmentation stage in a column-pipelined mode.

Each cell of the 3rd stage, the image-segmentation network, represents a pixel of the original picture. In this network, which consist of active cells and connection-weight registers shown in Fig. 3, the self-excitation and excitation steps of the algorithm are carried out for all pixels of the picture in parallel. The structures of an active cell, a block of 4 connection-weight-registers and the layout-floorplan for the network are shown in Fig. 4a, 4b and 5, respectively. The active cell consists of decoder, adder/ subtractor, control unit and three 1-bit registers. Fig. 5 also displays how the connection weight registers are effectively shared among neighboring active cells. In each region-growing cycle for a segment the new cell-state is decided by the states of the neighboring cells and the connection-weight registers. The 1-bit register l_i in each active cell is used as a flag for indicating whether this cell is included in the presently grown segment or not. After the growth of a given segment is completed, the segment number is stored in the upper-left connection-weight registers of all cells belonging to this segment. The segmentation process in the cell network finishes, if new segments cannot be grown anymore, i. e. when all leader pixels have been used up. The segmentation result, i.e. pixel/segment-number pairs, is then read-out from the cell network in a column-parallel mode and transmitted to the image-segmentation memory by the final segmentation-restore stage.

3. Performance and CMOS Test-Chip Implementation

The performance of the motion-picture segmentation architecture has been evaluated by applying the software-implemented algorithm [5] to many test images. Color/gray-scale segmentation examples for the same image are shown in Fig. 6. For 300 x 300 (90,000) pixels images very short average and worst-case image-segmentation times of 60 µsec and 300 µsec, respectively, were verified even with a low clock frequency of 50MHz. This is below motion-picture-segmentation requirements by a factor 100.

The test-chip of Fig. 7 for the cell-network core was designed in 0.35µm, 3 metal CMOS technology. Decoder and adder/subtractor of the active-cells, which consume the largest area portion, and connection-weight registor blocks were designed in full-custom. All other control circuits were generated with a standard-cell library from the high-level VERILOG design. An integration density of 22.2 pixels/mm^2 was thus achieved. We have also estimated the possible pixel density for full-custom high-speed (bit-parallel active cell) and high-density (bit-serial active cell) designs in scaled-down CMOS technologies (Table.1), assuming just 3-metal layers. From this data we expect a one-chip integration of the proposed architecture for 300 x 300 pixel pictures at the 100nm technology node and for 600 x 800 pixel pictures at the 50nm technology node.

4. Conclusions

We proposed a digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network-based implementation architecture in conventional CMOS technology. Segmentation of natural gray-scale or color images requires only a small change in the preprocessing circuit for weight calculation. Practical application in fully-integrated motion-picture-segmentation chips is estimated to become possible at the 100nm-technology node.

Acknowledgment

The test-chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References

[1] L. Lucchese et al, Proc. of IEEE 10th Tyrrhenian Workshop on Digital Communication, pp. 110-119, 1998.
[2] J. C. Russ, The Image Processing Handbook, CRC PRESS, 1999.
[3] H. Ando, et al., IEICE Trans. Fundamentals, Vol. E83-A, No. 2, pp. 329-336, 2000.
[4] F. Perez, et al., International J. of Comput. Vision, Vol. 12, pp.17-42, 1994.
[5] T. Koide, et al., Proc. of International Technical Conf. on Circuits/Systs., Computers and Communications (ITC-CSCC2002), pp. 670-673, 2002.
[6] D. L.Wang, et al., Neural Computation, Vol.9, No.4, pp.805-836, 1997.
[7] T. Morimoto, et al., Extend. Abst. of the 2002 international Conf. on Solid State Devices and Materials (SSDM2002), pp. 242-243, 2002.
[8] T. Morimoto, et al., Proc. of 2002 IEEE Asia-Pacific Conf. on ASIC (AP-ASIC2002), pp. 237-240, 2002.

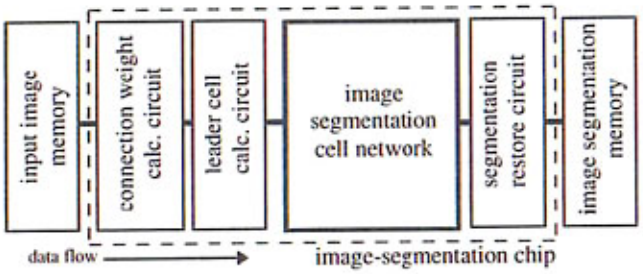


Fig. 1: Block diagram of the cell-network-based image segmentation architecture.

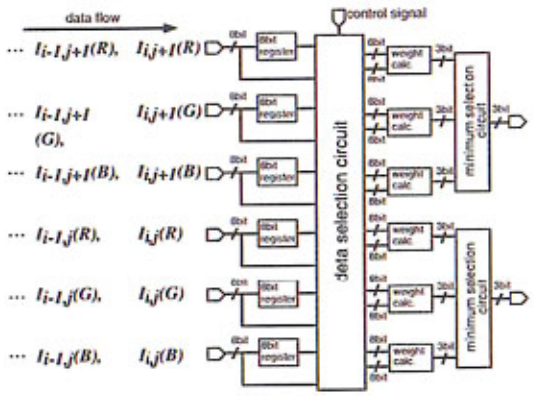


Fig.2: Structure of connection weight calculation circuit for color images.

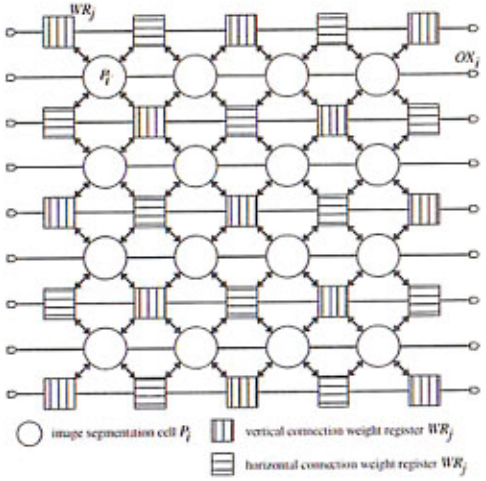
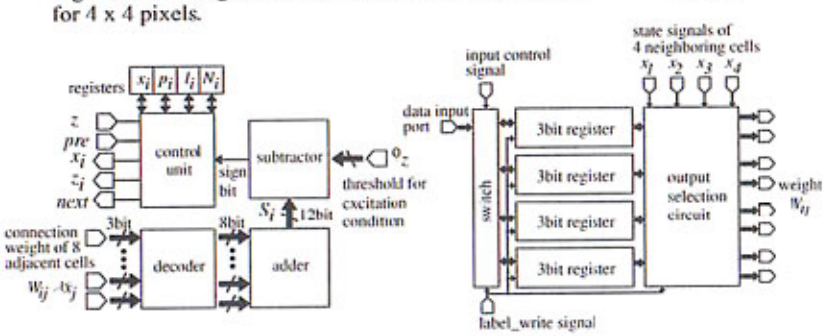


Fig. 3: Block diagram of the cell-network construction for 4 x 4 pixels.



(a) block of active cell P_i. (b) block of 4 connection-weight registers.

Fig. 4: Structure of active cells and connection-weight-register blocks.

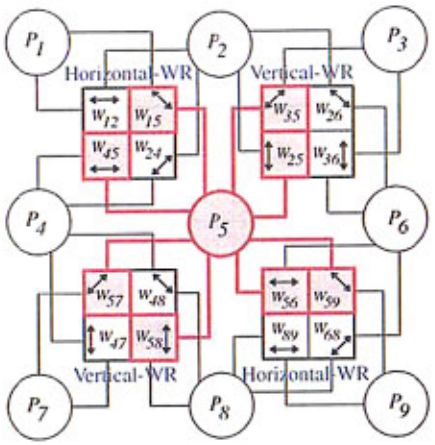
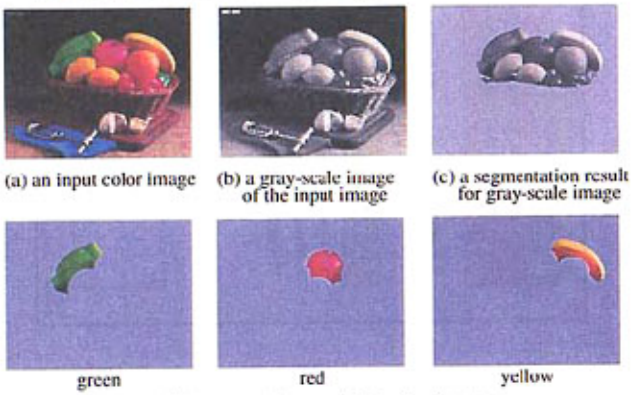


Fig. 5: An example of connections among cell P_5 and its four neighboring connection-weight-register blocks.



(a) an input color image (b) a gray-scale image of the input image (c) a segmentation result for gray-scale image

green red yellow

(d) segmentation results for color image

Fig. 6: Example of image segmentation for a color image.

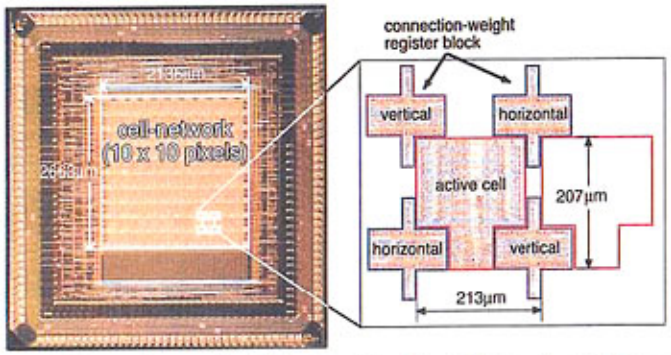


Fig. 7: Photomicrograph of the test-chip with a 0.35μm 3 metal layer CMOS technology. (a) cell network including 10 x 10 cells. (b) Layout of an active cell and four adjacent connection-weight-register blocks.

Table. 1: Estimated pixel density by full custom design.

Technology node(nm)	integration density (pixel/mm²)	
	High Speed Architecture (bit parallel)	Compact Architecture (bit serial)
350	22	43
180	81	163
100	263	527
50	1054	2107
35	2150	4300

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Image Segmentation

- Natural image is partitioned into meaningful regions
- Important initial task for higher level image processing

- Pixel-Based
- Edge-Based
- Region-Based
- Model-Based

†D.L.Wang et al., Neural Comp., 97

LEGION (Locally Excitatory, Globally Inhibitory Oscillator Network)†

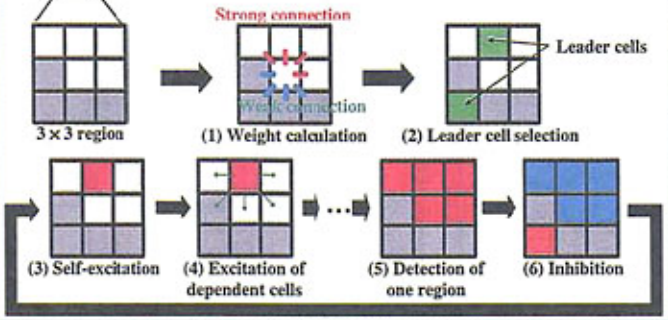
- Region-growing approach
- Binary/gray-scale image
- Neural oscillator network
- Good segmentation quality
- Differential-equation based algorithm
- Difficulty of VLSI implementation

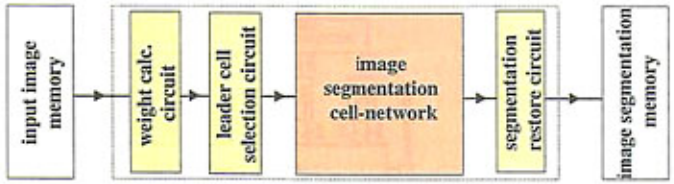
Digital Implementation

- Hardware implementation for real-time processing
- Improvement for compact implementation
- Digital image segmentation algorithm

Outline of Digital Segmentation Algorithm

1. **Weight calculation:** Difference of luminance between pixels
2. **Leader cell selection:** Sum of weights with neighboring pixels has to be larger than a threshold
3. **Segmentation:** Repeat self-excitation, excitation, and inhibition





transmitted in column pipeline mode

Weight calculation circuit

- Calculate connection weights between pixels for picture columns in parallel

for gray-scale image

$$W_{ik}(L) = \frac{I_{max}(L)}{1+|I_i(L) - I_k(L)|}$$

for color image

Calculate W_{ik} for each RGB-data

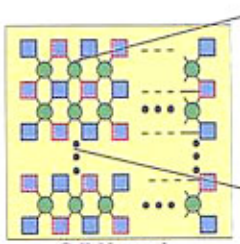
$W_{ik}(C) = \min (W_{ik}(R), W_{ik}(G), W_{ik}(B))$

Leader cell selection circuit

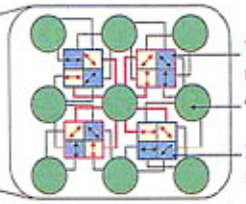
- Select a set of leader cells according to the sum of connection weights

Active cell : Consists of registers and adders/subtractors
Changes its state $x_k \in \{1,0\}$ depending on $\sum W_{ik} \times x_k$ of 8 neighbors

Weight-register block (WRB) : Two register-block types (borizontal/vertical)
Store the 4 connection-weights between the adjacent active cells
Output weights $W_{ik} \times x_k$ to adjacent active cells



Cell-Network

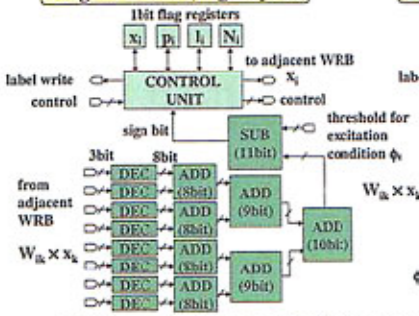


Vertical register block
Active cell
Horizontal register block

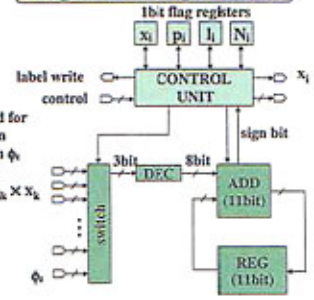
Network can be implemented by alternately laying an active cell and a WRB

- Area minimization with effective sharing of WRBs among neighboring cells
- High speed execution by pixel-based fully parallel processing

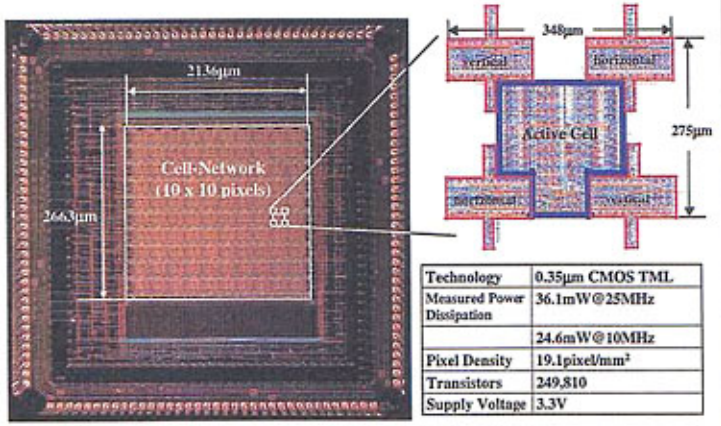
Weight Parallel (High-Speed)



Weight Serial (High-Density)

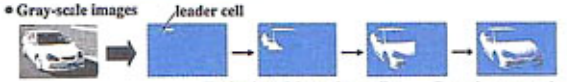


- Each active cell is excited if $\sum W_{ik} \times x_k > \phi_z$
- Two possible architectures for active cell
  - **Weight parallel**: state transition 1 cycle, larger circuit area
  - **Weight serial**: state transition 9 cycles, smaller circuit area



Technology	0.35μm CMOS TML
Measured Power Dissipation	36.1mW@25MHz
	24.6mW@10MHz
Pixel Density	19.1pixel/mm²
Transistors	249,810
Supply Voltage	3.3V

- Gray-scale images



- Color images

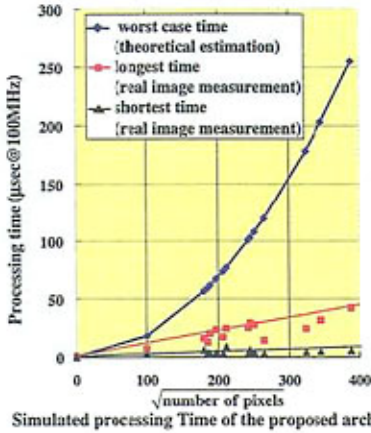
Integration density
(Estimated from full-custom layout with 3 metal layers 350nm CMOS technology)

Estimated Pixel Density

Technology node	Integration density (pixel/mm²)	
	High Speed (weight parallel)	High Density (weight serial)
350nm	22	43
180nm	81	163
100nm	263	527
50nm	1054	2107

High-Density Arch. (weight serial)
- 100nm, chip size 186mm²
  → < 320 × 240 (QVGA) image
  > 360μsec@100MHz
- 50nm, chip size 268mm²
  → < 800 × 600 (SVGA) image
  > 900μsec@100MHz

High-Speed Arch. (weight parallel)
- 50nm, chip size 268mm²
  → < 640 × 480 (VGA) image
  > 70μsec@100MHz



Simulated processing Time of the proposed architecture

- Cycle-base simulator in C and JAVA languages
- About 50 input image samples
- Assume weight parallel architecture (high-speed version)
- Worst case processing time is estimated by a checker-board image
- Weight-parallel architecture
  300 × 300 → >40μsec@100MHz
- Real time processing is also possible by weight-serial architecture (high-density version)
  300 × 300 → >360μsec@100MHz

Conclusions

- Digital algorithm for gray-scale/color image segmentation proposed
- Highly-parallel cell-network-based digital implementation architecture in conventional CMOS technology developed
- Simple adaptability to segmentation of natural gray-scale or color images by changing the preprocessing circuit for weight calculation
- Test-chip design of high-speed architecture with full-custom active cells/WRBs for architecture evaluation
- Single chip color motion-picture segmentation at 100nm-technology node possible

