Self-Assembling of Si Quantum Dots and Their Application to Memory Devices

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1. Research Background

Formation of Si nanometer dots on ultrathin SiO_2 is a key for unique electrical properties at room temperature related to coulomb blockade and/or resonant tunneling which lead us to novel functional Si-based devices such as resonant tunneling devices [1], single electron transistors [2] and quantum dot-floating gate memories [3, 4]. For the application of Si quantum dots (QDs) to the floating gate of FETs, one of major research issues is to control the size distribution of nanometer dots with an areal number density higher than $\sim 10^{11}cm^{-2}$ to realize a multi-level memory operation at room temperature.

2. Self-Assembling Formation of Si QDs by Low Pressure CVD

We have demonstrated that hemispherical single-crystalline Si QDs with a fairly uniform size distribution and a high areal density ($\sim 10^{12}cm^{-2}$) can be spontaneously formed on thermally-grown SiO_2 layers by controlling the early stages of LPCVD using a SiH_4 gas [5]. The temperature dependences of the areal dot density and the dot size in the early stages of LPCVD in the range of 560-700°C have shown that, for the dot formation on clean as-grown SiO_2, the Si-O bond breaking plays a role in the creation of nucleation sites and the dot size is rate-limited by the SiH_4 decomposition on Si and Si cohesive action. In addition, it has been found that surface Si-OH bonds if any act as reactive sites during LPCVD to efficiently promote the dot formation. Also, the SiH_4 pressure dependence of the areal dot density at 560°C show that, in the pressure region below 0.1Torr, a reduction in the SiH_4 pressure causes a marked decrease in the dot density, especially on as-grown SiO_2, suggesting that the thermal decomposition of small Si clusters before reaching the critical size for stable nucleation growth becomes significant under a low SiH_4 flux. The result indicates that, to obtain high selectivity of Si dot nucleation between as-grown and OH-terminated SiO_2 surfaces, the suppression of the spontaneous nucleation on as-grown SiO_2 is of great importance and the control of the SiH_4 pressure during LPCVD is one of critical factors.

3. Positioning of Si QDs on SiO_2

Based on the better understanding of the Si dot formation mechanism, the spatial control of OH termination on SiO_2 leads into positioning the nucleation site. In fact, the chemical or electrochemical surface modification on a nanometer scale by using AFM/STM probe techniques enables us to make regular arrays of Si dots as demonstrated in Fig. 1. In the case, the as-grown SiO_2 surface just before LPCVD was exposed to the electron beam from the a Pt (20%Ir) STM tip in H_2 ambient of $1x10^{-5}$Pa[6]. Since H atoms are adsorbed on the clean Pt-tip surface through dissociative adsorption even at room temperature and emitted under a high electric field between the tip and the sample surface[7], reactive sites such as Si-H and Si-OH bonds are formed efficiently.

4. Si QDs Acting as Electron Memory Nodes

We have demonstrated that charges retained in the single Si dot covered with ultrathin SiO_2 are directly quantified from the change in the surface potential at each of Si dots induced by electron injection or emission through ultrathin SiO_2 as measured with an AMF/Kelvin probe technique[8]. Based on the estimation of electron charging energy and quantization energy in Si QDs, we have designed and fabricated MOS capacitors and FETs with the Si dots as a floating gate. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of Si-QDs floating gate MOS capacitors exhibit unique hystereses which arise from charging and discharging in the Si QDs through the bottom tunnel oxide as shown in Fig. 2. For the case on p-Si(100) with an acceptor concentration of $3x10^{16}cm^{-3}$, the C-V curve measured from –3 to 3V is almost identical to the C-V curves for the case of uncharged Si-QDs floating gate. Similarly, the C-V curve measured from +3 to –3V for the case on n-Si(100) with a donor concentration of $1x10^{15}cm^{-3}$, is almost identical to the C-V curve for the uncharged floating gate. In both cases, a flat-band voltage shift of ~0.27V is observed and the capacitance peak, which is due to the emission of remaining charges to the substrate as seen in I-V characteristics, is measured around the corresponding flat-

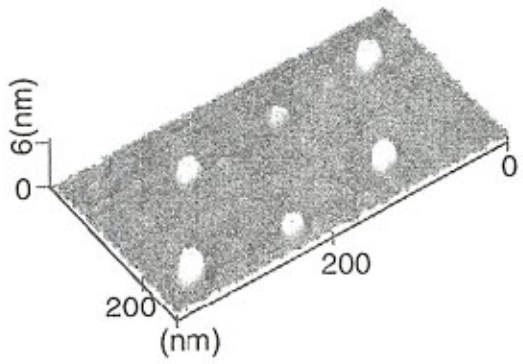

Fig. 1 AFM image obtained after Si dot formation at 560°C on the SiO_2 surface modified with a spot pattern by the STM tip. In the STM surface modification prior to LPCVD, the substrate bias and the duration time were +10V and 0.1s, respectively.

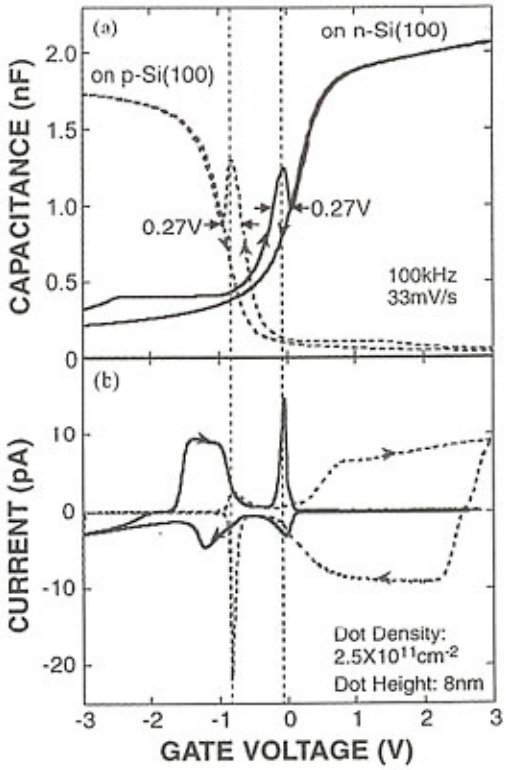

Fig. 2 Capacitance-voltage (a) and current-voltage (b) characteristics of Si-QDs floating gate MOS capacitors fabricated on p-Si(100) and n-Si(100).

band voltage, namely the voltage separation of the peaks agrees well with the value expected from the difference in the Fermi level between p-Si(100) and n-Si(100). The results indicate that the dots act as electric memory nodes. In other words, we can rule out the contribution of traps with specific energy levels to the measured C-V hystereses. I-V characteristics shows multiple-step electron charging (or discharging) characteristics of the Si-dot floating gate, suggesting that Coulombic force arising from charged dots efficiently suppresses the electron charging of neighboring neutral dots. When the floating gate consists of double-stacked dots instead of a single dot layer, the retention characteristics are improved significantly with keeping the tunneling oxide thickness constant for a high writing speed as represented in Fig. 3. For nMOSFETs with a double-stacked Si-QDs floating gate, the distinct multi-level memory operation even at 350K are confirmed (Fig. 4).

5. Research Issues in the COE Program

To further improve the performance of the Si-QDs floating gate MOSFETs, we will focus on the precise control of the dot size distribution and the optimization of the dot stacked structure, especially the oxide thickness between the dots. In addition, we will extend our research to realize photosensitive functional devices with the stacked Si-QDs floating gate for optical interconnect. In a preliminary experiment, we have demonstrated the electron injection to the Si-QDs floating gate is enhanced by illumination with 633nm photons through n^+poly-Si gate.

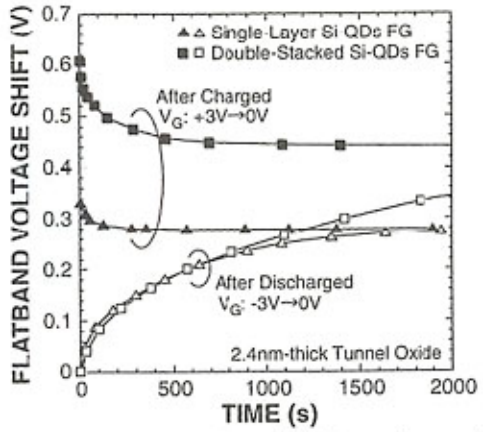

Fig. 3 Retention characteristics of MOS capacitors with the floating gate consists of double-stacked and a single-layer Si QDs.

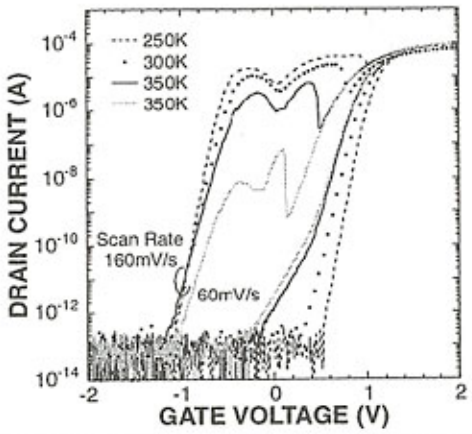

Fig. 4 Drain current vs gate voltage characteristics of a Si-QDs floating gate MOSFET, which are measured after fully discharged at a gate bias of -4V. The drain voltage was 50mV. The temperature was changed in the range from 250 to 350K.

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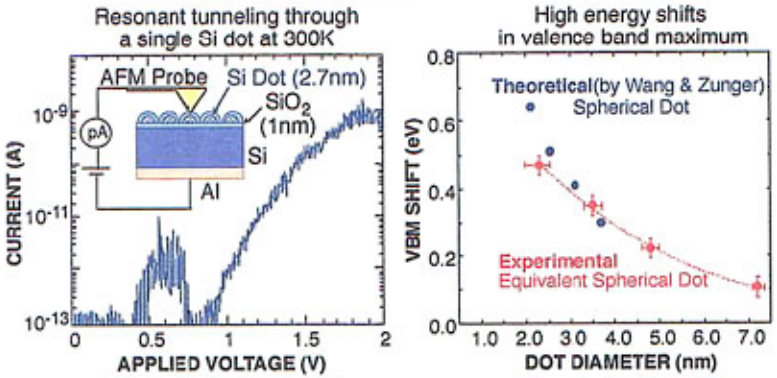
References

[1] M. Fukuda, K. Nakagawa, S. Miyazaki and M. Hirose, Appl. Phys. Lett. 70 (1997) 2291.
[2] A. Dutta , S. Oda, Y. Fu and M. Willander, Jpn. J. Appl. Phys. 39 (2000) 4647.
[3] S. Tiwari, F. Rana, H. Hanafi, H. Hartstein, E. F. Crabbé and K. Chan, Appl. Phys. Lett. 68 (1996) 1377, ibid 69 (1996) 1232.
[4] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. 40 (2001) L721.
[5] S. Miyazaki, Y. Hamamoto, E. Yoshida, M. Ikeda and M. Hirose, Thin Solid Films 369 (2000) 55.
[6] S. Miyazaki, M. Ikeda, E. Yoshida, N. Shimizu, Proc. of the 25th Intern. conf. on the Physics of Semiconductor (2001) p. 373.
[7] H. Kuramochi, H. Uchida and M. Aono, Phys. Rev. Lett. 72 (1994) 932.
[8] K. Takeuchi, H. Murakami and S. Miyazaki, Ext. Abs. Semicond. Technol. Conf. (2002) No. 33.

Our Previous Work



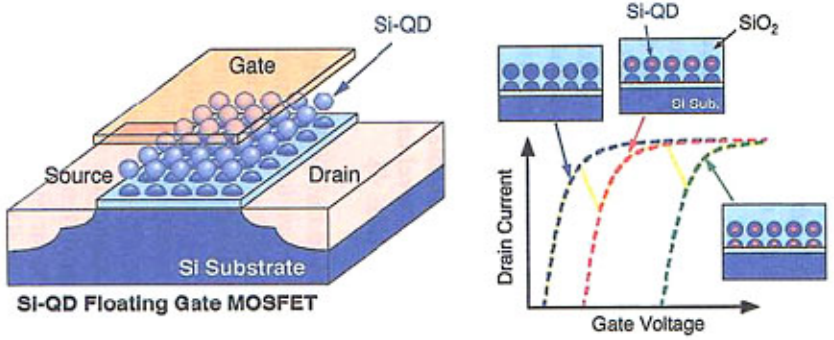
Fukuda et al. APL (1997) Ding et al. APL (1998)

- Quantum Size Effect
- Coulomb Blockade

⇨ Novel Functional Devices

- **QD Floating Gate Memory** — A. Kohno et al., JJAP (2001); S. Tiwari et al., APL (1996)
- **Single Electron Transistor** — Y. Takahashi et al., IEDM (1994, 1998)

Si-QDs Functional Memory –Room Temperature Multivalued Operation at Low Voltages–

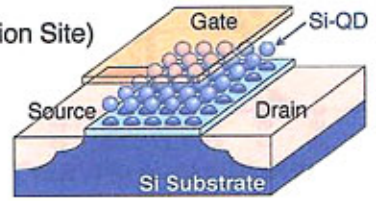


Control of Electron Charging & Coulombic Interactions among Charged Electrons in Multiplly-Stacked Si-QDs Floating Gate ⇨ Control of Dielectric Functions in Dot-Stacked Gate Dielectrics

Application of Si QDs to a Floating Gate in MOSFETs

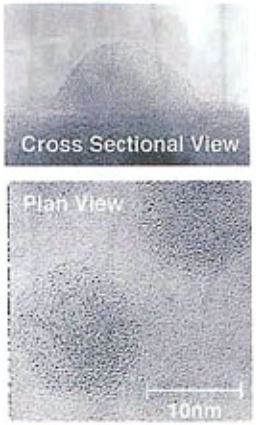
Key Issues

- To control the growth of Si nanocrystallites on SiO_2 as accurate as possible (Dot Size, Dot Density & Nucleation Site)
- To minimize the size distribution of Si dots with an areal density as high as ~$5x10^{11}cm^{-2}$



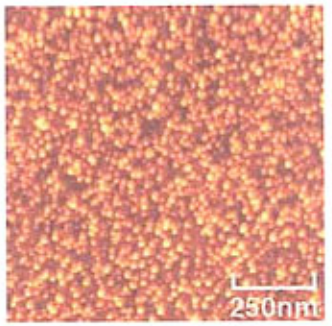
Spontaneous Formation of nc-Si on SiO_2 by LPCVD

HR-TEM Images



on as-grown SiO_2
600°C, 0.2Torr, 36s

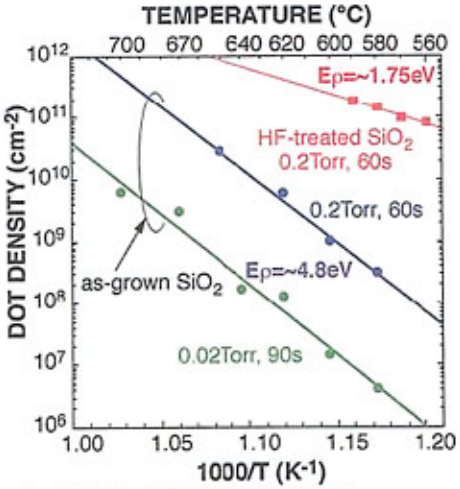
AFM Image



on HF-treated SiO_2
560°C, 0.2Torr, 90s

DOT DENSITY : **$1.7x10^{11}$** cm^{-2}

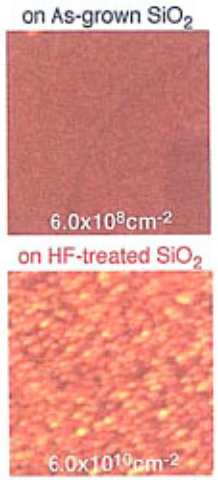
Temperature Dependence of Areal Dot Density



E_ρ=4.8eV ⇒ Si-O Bond Energy

E_ρ=1.75eV ⇒ Chemical Reaction between Si-OH Bonds and SiH_4

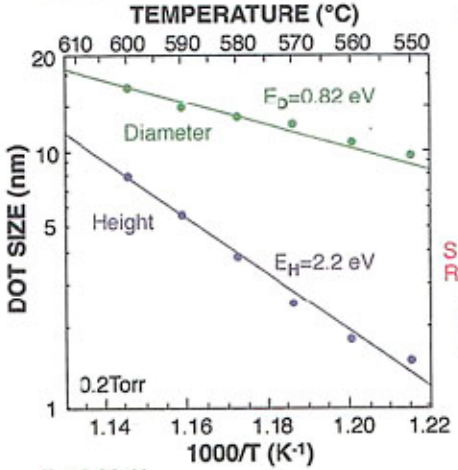
AFM Images after Si Dot Formation



SiH_4, 640°C, 0.02Torr, 90s

Si-OH Bond ⇒ Nucleation Site of Si Dot

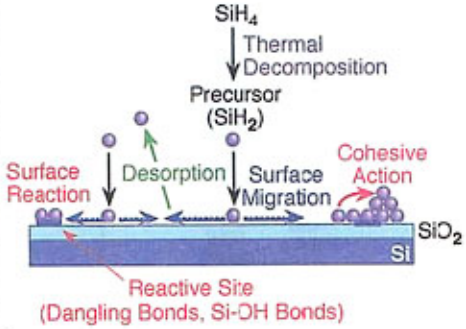
Temperature Dependence of Si Dot Size



E_D=0.82eV ⇒ SiH_4 Decomposition Energy on Si

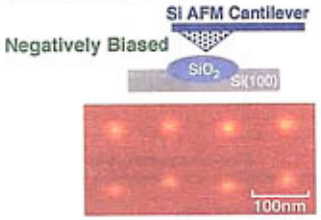
E_H=2.2eV ⇒ Si Cohesive Energy

Model for Si Dot Formation



Positioning of Self-Assembling Si Dots on SiO_2

Local Anodic Oxidation



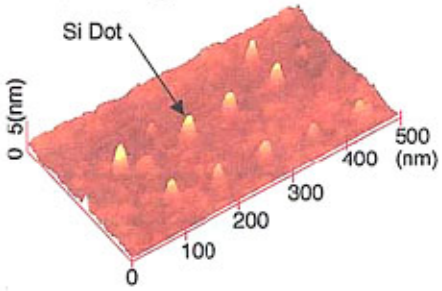
Oxidation
Dry O_2 : 1000°C, 0.3Torr, 10sec

HF-Treatment : OH-Terminated SiO_2

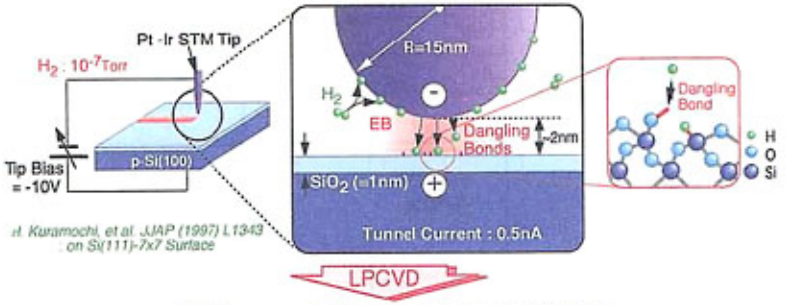
Oxidation
Dry O_2 : 750°C, 0.3Torr, 1min

Si Dot Formation by LPCVD
SiH_4 : 565°C, 0.1Torr, 90sec

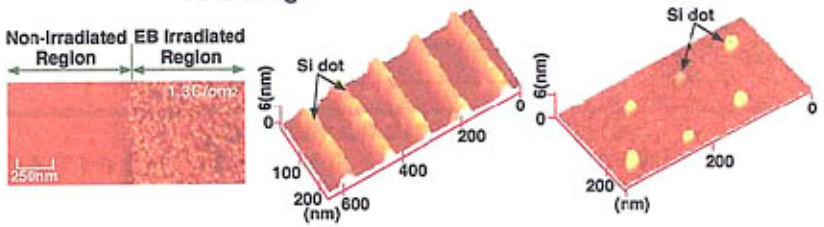
AFM Image After Dot Formation



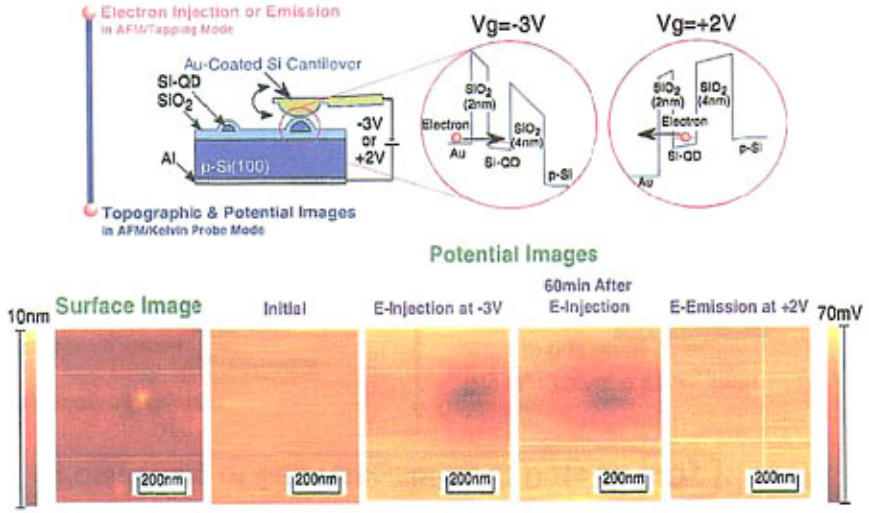
Nucleation Site Control by Low Energy Electron Beam



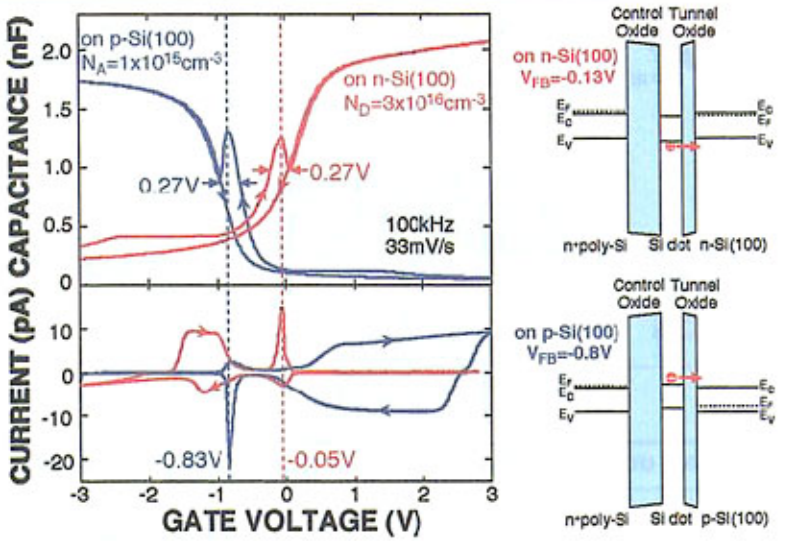
AFM Images After Formation of Si-Dots



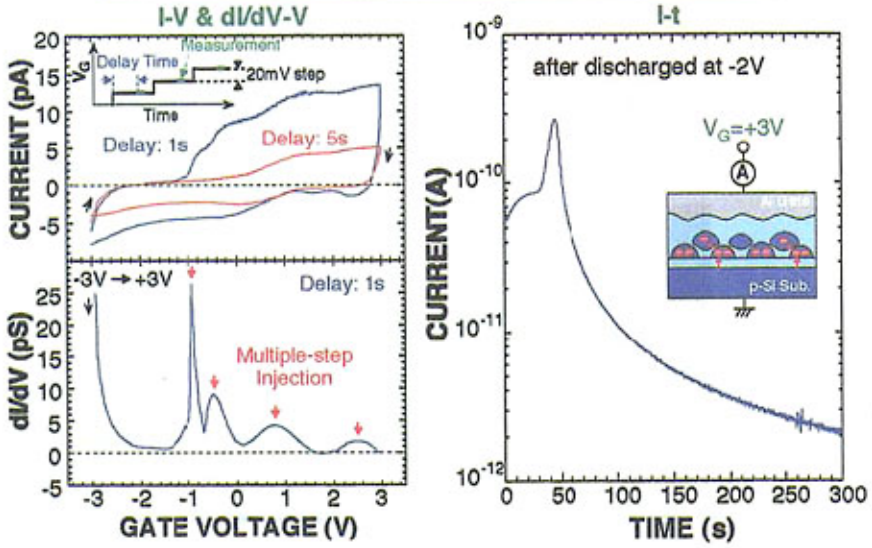
Confirmation of Single Electron Charging & Discharging in Single Si-QD



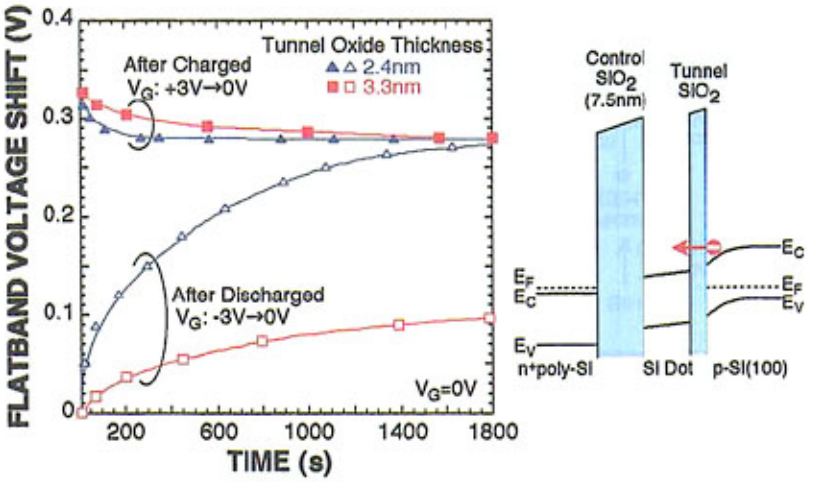
C-V & I-V Characteristics of Si-QDs Floating gate MOS Capacitors Fabricated on p-Si(100) & n-Si(100)



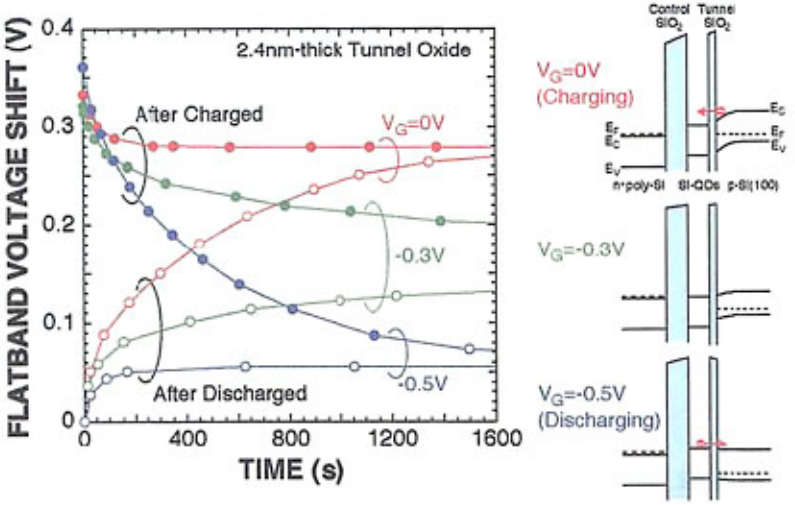
Charge Injection Characteristics for MOS Capacitor with Double-Stacked Si-QDs Floating Gate



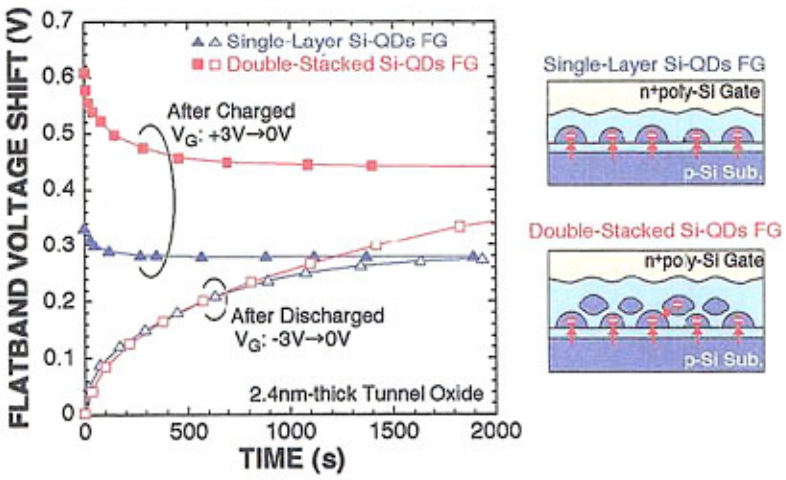
Retention Characteristics on ΔV_{FB} for a Si-QDs Floating Gate



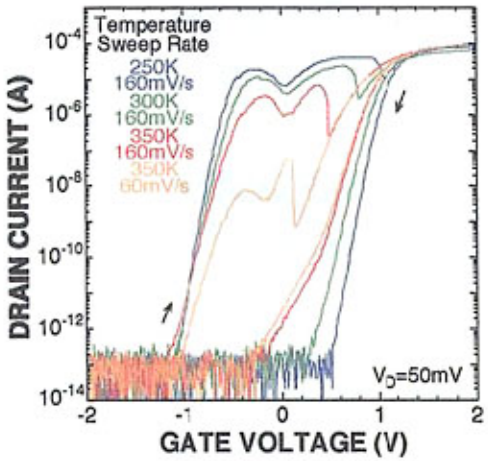
Retention Characteristics on ΔV_{FB} for a Si-QDs Floating Gate



Retention Characteristics on ΔV_{FB} for Single or Double Si-QDs Floating Gate



I_D-V_G Characteristics for MOSFET with Double-Stacked Si-QDs Floating Gate



Photoelectron Charging to Si QD Floating Gate

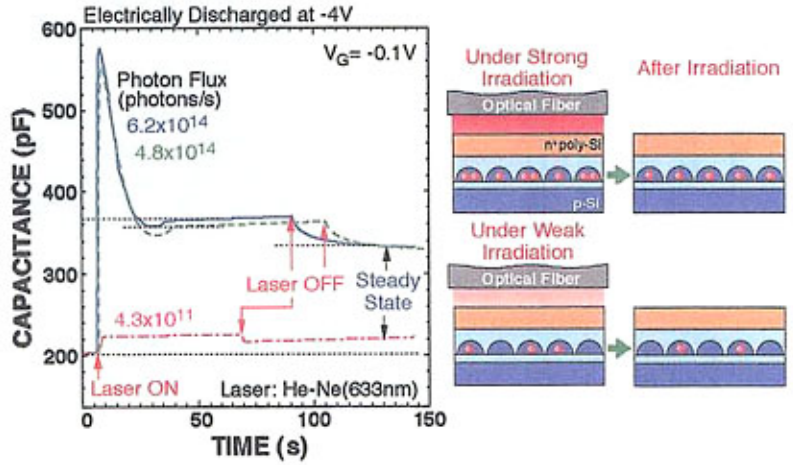
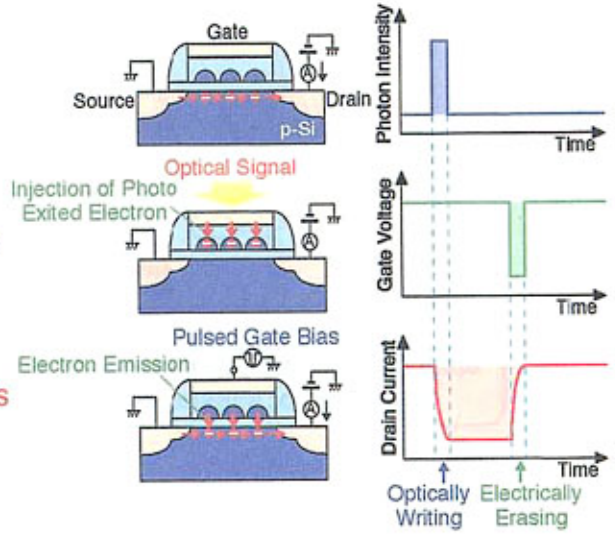


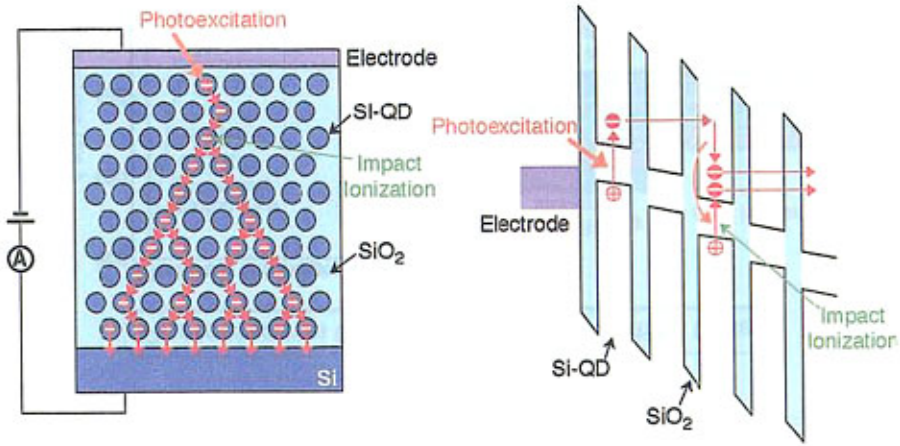
Photo-Coupled Si-QDs Floating Gate Memories –Optically-Writing/Electrically-Erasing–

Detection of a Few Photons & Transport Control of a Few Electrons

I/O Devices for Optical Interconnects



Application of Regularly-Stacked Si-QDs to High-Efficiency Avalanche Photodetector



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