Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate MOS Memories

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1. Introduction

The application of silicon quantum dots (Si-QDs) to a floating gate of MOSFETs has been attracting much attention because of its multivalued capability [1, 2]. For MOS structures with a Si-QDs floating gate [3, 4], we have confirmed the memory operations at room temperature. Also, we have demonstrated that unique multiple-step charging in the Si-QD floating gate to a level of about one electron per dot [4].

In this paper, to gain a better understanding of such a multiple-step charging mechanism, we focus on the charge injection characteristics in MOSFETs with a Si-QDs floating gate.

2. Fabrication of Si-QDs Floating Gate MOSFETs

Hemispherical and single-crystalline Si-QDs were self-assembled on 3.3nm-thick SiO_2 by controlling the early stages of LPCVD of pure SiH_4 at 575°C [5]. After the formation of the first Si-QD layer, a ~1nm-thick thermal oxide layer was thermally grown, and the second Si-QD layer was deposited under the same conditions. The average dot height and the total dot density evaluated by AFM were ~7.2nm and ~6×10^{11} cm^{-2}, respectively. The surface of the second Si-QD layer was also covered with ~1nm-thick thermal oxide. Subsequently, a 3.3nm-thick amorphous Si layer was grown over the dot layer by LPCVD at 440°C, and fully oxidized in dry O_2 at 1000°C to form a 7.5nm-thick control oxide conformally. Finally, n^+poly-Si gate and source/drain junction were fabricated. The gate length and width are 0.5~0.8 and 10μm, respectively.

3. Results and Discussion

The drain current versus gate voltage (I_D-V_G) characteristics of a Si-QDs floating gate MOSFET were measured at room temperature as shown in Fig. 1. The gate voltage was swept between -4 and +3V at a different sweep rate with a range of 4.6 to 61mV/s. The I_D-V_G curves show characteristic hysteresis arising from electron charging or discharging of the Si-QDs floating gate. Three current bumps, which were observed in the gate voltage sweeping from -4 to +3V, indicate the multiple-step electron charging to the Si-QDs floating gate caused by the Coulomb blockade effect. The observed multiple-step charging is like to be related to size-uniformity of the Si-QDs with an areal density of $6 \times 10^{11} cm^{-2}$. Note that the threshold voltage shift at each charging steps is not equal to that of the next charging step and slightly increased with progressive electron charging. This implies that the Coulomb interaction among the neighboring charged QDs plays a subsidiary role on the electron tunneling from the channel to the Si-QDs. In other words, this can be interpreted in terms that the charging energy of the Si-QDs depends on not only charged states of individual Si-QDs but also charged states of neighboring QDs. With decreasing sweep rate, the current bumps become clear and appear at lower gate voltage. In general, since the charging time of the Si-QD floating gate strongly depends on the gate voltage, faster the sweep rate is, higher the gate voltage for the charge injection becomes. Besides, the result of Fig. 1 may be associated with the rearrangement of charge distribution in the Si-QDs floating gate during the gate voltage sweep as discussed later.

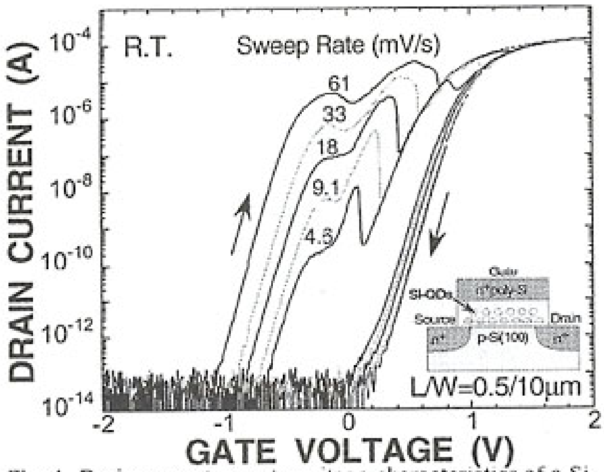

Fig. 1 Drain current vs gate voltage characteristics of a Si-QDs floating gate MOSFET, which were measured after fully discharged at a gate bias of -4V. The drain voltage was 50mV. The voltage sweep rate was changed in the range from 4.6 to 61 mV/s.

Figure 2 shows temporal change in the drain current (I_D-t) measured at constant gate biases after complete discharging of the Si-QDs floating gate. The drain current decreases stepwise with time, which originates from the electron charging to the Si-QDs floating gate. The charged state after each current step corresponds to that of the scanned I_D-V_G characteristics. The distinct metastable states, in which the drain current is almost constant with

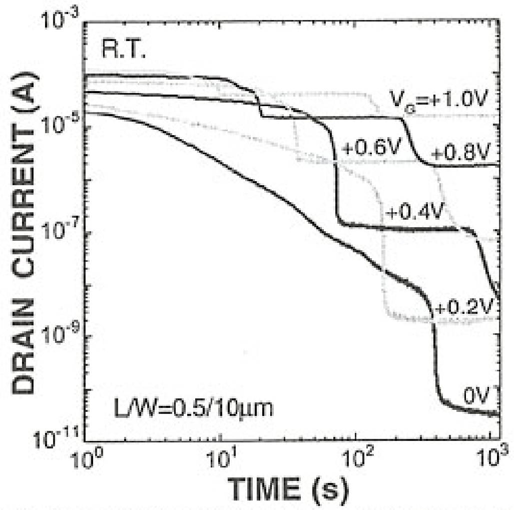

Fig. 2 Temporal change in drain current at various gate biases and a drain voltage of 50mV after complete discharging of a Si-QDs floating gate. For the discharging, the gate was biased at -4V.

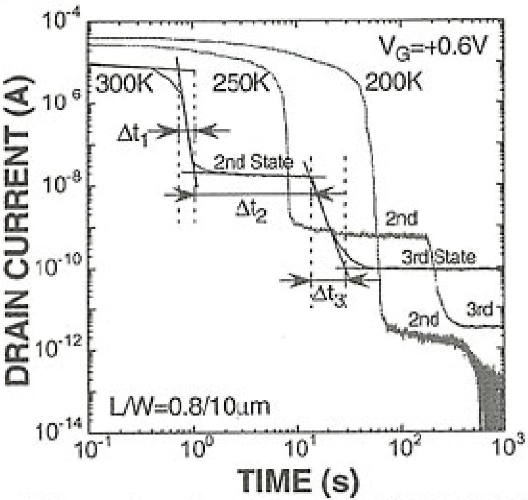

Fig. 3 Temperature dependence of I_D-t characteristics at a gate bias of 0.6V after complete discharging under the same condition of Figs. 1 and 2.

respect to holding time, indicate that the total amount of effective charge in the Si-QDs floating gate remains unchanged in each of the metastable states. This result suggests that injected electrons in the Si-QDs floating gate redistribute during each metastable state to reduce the effect of the Coulomb interaction among charged QDs, namely to decrease the charging energy of QDs.

To find a clue to the mechanism of electron charging to the Si-QDs floating gate, temperature dependence of I_D-t characteristics was measured at a constant gate bias in the temperature range from 200 to 300 K as shown in Fig. 3. Obviously, a decrease in temperature decelerates the electron charging and prolongs the metastable states.

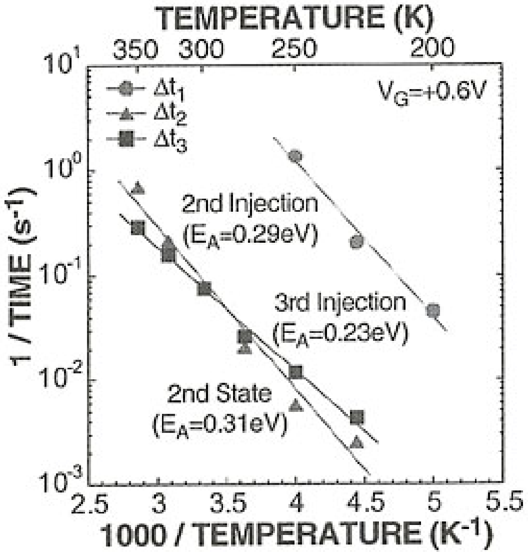

Fig. 4 Arrhenius plot of 2nd injection (Δt_1), 2nd state (Δt_2) and 3rd injection (Δt_3) time from I_D-t characteristics.

This suggests that the tunneling probability is decreased with temperature for rearrangements of electrons in the Si-QDs floating gate. The charging time (Δt_1 and Δt_3) and metastable time (Δt_2) were determined with the method in which both charging and metastable states were linearly extrapolated as demonstrated in Fig. 3, and their reciprocal values are summarized in Arrehnius plots (Fig. 4). From the slope of the Arrehnius plots, the activation energy in the range of 0.23~0.31eV were obtained. Estimating the sum of quantized and charging energies for QDs, the obtained activation energy is almost equal to the energy separation between states for tunneling in QDs. Therefore, this result could be interpreted in terms that the electron tunneling between different energy states plays an important role on multiple-step charging characteristics.

4. Conclusions

The multiple-step electron charging to a Si-QDs floating gate in the MOSFETs has been demonstrated at room temperature. The metastable states in electron charging at the constant gate bias are attributable to the rearrangement of charge distribution in the Si-QDs floating gate due to the Coulomb interaction among the charged QDs.

References
[1] S. Tiwari, F. Rana, K. Chan, L. Shi and H. Hanafi, Appl. Phys. Lett. 69 (1996) 1232.
[2] L. Guo, E. Leobandung and Y. Chou, Appl. Phys. Lett. 70 (1997) 850.
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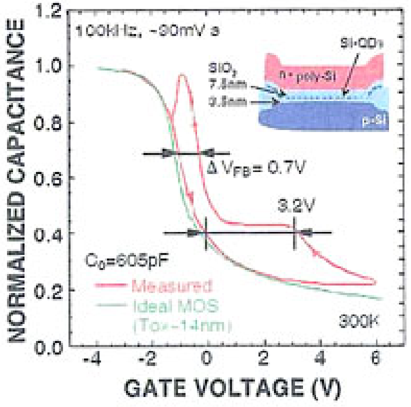
[4] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. 40 (2001) L721.
[5] S. Miyazaki, Y. Hamamoto, E. Yoshida, M. Ikeda and M. Hirose, Thin Solid Films, 369 (2000) 55.

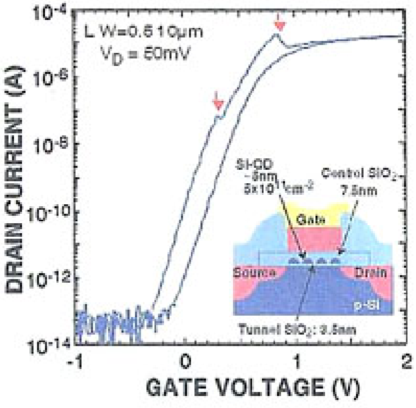
Our Previous Work

C-V Characteristics



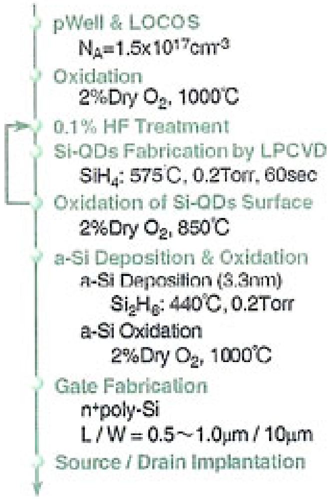
Kohno et al. SSDM (1997)

I_D-V_G Characteristics

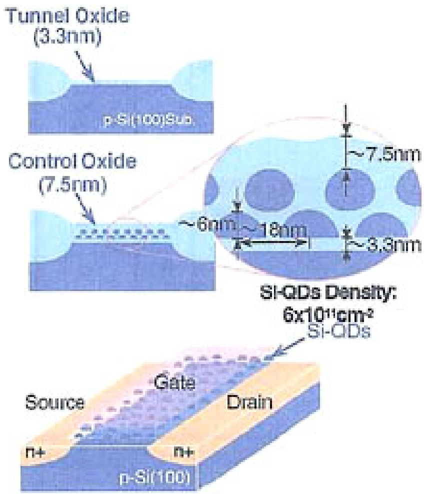


Kohno et al. JJAP (2001)

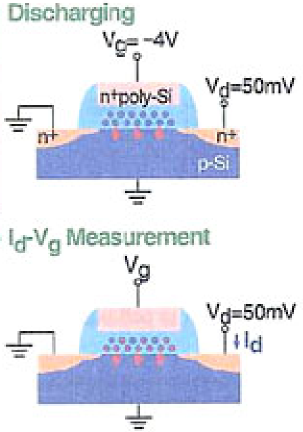
Fabrication of Si-QDs Floating Gate nMOS FETs

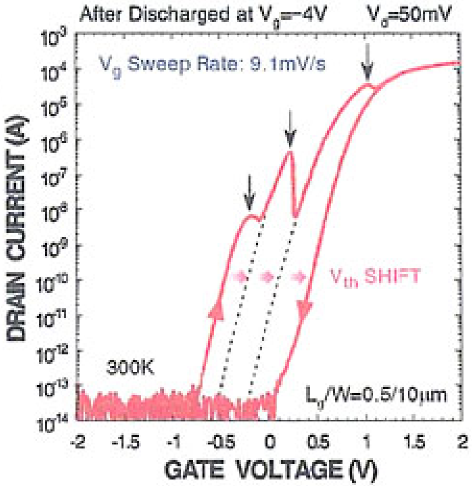


- pWell & LOCOS
  - N_A=1.5x10^{17}cm^{-3}
- Oxidation
  - 2%Dry O_2, 1000°C
- 0.1% HF Treatment
- Si-QDs Fabrication by LPCVD
  - SiH_4: 575°C, 0.2Torr, 60sec
- Oxidation of Si-QDs Surface
  - 2%Dry O_2, 850°C
- a-Si Deposition & Oxidation
  - a-Si Deposition (3.3nm)
    - Si_2H_6: 440°C, 0.2Torr
  - a-Si Oxidation
    - 2%Dry O_2, 1000°C
- Gate Fabrication
  - n+poly-Si
  - L / W = 0.5~1.0μm / 10μm
- Source / Drain Implantation

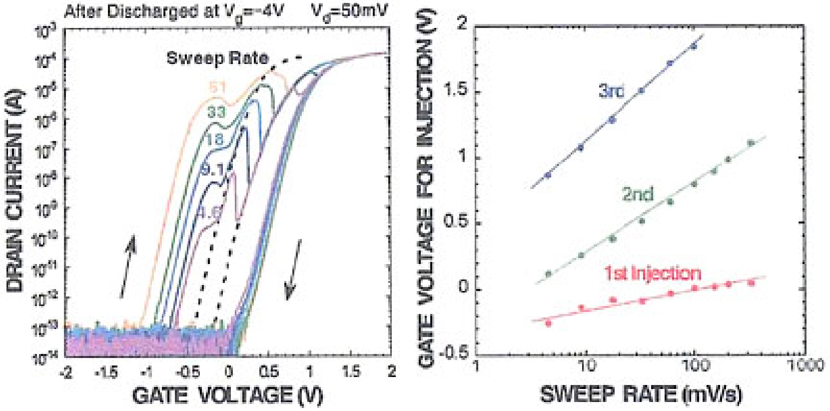


I_d-V_g Characteristics for MOSFET with Doubly-Stacked Si-QDs Floating Gate

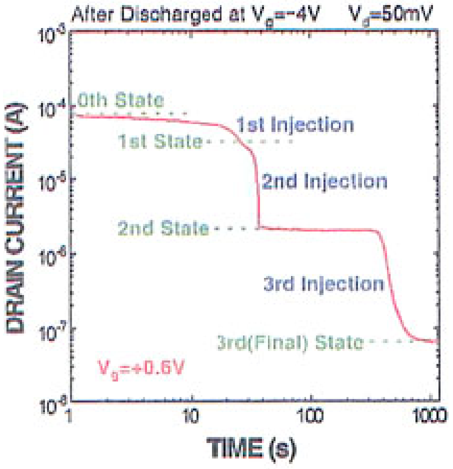




Sweep Rate Dependence of I_d-V_g Characteristics

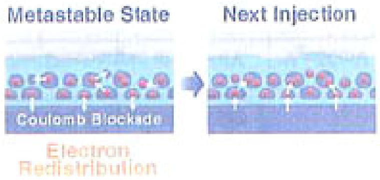


Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate

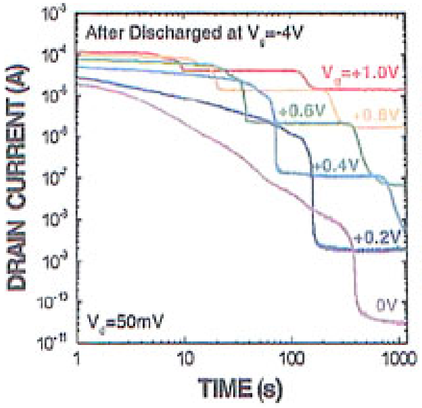


- Multiple-Step Electron Injection
- Incubation period between electron injections

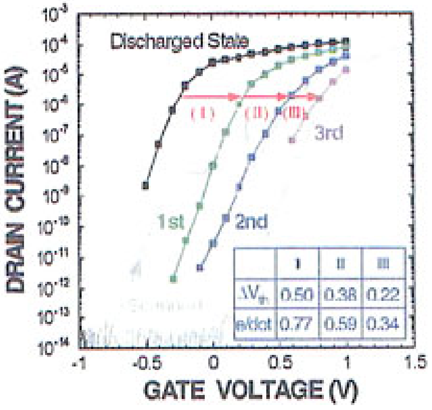
During each metastable state, electrons injected in Si-QDs floating gate are likely to be redistributed for the next electron injection.



I_d-t Characteristics

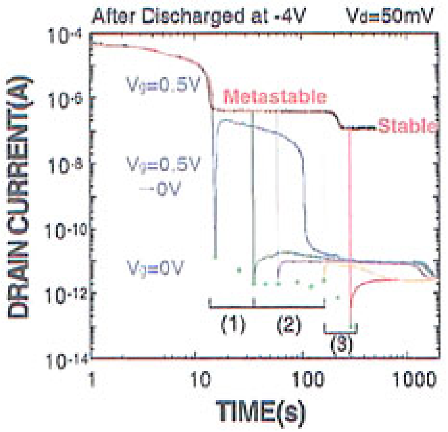


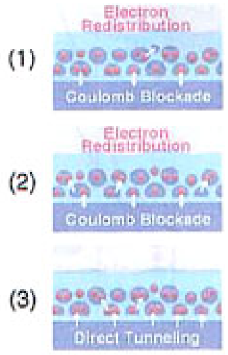
I_d-V_g Characteristics



	I	II	III
ΔV_{th}	0.50	0.38	0.22
e/dot	0.77	0.59	0.34

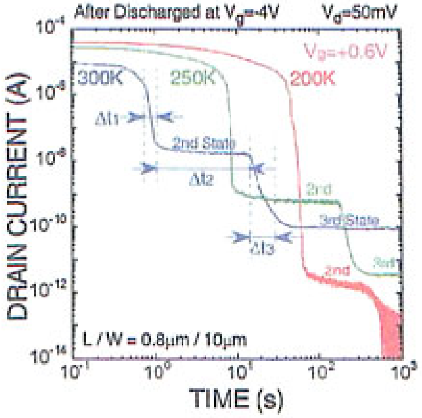
Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate

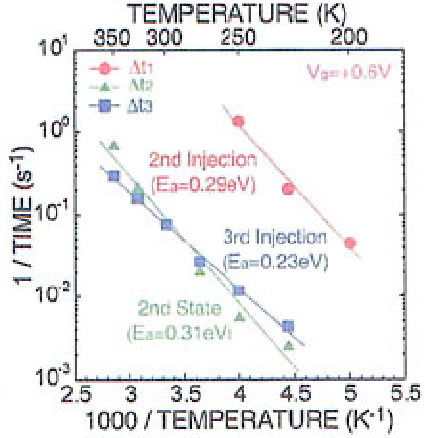




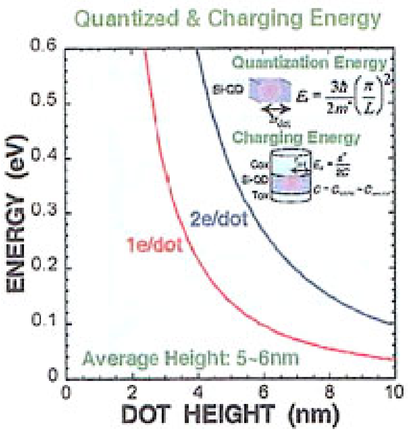
Average dot height: 6nm
Mean distance between dots for the 1st dot layer: 17nm

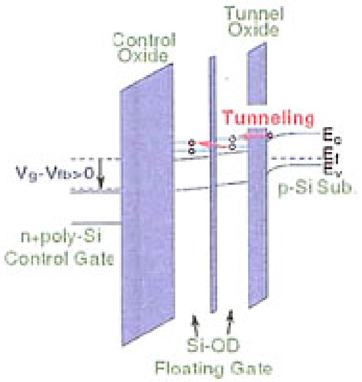
Temperature Dependence of I_d-t Characteristics



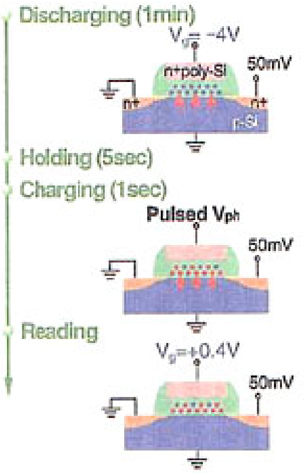


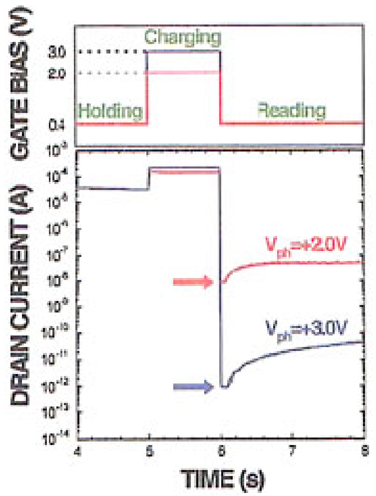
Model for Electron Charge in Si-QDs Floating Gate



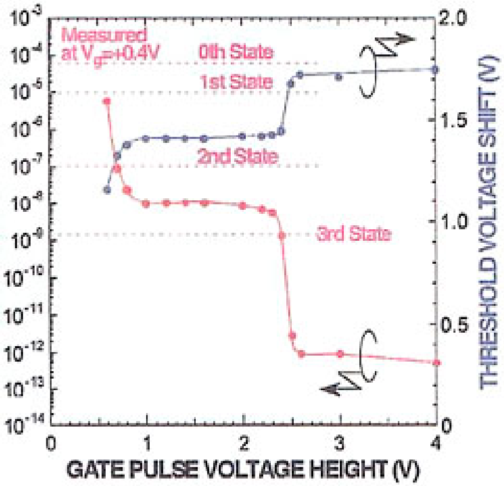


Temporal Changes in Drain Current for Pulse Gate Bias





Charging Characteristics by Pulsed V_g



Conclusions

- The multiple-step electron charging to a Si-QDs floating gate in the MOSFETs has been demonstrated at room temperature.
- The metastable states in electron charging at the constant gate bias are attributable to the rearrangement of charge distribution in the Si-QDs floating gate due to the Coulomb interaction among the charged QDs.
- It is suggested that the electron tunneling between different energy states plays an important role on multiple-step charging characteristics.