List of Publications, Patents, and Awards

I. Circuits and Systems

COE Subject

I-1. Journal Papers

[1] H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata, "Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques," IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, 2002.

[2] T. Morie and T. Matsuura and M. Nagata and A. Iwata, "A Multi-Nano-Dot Circuit and Structure Using Thermal-Noise Assisted Tunneling for Stochastic Associative Processing," J. Nanosci. Nanotech., Vol. 2, No. 3, pp. 343-349, June, 2002

[3] K. Katayama, M. Nagata, T. Morie and A. Iwata, An Hadamard, "Transform Chip Using the PWM Circuit Technique and Its Application to Image Processing," IEICE Trans. Electron., Vol. E85-C, NO.8, pp. 1596-1603, Aug. 2002.

[4] H.J. Mattausch, T. Gyohten, Y. Soda and T. Koide, "Compact Associative-Memory Architecture with Fully-Parallel Search Capability for the Minimum Hamming Distance," IEEE Journal of Solid-State Circuits, 37, 218-227 (2002).

[5] K. Katayama, and A. Iwata, "A High-Resolution CMOS Image Sensor with Hadamard Transform Function," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences E86-ANO.2, pp. 396-403、Aug.2003.

[6] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, "A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models," IEEE Trans. Nanotechnology, Vol. 2, No. 3, pp. 158-164, Sept. 2003

[7] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels," IEICE Trans. Fundamentals., vol.E87-A, pp.376-383, Feb. 2004.

[8] T. Yoshida, M. Akagi, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Wireless Neural-Sensing LSI," IEICE Trans. Electronics, vol.E87-C, pp.996-1002, June 2004.

[9] T. Morie, T. Nakano, J. Umezawa, and A. Iwata, "Gabor-Type Filtering Using Transient States of Cellular Neural Networks," Intelligent Automation and Soft Computing, in press, 2004.

[10] K. Korekado, T. Morie, O. Nomura, H. Ando, T. Nakano, M. Matsugu, and A. Iwata, "A VLSI Convolutional Neural Network for Image Recognition Using Merged/Mixed Analog-Digital Architecture," Int. J. Fuzzy and Intelligent Systems, in press, 2004.

[11] T. Sasaki, T. Inoue, N, Omori, T. Hironaka, H.J. Mattausch, and T. Koide, "Chip Size and Performance Evaluations of Shared Cache for On-chip Multiprocessors," IEICE Trans. on Information & Systems Part 1, vol. J87-D-I, 350-363 (2004) (in Japanese).

[12] S. Fukae, T. Inoue, H.J. Mattausch, T. Koide, and T. Hironaka, “Distributed against centralized crossbar function for realizing bank-based multiport memories,” IEE Electronics Letters 40, 101-103 (2004)

[13] K. Johguchi, Z. Zhu, T. Hirakawa, T. Koide, T. Hironaka, and H.J. Mattausch, “Distributed-crossbar architecture for area-efficient combined data/instruction caches with multiple ports,” IEE Electronics Letters 40, 160-162 (2004).

[14] H. Noda, K. Inoue, M. Kuroiwa, F. Igaue, K. Yamamoto, H.J. Mattausch, T. Koide, A. Amo, A. Hachisuka, S. Soeda, F. Morishita, K. Dosaka, K. Arimoto, and T. Yoshihara, “ A Cost-Efficient High-Performance Dynamic TCAM with Pipelined Hierarchical Searching and Shift Redundancy Architecture,” IEEE Journal of Solid-State Circuits, 39, in press (2004).

[15] T. Morimoto, Y. Harada, T. Koide, and H.J. Mattausch, “Efficient Video-Picture Segmentation Algorithm for Cell-Network-Based Digital CMOS Implementation,” IEICE Trans. on Information & Systems, vol. E87-D, 500-503 (2004).

I-2. Proceedings of International Conferences

[16] M. Nagata, Y. Murasaka, Y. Nishimori, T. Morie, and A. Iwata, “Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models,” Proc. 7th Asia and South Pacific Design Automation Conf, pp. 71-76, Bangalore, Jan. 2002.

[17] T. Morie, J. Umezawa, T. Nakano, H. Ando, M. Nagata, and A. Iwata, “A Biologically-Inspired Object Recognition System Using Pixel-Parallel Feature Extraction VLSIs,” International Invitational Workshop on Intelligent Interface Devices, pp. 35-37, Kitakyushu, March 14, 2002.

[18] M. Nagata, T. Morie, and A. Iwata, “Modeling Substrate Noise Generation in CMOS Digital Integrated Circuits” IEEE 2002 Custom Integrated Circuit Conf, Orlando, May 2002.

[19] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models,” 2002 IEEE Silicon Nanoelectronics Workshop, pp.53-54, Honolulu, June 9, 2002.

[20] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “An Efficient Clustering Algorithm Using Stochastic Association Model and Its Implementation Using Nanostructures,” Advances in Neural Information Processing Systems 14, Ed. T. G. Dietterich, S. Becker and Z. Ghahramani, MIT Press, Cambridge, MA, 2002.

[21] K. Katayama and A. Iwata, “A High-Resolution Hadamard Transform Chip,” International Conference on Solid State Devices and Materials (SSDM), pp. 372-373, Nagoya, September17-19, 2002.

[22] T. Maeda, A. Iwata, M. Kawabata, and S. Orisaka, “A 10-GHz Bipolar VCO with Reduced Phase Noise,” International Conference on Solid State Devices and Materials (SSDM), pp. 370-371, Nagoya, September17-19, 2002.

[23] H. Ando, T. Morie, M. Nagata, and A. Iwata, “An Image Region Extraction LSI Based on a Merged/Mixed-Signal Nonlinear Oscillator Network Circuit,” 28th European Solid-State Circuits Conference (ESSCIRC 2002), CP.11, pp. 703-706, Florence, Italy, Sept. 26, 2002.

[24] K. Katayama and A. Iwata, “Pulse Coupled Neural Network using Coupled Phase Locked Loop,” International Symposium on Nonlinear Theory and its Applications (NOLTA), pp. 853-856, Xi'an,October 7-11, 2002.

[25] H.J. Mattausch, N. Omori, S. Fukae, T. Koide and T. Gyohten, “Fully-Parallel Pattern-Matching Engine with Dynamic Adaptability to Hamming or Manhattan Distance,” 2002 Symposium on VLSI Circuits Digest of Technical Papers, 252-255 (2002).

[26] Y. Yano, T. Koide and H.J. Mattausch, “Fully Parallel Nearest Manhattan-Distance-Search Memory with Large Reference-Pattern Number,” Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials (SSDM’2002), 254-255 (2002).

[27] T. Koide, T. Morimoto, Y. Harada, H.J. Mattausch, “Digital Gray-Scale/Color Image-Segmentation Architecture for Cell-Network-Based Real-Time Applications,” Proceedings of the 2002 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC‘2002), 670-673 (2002).

[28] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, “Real-Time Segmentation Architecture of Gray-Scale/Color Motion Pictures and Digital Test-Chip Implementation,” Proceedings of the 2002 IEEE Asia-Pacific Conference on ASICs (AP-ASIC‘2002), 237-240 (2002).

[29] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, “Low-Complexity, Highly-Parallel Color Motion-Picture Segmentation Architecture for Compact Digital CMOS Implementation,” Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials (SSDM’2002), 242-243 (2002).

[30] A. Iwata, “Advanced Design for Analog-RF and Digital Mixed LSIs- Crosstalknoise Evaluaiton and Reduction,” Proc. of the Workshop on SASIMI, pp.17-22, Hiroshima, April 3, 2003 (Invited).

[31] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, “A Design of Neural Signal Sensing LSI with Multi-Input-Channels,” Proc. of the Workshop on SASIMI, pp. 206-210, Hiroshima, April 3, 2003.

[32] Wen Kung Chu, Nishath Verghese, Heayn-Jun Cho, Kenji Shimazaki, Hiroyuki Tsujikawa, Shouzou Hirano, Shirou Doushoh, Makoto Nagata, Atsushi Iwata, Takafumi Ohmoto, “A Substrate Noise Analysis Methodology for Large-Scale Mixed-Signal ICs,” Proceedings of IEEE 2003 Custom Integrated Circuits Conference (CICC 2003) pp. 369-372, Sept. 2003.

[33] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “An Efficient Clustering Algorithm Using Stochastic Association and Its Implementation Using 3D-Nanodot-Array Structures,” 2003 RCIQE International Seminar on "Quantum Nanoelectronics for Meme-Media-Based Information Technologies", pp. 59-63 , Sapporo, Feb. 13, 2003 (Invited).

[34] Seiji Kameda and Tetsuya Yagi, “A silicon retina system that calculates direction of motion,” Proc. The 2003 IEEE International Symposium on Circuits and Systems vol.IV, pp.792-795, Bangkok, Thailand, 2003.5.

[35] Seiji Kameda and Tetsuya Yagi, “An analog silicon retina with multi-chip configuration,” International Joint Conference on Neural Networks 2003 Conference Proceedings pp.387-392, Oregon, the United States, 2003.7.

[36] T. Koide, H.J. Mattausch, Y. Yano, T. Gyohten and Y. Soda, "A Nearest-Hamming-Distance Search Memory with Fully Parallel Mixed Digital-Analog Match Circuitry," Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2003), 591-592 (2003), Special Feature Award, University Design Contest.

[37] T. Koide, Y. Yano, H. J. Mattausch, "An Associative Memory for Real-Time Applications Requiring Fully-Parallel Nearest Manhattan-Distance Search," 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2003), 200-205 (2003).

[38] S. Fukae, N. Omori, T. Koide, H.J. Mattausch, T. Inoue and T. Hironaka, "Optimized Bank-Based Multi-Port Memories through a Hierarchical Multi-Bank Structure," 11th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI'2003), 323-330 (2003).

[39] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, "High Access Bandwidth Multi-Port-Cache Design with Compact Hierarchical 1-Port-Bank Structure," 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2003), 394-400 (2003).

[40] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, "High-Speed and Low-Power Multi-Port-Cache," Proceedings of COOL Chips VI, 76 (2003).

[41] H. Noda, K. Inoue, H.J. Mattausch, T. Koide and K. Arimoto, "A Cost-Efficient Dynamic Ternary CAM in 130nm CMOS Technology with Planar Complementary Capacitors and TSR Architecture," 2003 Symposium on VLSI Circuits Digest of Technical Papers, 83-84 (2003).

[42] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, "A Novel Hierarchical Multi-Port Cache," Proceedings of the 29th European Solid-State Circuits Conference (ESSCIRC'2003), Estoril, Portugal, September 16-18, 405-408 (2003).

[43] T. Sueyoshi, H. Uchida, Y. Mitani, K. Hiramatsu, H.J. Mattausch, T. Koide, and T. Hironaka, "Bank-Type Multiport Register File for Highly-Parallel Processors," Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.400-401 (2003).

[44] K. Johguchi, Z. Zhu, T. Hirakawa, T. Koide, T. Hironaka, and H.J. Mattausch, "Combined Data/Instruction Cache with Bank-Based Multi-Port Architecture," Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.152-153 (2003).

[45] S. Fukae, N. Omori, T. Koide, H.J. Mattausch, and T. Hironaka, "A Hierarchical 512-Kbit SRAM with 8 Read/Write Ports in 130nm CMOS," Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.150-151 (2003).

[46] Y. Harada, T. Morimoto, T. Koide, H.J. Mattausch, "CMOS Test Chip for a High-Speed Digital Image-Segmentation Architecture with Pixel-Parallel Processing," Proceedings of the 2003 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC'2003), 284-287 (2003).

[47] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, "Low-Power Real-Time Region-Growing Image-Segmentation in 0.35 μm CMOS due to Subdivided-Image and Boundary-Active-Only Architectures," Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), 146-147 (2003).

[48] T. Morie and T. Nakano, "A face/object recognition system using coarse region segmentation and dynamic-link matching," International Symposium on Bio-Inspired Systems, Part IV, Brain-inspired Information Technology (Brain IT 2004), Kitakyushu, March 8, 2004.

[49] T. Morie, J. Umezawa, and A. Iwata, "A Pixel-Parallel Image Processor for Gabor Filtering Based on Merged Analog-Digital Architecture," accepted for presentation in 2004 Symposium on VLSI Circuits, Honolulu, Hawaii, June 17-19, 2004.

[50] M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, "A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System," accepted for presentation in 2004 Symposium on VLSI Circuits, Honolulu, Hawaii, June 17-19, 2004.

[51] T. Morie, T. Nakano, J. Umezawa, and A. Iwata, "Gabor Filtering Using Cellular Neural Networks and its Application to Face/Object Recognition," accepted for presentation in World Automation Congress, Seville, Spain, June 28 - July 1, 2004.

[52] O. Nomura, T. Morie, K. Korekado, M. Matsugu, and A. Iwata, "A Convolutional Neural Network VLSI Architecture Using Thresholding and Weight Decomposition," accepted for presentation in Int. Conf. on Knowledge-Based Intelligent Information and Engineering Systems (KES'2004), Wellington, New Zealand, Sept. 22-24, 2004.

[53] K. Sasaki, T. Morie, and A. Iwata, "A Spiking Neural Network with Negative Thresholding and Its Application to Associative Memory," accepted for presentation in 2004 IEEE Int. Midwest Symposium on Circuits and Systems (MWCAS2004), Hiroshima, July 25-28, 2004.

[54] T. Sueyoshi, H. Uchida, Y. Mitani, K. Hiramatsu, H.J. Mattausch, T. Koide, and T. Hironaka, "Compact 12-Port Multi-Bank Register File Test Chip in 0.35μm CMOS for Highly Parallel Processors," Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2004), pp.551-552 (2004).

[55] Y. Yano, T. Koide, and H.J. Mattausch, "Associative Memory with Fully Parallel Nearest-Manhattan-Distance Search for Low-Power Real-Time Single-Chip Applications," Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2004), pp. 543-544, (2004).

[56] H. Noda, K. Inoue, M. Kuroiwa, A. Amo, A. Hachisuka, H.J. Mattausch, T. Koide, S. Soeda, K. Dosaka, and K. Arimoto, "A 143MHz, 1.1W, 4.5Mb dynamic TCAM with hierarchical searching and shift redundancy architecture," IEEE International Solid-State Circuits Conference Digest of Tech. Papers (ISSCC'2004), pp.208-209, (2004).

[57] T. Inoue, T. Hironaka, T. Sasaki, S. Fukae, T. Koide, H.J. Mattausch, "A Proposition and Evaluation of a Bank-Based Multi-Port Memory with Blocking Network," Proceedings of the 2004 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC'2004), in press (2004).

[58] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, and T. Hironaka, "Low Power Bank-based Multi-port SRAM Design due to Bank Standby Mode," Proceedings of the 47th IEEE

International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press (2004).

[59] Y. Shirakawa, H.J. Mattausch, and T. Koide, “Reference-Pattern Learning and Optimization from an Input-Pattern Stream for Associative-Memory-Based Pattern-Recognition System,” Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press (2004).

[60] K. Kamimura, K. M. Rahman, H.J. Mattausch, and T. Koide, “Optimized Multi-Stage Minimum-Distance-Search Circuit with Feedback Stabilization for Fully-Parallel Associative Memories,” Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press (2004).

[61] K. Takemura, T. Koide, H.J. Mattausch, and T. Tsuji, “Analog-Circuit-Component Optimization with Genetic Algorithm,” Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press (2004).

[62] T. Morimoto, Y. Harada T. Koide, and H.J. Mattausch, “350nm CMOS Test-Chip for Architecture Verification of Real-Time QVGA Color-Video Segmentation at the 90nm Technology Node,” Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC‘2004), 531-532 (2004).

[63] O. Kiriyama, T. Morimoto, H. Adachi, Y. Harada, T. Koide and H.J. Mattausch, “Low-Power Design for Real-Time Image Segmentation LSI and Compact Digital CMOS Implementation,” Proceedings of the 2004 IEEE Asia-Pacific Conference on ASICs (AP-ASIC‘2004), in press (2004).

Beside COE Subject

I-3. Journal Papers

[64] S. Nakaya, T. Koide, S.Wakabayashi, "A VLSI floorplanning method based on an adaptive genetic algorithm,” The Transactions of Information Processing of Society Japan, Vol.43, No.5, pp.1361-1371, (2002) (in Japanese).

[65] S. Yamasaki, S. Nakaya, S. Wakabayashi, and T. Koide, "A Performance-Driven Floorplanning Method with Interconnect Performance Estimation,” IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E85-A, No.12, pp. 2775-2784, December (2002).

[66] S. Wakabayashi,.S. Koizumi, T. Koide, N. Imura, K. Fujiwara "A RISC Processor DLX-GA with Instruction Set Suitable for High-Speed Execution of a Genetic Algorithm,” The Transactions of Information Processing of Society Japan, Vol.44, No.2, pp.340-343 (2003) (in Japanese).

I-4. Proceedings of International Conferences

[67] H. Kubota, S. Wakabayashi, and T. Koide, “A Hierarchical Placement Method for Standard Cell Layout Based on Wire Length Driven Clustering,” Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press (2004).

II. Device Modeling

COE Subject

II-1. Journal Papers

[68] T. Okagaki, M. Tanaka, H. Ueno, and M. Miura-Mattausch, "Importance of Ballistic Carriers for the Dynamic Response in Sub-100nm MOSFETs," IEEE Electron Device Letters, Vol. 23, No. 3, pp. 154-156, (2002.3).

[69] Hans Juergen Mattausch, M. Suetake, D. Kitamaru, M. Miura-Mattausch, S. Kumashiro, N. Shigyo, S.Odanaka, and N. Nakayama, "Simple Nondestructive Extraction of the Vertical Channel-Impurity Profile of Small-Size Metal-Oxide-Semiconductor Field-Effect Transistors," Appl. Phys. Letters, Vol. 80, No. 16, pp. 2994-2996, (2002.4).

[70] H. Ueno, M. Tanaka, K. Morikawa, T. Takahashi, M. Miura-Mattausch, and Y. Omura, "Origin of Transconductance Oscillations in Silicon-on-Insulator Metal-Oxide-Semiconductor Field-Effect Transistors with an Ultrathin 6-nm-Thick Active Si Layer," J. Appl. Phys., Vol. 91, No. 8, pp. 5360-5364, (2002.4).

[71] H. Ueno, M. Tanaka, K. Morikawa, T. Takahashi, M. Miura-Mattausch, and Y. Ohmura, "Evidence of Mesoscopic Carrier Transport in SOI-MOSFETs with Ultra-Thin Active Si-Layer," Physica B, Vol. 314, pp. 367-371, (2002).

[72] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Circuit Simulation Models for Coming MOSFET Generations," IEICE Trans. Fund. Electron., Vol. E85-A, No. 4, pp. 740-747, (2002.4).

[73] K. Morikawa, H. Ueno, D. Kitamaru, M. Tanaka, T. Okagaki, M. Miura-Mattausch, Hans Juergen Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Quantum Effect in Sub-0.1um MOSFET with Pocket Technologies and Its Relevance for the On-Current Condition," Jpn. J. Appl. Phys., Vol. 41, No. 4B, pp. 2359-2362, (2002.4).

[74] H. Ueno, D. Kitamaru, K. Morikawa, M. Tanaka, M. Miura-Mattausch, H.J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Impurity-Profile-Based Threshold-Voltage Model of Pocket-Implanted MOSFETs for Circuit Simulation," IEEE Transactions on Electron Devices, 49[10], pp.1783-1789, (2002.10).

[75] S. Matsumoto, K. Hisamitsu, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Validity of Mobility Universality for Scaled Metal-Oxide-Semiconductor Field-Effect Transistors Down to 100nm Gate Length," J. Appl. Phys., 92[9], pp.5228-5232, (2002.11).

[76] D. Navarro, H. Kawano, K. Hisamitsu, T. Yamaoka, M. Tanaka, H. Ueno, M. Miura-Mattausch, H.J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Circuit-Simulation Model of Cgd Changes in Small-Size MOSFETs Due to High Channel-Field Gradients," IEICE Transactions on Electronics, E86-C[3], pp.474-480, (2003.3) (Invited).

[77] N. Nakayama, H. Ueno, T. Inoue, T. Isa, M. Tanaka, and M. Miura-Mattausch, “A Self-Consistent Non-Quasi Static MOSFET Model for Circuit Simulation Based on Transient CarrierResponse,” Jpn. J. Appl. Phys., 42[4B], pp.2132-2136, (2003.4).

[78] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, “100nm-MOSFET Model for Circuit Simulation: Challenges and Solutions,” IEICE Transactions on Electronics, E86-C[6], pp.1009-1021, (2003.6) (Invited).

[79] K. Konno, O. Matsushima, D. Navarro, and M. Miura-Mattausch, “Limit of Validity of the Drift-Diffusion Approximation for Simulation of Photodiode Characteristics,” Appl. Phys. Letters, Vol. 84, No. 8, pp. 1398-1400, (2004.2).

[80] N. Nakayama, D. Navarro, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, T. Kage, and S. Miyamoto, “Non-Quasi-Static Model for MOSFET Based on Carrier-Transit Delay,” IEE Electronics Letters, Vol.40, No. 4, pp.276-279. (2004.2).

[81] O. Matsushima, K. Konno, M. Tanaka, K. Hara, and Miura-Mattausch, “Carrier Transport in Highly Generated Carrier Concentration,” Semiconductor science and technology, Vol.19, No.4, S185-187. (2004.4).

[82] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch, “Complete Surface-Potential-Based Fully-Depleted Silicon-on-Insulator Metal-Oxide-Semiconductor Field-Effect-Transistor Model for Circuit Simulation,” Jpn. J. Appl. Phys., 43[4B], pp.L2166-2169, (2004).

II-2. Proceedings of International Conferences

[83] M. Miura-Mattausch, “The 100nm-MOSFET Model HiSIM and Its Extension to RF Applications,” Int. Sym. Quality Electronic Design, (San Jose), (2002.3) (Invited).

[84] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “HiSIM: Selft-Consistent Surface-Potential MOS-Model Valid Down to Sub-100nm Technologies,” Proc. Modeling and Simulation of Microsystems, pp. 678-681, (2002.4) (Invited).

[85] H. Kawano, M. Nishizawa, S. Matsumoto, S. Mitani, M. Tanaka, N. Nakayama, H. Ueno, M. Miura-Mattausch, and H. J. Mattausch, “A Practical Small-Signal Equivalent Circuit Model for RF-MOSFETs Valid Up to the Cut-Off Frequency,” IEEE Int. Microwave Sym. Digest, pp. 2121-2124, (2002.6).

[86] S. Jinbou, H. Ueno, H. Kawano, K. Morikawa, N. Nakayama, M. Miura-Mattausch, and H. J. Mattausch, “Analysis of Non-Quasisratic Contribution to Small-Signal Response for Deep Sub-*u*m MOSFET Technologies,” Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 26-27, (2002.9).

[87] N. Nakayama, H. Ueno, T. Isa, M. Tanaka, and M. Miura-Mattausch, “A Self-Consistent Non-Quasi Static MOSFET Model for Circuit Simulation Based on Transient Carrier Response,” Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 408-409, (2002.9).

[88] D. Navarro, K. Hisamitsu, T. Yamaoka, M. Tanaka, H. Kawano, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Circuit-Simulation Model of Gate-Drain-Capacitance Changes in Small-Size

MOSFETs Due to High Channel-Field Gradient," Proc. Int. Conf. Simulation Semicon. Processes & Devices, pp. 51-54, (2002.9).

[89] H. Ueno, S. Jinbou, H. Kawano, K. Morikawa, N. Nakayama, M. Miura-Mattausch, and H. J. Mattausch, "Drift-Diffusion-Based Modeling of the Non-Quasistatic Small-Signal Response for RF-MOSFET Applications," Proc. Int. Conf. Simulation Semicon. Processes & Devices, pp. 71-74, (2002.9).

[90] M. Miura-Mattausch, "HiSIM:MOSFET-Model for Circuit Simulation with Self-Consistent Surface Potential," Fabless-Semiconductor-Association Meeting, (San Jose), (2002.9) (Invited)

[91] M. Miura-Mattausch, H. Ueno, M. Tanaka, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "HiSIM: A MOSFET Model for Circuit Simulation Connecting Circuit Performance with Technology," Tech. Digest Int. Electron Devices Meeting, pp.109-112, (2002.12) (Invited).

[92] K. Hisamitusu, H. Ueno, M. Tanaka, D. Kitamaru, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. yamaguchi, K. Yamashita, and N. Nakayama, "Temperature-Independence-Point Properties for 0.1um-Scale Pocket-Implant Technologies and the Impact on Circuit Design," Proc. Of ASP-DAC, pp.179-183, (2003.1).

[93] M. Miura-Mattausch, D. Navarro, H. Ueno, S. Jinbou, H, J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, "HiSIM: Accurate Change Modeling Important for RF Era," Proc. Modeling and Simulation of Microsystems, Vol.2, pp258-261, (2003.2) (Invited).

[94] Q. Ngo, D. Navarro, T. Mizoguchi, S. Hosokawa, H. Ueno, M. Miura-Mattausch, and C. Y. Yang, "Gate Current Partitioning in MOSFET Models for Circuit Simulation," Proc. Modeling and Simulation of Microsystems, Vol.2, pp.322-325, (2003.2).

[95] T. Mizoguchi, H.J. Mattausch, H. Ueno, D. Kitamaru, K. Hisamitsu, M. Miura-Mattausch, S. Itoh, and K. Morikawa, "Extraction of Inter-and Intra-Chip Device-Parameter Variations with a Differential-Amplifier-Stage Test Circuit," SASIMI 2003 Proceedings(1-8), pp.76-82, (2003.4).

[96] O. Matsushima, M. Tanaka, H. Ueno, K. Hara, K. Konno, and M. Miura-Mattausch, "Carrier Transport in Highly Generated Carrier Concentration," Proc. Int. Conf. Nonequilibrium Carrier Dynamics in Semiconductors, pp. PTu4-8, (2003.7).

[97] S. Hosokawa, Y. Shiraga, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, H. Masuda, and S. Miyamoto, "Origin of Enhanced Thermal Noise for 100nm-MOSFETs," Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 20-21, (2003.9).

[98] D. Kitamaru, Y. Uetsuji, and M. Miura-Mattausch, "A Complete Surface-Potential-Based SOI-MOSFET Model for Circuit Simulation,", Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 622-623, (2003.9).

[99] H. Ueno, S. Matsumoto, S. Hosokawa, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Modeling of 1/*f* Noise with HiSIM for 100nm CINS Technology," Proc. On the 1st International Workshop on Compact Modeling, pp.18-23, (2004.1).

[100] M. Miura-Mattausch, “MOSFET Modeling for RF-CMOS Design,” Proc. Asia and South Pacific Design Automation Conference 2004, 6A-1, pp.482-490. (2004.1) (Invited).

[101] M. Miura-Mattausch, S. Hosokawa, D. Navarro, S. Matsumoto, H. Ueno, H. J. Mattausch, T. Ohguro, T. Iizuka, T. Taguchi, and S. Miyamoto, “Noise Modeling with HiSIM Based on Self-Consistent Surface-Potential Description,” Nanotech 2004 Conference Technical Proc., Vol. 2. pp.66-69. (2004.3) (Invited).

[102] M. Miura-Mattausch, S. Matsumoto, K. Mizoguchi, D. Miyawaki, H. J. Mattausch, S. Itoh, and K. Morikawa, “Test Circuits for Extracting Sub-100nm MOSFET Technology Variations with the MOSFET Model HiSIM,” Proc. IEEE 2004 Int. Conference on Microelectronic Test Structures, Vol.17, No. 9.1, pp.267-272. (2004.3) (Invited).

II-3. Books

[103] M. Miura-Mattausch, H. Ueno, “Device Model and Its Applications for Circuit Simulation,” Oyobuturi, Vol.71, pp. 726-730, (2002.6).

[104] M. Miura-Mattausch,T. Myouno,K. Mori, “Circuit-Simulation Techniques and MOSFET Modeling,” Sipec, (2003.3).

Beside COE Subject

II-4. Journal Papers

[105] M. Tanaka, H. Ueno, O. Matsushima, and M. Miura-Mattausch, “High-Electric-Field Electron Transport at Silicon/Silicon-Dioxide Interface Inversion Layer,” Jpn., J. Appl. Phys., 42[3B], pp.L280-282, (2003.3).

II-5. Proceedings of International Conferences

[106] S. Ito, K. Morikawa, A. Kobayashi, H. Masuda, S. Fujimoto, T. Mizoguchi, H. Ueno, and M. Miura-Mattausch, “Parameter Extraction of HiSIM1.1/HiSIM1.2,” JPSJ Symposium Series Vol. 2003, No.11, (DA Symposium 2003), pp.247-252. (2003.7).

III. Nanodevices and Processing

COE Subject

III-1. Journal Papers

[107] K. Shibahara, "Ultra-Shallow Junction Formation with Antimony Implantation,” IEICE Trans. Electron., E.85-C, pp. 1091-1097 (2002).

[108] S. Miyazaki, H. Takahashi, H. Yamashita, M. Narasaki and M. Hirose, "Growth and

Characterization of Microcrystalline Silicon-Germanium Films" J. Non-Cryst. Solid 299-302 Part I, 148-152 (2002).

[109] S. Miyazaki, M. Narasaki, M. Ogasawara and M. Hirose, "Chemical and Electronic Structure of Ultrathin Zirconium Oxide Films on Silicon as Determined by Photoelectron Spectroscopy," Solid State Electronics, 16, 1679-1685 (2002).

[110] S. Miyazaki, "Characterization of High-k Gate Dielectric/Silicon Interfaces," Appl. Surf. Sci. 190, 66-74 (2002).

[111] H. Murakami, T. Mihara, S. Miyazaki and M. Hirose, "Carrier Depletion Effect in the n^+ Poly-Si Gate Side-Wall/SiO_2 Interfaces as Evaluated by Gate Tunnel Leakage Current," Jpn. J. Appl. Phys. 41, L512-L514 (2002).

[112] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "High Transmission Gain Integrated Antenna on Extremely High Resistivity Si for ULSI Wireless Interconnect," IEEE Electron Device Letters, Vol. 23, No.12, December, pp.731-733 (2002).

[113] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, "NH_3-annealed atomic-layer-deposited silicon nitride as a high-*k* gate dielectric with high reliability," Appl. Phys. Lett. 80, pp.1252-1254 (2002).

[114] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Low thermal-budget ultrathin NH_3-annealed atomic-layer-deposited Si-nitride/SiO_2 stack gate dielectrics with excellent reliability," IEEE Electron Device Lett. 23, pp. 179-181 (2002).

[115] K. Kawamura, T. Kidera, A. Nakajima, and S. Yokoyama, "Coulomb blockade effects and conduction mechanism in extremely thin polycrystalline-silicon wires," J. Appl. Phys. 91, pp. 5213-5220 (2002).

[116] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Reliable extraction of the energy distribution of Si/SiO_2 interface traps in ultrathin metal-oxide-semiconductor structures," Appl. Phys. Lett. 80, pp. 3952-3954 (2002).

[117] Y. Ito, T. Hatano, A. Nakajima, and S. Yokoyama, "Fabrication of Si single-electron transistors having double SiO_2 barriers," Appl. Phys. Lett. 80, pp. 4617-4619 (2002).

[118] A. Nakajima, Y. Ito, and S. Yokoyama, "Conduction mechanism of Si single-electron transistors having an one-dimensional regular array of multiple tunnel junctions," Appl. Phys. Lett. 81, pp. 733-735 (2002).

[119] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "High quality NH_3-annealed atomic Layer Deposited Si-nitride/SiO_2 Stack Gate Dielectrics for Sub-100nm Technology Generations," Solid State Electron. 46, pp. 1659-1664 (2002).

[120] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, "Low-temperature formation of highly-reliable silicon-nitride gate dielectrics with suppressed soft-breakdown phenomena for advanced complementary metal-oxide-semiconductor technology," J. Vac. Sci. & Technol. B 20, pp. 1406-1409 (2002).

[121] A. Nakajima, T. Kidera, H.Ishii, and S. Yokoyama, "Atomic-layer deposition of ZrO_2 with a Si nitride barrier layer," Appl. Phys. Lett. 81, pp. 2824-2826 (2002).

[122] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Response to "Comment on 'Reliable extraction of the energy distribution of Si/SiO_2 interface traps in ultrathin metal-oxide-semiconductor structures'" [Appl. Phys. Lett. 81, 3681 (2002)].

[123] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, and S. Yokoyama, "Atomic-layer-deposited silicon-nitride/SiO_2 stack ---- a highly potential gate dielectrics for advanced CMOS technology," Microelectronics Reliability 42, pp.1823-1835 (2002) (Introductory Invited).

[124] T. Yoshino, S. Yokoyama and T. Fujii, "Influence of Organic Contaminant on Trap Generation in Thin SiO_2 of Metal-Oxide-Semiconductor Capacitors," Jpn. J. Appl. Phys. 41, No. 7A, pp.4750-4753 (2002).

[125] S. Yokoyama, T. Yoshino, Shibahara, A. Nakajima, T. Kikkawa, and H. Sunami, "Influence of Wafer Storage Environment on MOS Device Characteristics," J. Aerosol Research, Japan 17, No. 2, ,pp. 96-104 (2002) [in Japanese].

[126] T. Furukawa, H. Yamashita, and H. Sunami, "A Proposal of Corrugated-Channel Transistor (CCT) with Vertically-Formed Channels for Area-Conscious Applications," Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2067-2072, April 2003.

[127] A. Takase, T. Kidera, and H. Sunami, "Field-Shield Trench Isolation with Self-Aligned Field Oxide," Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2100-2105, April 2003.

[128] H. Sunami, "Prospect of ULSI and Requirement to Polymer" , Polymer,Vol.52, Aug., pp. 546-550,(2003).

[129] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, " Multiple-Step Electron Charging in Silicon-Quantum- Dot Floating Gate Metal-Oxide-Semiconductor Memories," Jpn. J. Appl. Phys. 42 ,4134-4137 (2003).

[130] Y. Darma, R. Takaoka, H. Murakami and S. Miyazaki, "Self-Assembling Formation of Silicon Quantum Dots with a Germanium Core by Low- Pressure Chemical Vapor Deposition," Nanotechnology, 14,413-415 (2003).

[131] Y. Darma, H. Murakami and S. Miyazaki, "Formation of Nanometer Silicon Dots with Germanium Core by Highly-Slective Low-Pressure Chemical Vapor Deposition," Jpn. J. Appl. Phys. 42, 6B, 4129-4133 (2003).

[132] N. Kosku, F. Kurisu, M. Takegoshi, H. Takahashi and S. Miyazaki, "High-Rate Deposition of Highly Crystallized Silicon Films from Inductively Coupled Plasma," Thin Solid Films, 435, 39-43 (2003).

[133] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "Characteristics of Integrated Antenna on Si for On-Chip Wireless Interconnect," Japanese Journal of Applied Physics, Vol. 42, No. 4B, April, pp. 2204-2209 (2003).

[134] Y. Hara, S. Yokoyama and K. Umeda, "Compact Branched Optical Waveguides Using High-Index-Contrast Stacked Structure," Optical Review 10, No. 5, pp. 357-360 (2003).

[135] S. Miyazaki, M. Narasaki A. Suyama M. Yamaoka and H. Murakami, "Electronic Structure and Energy Band Offsets for Ultrathin Silicon Nitride on Si(100)," Appl. Surf. Sci. 216,252-257 (2003).

[136] M. Yamaoka, H. Murakami and S. Miyazaki, "Diffusion and Incorporation of Zr into

Thermally-Grown SiO_2 on Si(100),” Appl. Surf. Sci., 216,223-27 (2003).

[137] A. Nakajima, Q.D.M. Khosru, T. Kasai, and S. Yokoyama, "Carrier Mobility in p-MOSFET with Atomic-Layer-Deposited Si-Nitride/SiO_2 Stack Gate Dielectrics," IEEE Electron Device Lett. 24, pp. 472-474 (2003).

[138] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kasai, and S. Yokoyama, "High Quality Atomic-Layer-Deposited Ultrathin Silicon-Nitride Gate Dielectrics with Low Density of Interface and Bulk Traps," Appl. Phys. Lett. 83, pp. 335-337 (2003).

[139] Q.D.M. Khosru, S. Yokoyama, A. Nakajima, K. Shibahara, T. Kikkawa, H. Sunami, and T. Yoshino, "Organic Contamination Dependence of Process-Induced Interface Trap Generation in Ultrathin Oxide Metal Oxide Semiconductor Transistors," Jpn. J. Appl. Phys. 42, pp. L1429-L1432 (2003).

[140] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, “Evaluation of Surface Contamination by Noncontact Capacitance Method under UV Irradiation,” Jpn. J. Appl. Phys. 42, No. 9A, pp.5837-5843 (2003).

[141] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, “Investigation of Surface Contamination on Silicon Oxide after HF Etching by Noncontact Capacitance Method,” Jpn. J. Appl. Phys. 42, pp, 7601-7602 (2003).

[142] H. Sunami, T. Furukawa, and T. Masuda, “A Three-Dimensional MOS Transistor Formation Technique with Crystallographic Orientation-Dependent TMAH Etchant,” SENSORS and ACTUATORS A: PHYSICAL, A111, pp. 310-316, 2004.

[143] A. Katakami, K. Kobayashi, and H. Sunami, “A High-Aspect Ratio Silicon Gate Formation Technique for Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation,” Jpn. J. Appl. Phys., Vol. 43, No. 4B, pp. 2145-2150, April 2004.

[144] Y. Darma, H. Murakami and S. Miyazaki, "Influence of Thermal Annealing on Compositional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core", Appl. Surf. Sci. 224 ,156-159 (2004).

[145] W. Mizubayashi, Y. Yoshida, H. Murakami, S. Miyazaki and M. Hirose, "Statistical Analysis of Soft and Hard Breakdown in 1.9-4.8nm-thick Gate Oxides,” IEEE Electron Device Lett. in press (2004).

[146] A. Ohta, M. Yamaoka and S. Miyazaki, "Photoelectron Spectroscopy of Ultrathin Yttrium Oxide Films on Si(100)", Microelec. Eng., 72,154-159 (2004).

[147] S. Watanabe, A.B.M.H. Rashid and T. Kikkawa, “Effect of High Resistivity Si substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects,” Japanese Journal of Applied Physics Vol. 43, No. 4B, pp.2297-2301(2004).

[148] A.B.M.H. Rashid, S. Watanabe and T. Kikkawa, “Characteristics of Si Integrated Antenna for Inter-Chip Wireless Interconnection,” Japanese Journal of Applied Physics Vol. 43, No. 4B, pp.2283-22287(2004).

[149] H. Setyawan, M. Shimada, Y. Hayashi, K. Okuyama and S. Yokoyama, “Particle Formation and Trapping Behavior in a TEOS/O_2 Plasma and Their Effects on Contamination of a Si Wafer,” Aerosol Science and Technology 38, No. 2, pp. 120-127 (2004).

[150] H. Ishii, A. Nakajima, and S. Yokoyama, "Growth and electrical properties of atomic-layer deposited ZrO_2/Si-nitride stack gate dielectrics," J. Appl. Phys. 95, pp.536-542 (2004).

[151] T. Kitade and A. Nakajima, "Application of highly doped Si single-electron transistors to an exclusive-NOR operation," Jpn. J. Appl. Phys. 43, pp. L418-L420 (2004).

[152] M. Ooka and S. Yokoyama, "Excellent Contact-Hole Etching with NH_3 Added C_5F_8 Pulse-Modulated Plasma," Jpn. J. Appl. Phys. 43 (2004) (in press).

III-2. Proceedings of International Conferences

[153] T. Amada, N. Maeda and K. Shibahara, "Degradation in a Molybdenum-Gate MOS Structure Caused by N^+ Ion Implantation for Work Function Control," Mat. Res. Soc. Symp. Proc., 716, pp. 299-314 (2002).

[154] A. Matsuno, K. Kagawa, Y. Niwatsukino, T. Nire and K. Shibahara, "Pulse Duration Effects on Laser Anneal Shallow Junction," Proc. of the 2nd Int. Semiconductor Tech. Conf. (ISTC2002), 2002-17, pp. 148-156 (2002).

[155] N. Maeda, D. Onimatsu, Y. Ishikawa and K. Shibahara, "Gate-Extension Overlap Control by Sb Tilt Implantation," Proc. of the 2nd Int. Semiconductor Tech. Conf. (ISTC2002), 2002-17, pp. 165-171 (2002).

[156] K. Kagawa, Y. Niwatsukino, M. Matsuno and K. Shibahara, "Influence of Pulse Duration on KrF Excimer Laser Annealing Process for Ultra Shallow Junction Formation," Int. Workshop on Junction Tech. (IWJT'02), pp. 31-34 (2002).

[157] K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matsuno and K. Shibahara, "Formation of Low-Resistive Ultra-Shallow n^+/p Junction by Heat-Assisted Excimer Laser Annealing," Int. Workshop on Junction Tech. (IWJT'02), pp. 35-36 (2002).

[158] H. Sunami, T. Furukawa, and T. Masuda, "Orientation-Dependent Anisotropic TMAH Etchant Applied to 3-D Silicon Nanostructure Formation," Proc. Pacific Rim Workshop on Transducers and Micro/nano Technologies, pp. 367-372, Xiamen, July 22-24, (2002).

[159] T. Furukawa, H. Yamashita, and H. Sunami, "Corrugated-Channel Transistor (CCT) for Area-Conscious Applications," Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. A-3-2, pp. 139-140, Nagoya, Sept. 17-19, (2002).

[160] A. Takase, T. Kidera, and H. Sunami, "Field-Shield Trench Isolation with Self-Aligned Field Oxide," Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. A-7-4, pp. 694-695, Nagoya, Sept. 17-19, (2002).

[161] S. Miyazaki, "Characterization of Ultrathin Gate Dielectrics on Silicon by Photoelectron Spectroscopy," Proc of 2001 MRS Workshop Series - Alternatives on to SiO_2 as Gate Dielectric for Future Si-Based Microelectronics, pp. 8.1-8.7 (2002).

[162] Y. Darma, H. Murakami and S. Miyazaki, "Formation of Nanometer Silicon Dots with Germanium Core by Highly-Selective Low-Pressure Chemical Vapour Deposition," Dig. of Papers of Int. Microprocesses and Nanotechnology Conf. ,pp. 58-59 (Tokyo, Nov. 6-8, 2002).

[163] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, "Multiple-Step Electron Charging in

Si Quantum-Dot Floating Gate MOS Memories," Dig. of Papers of Intern. Microprocesses and Nanotechnology Conf., pp. 116-117 (Tokyo, Nov. 6-8, 2002).

[164] Y. Darma, R. Takaoka, H. Murakami and S. Miyazaki, "Self-Assembling Formation of Silicon Quantum Dot with Germanium Core by LPCVD," Proc of 2002 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, pp. 307-310 (Sapporo, July 1-3, 2002). .

[165] N. Kosku, F. Kurisu, M. Takegoshi, H. Takahashi and S. Miyazaki, "High-rate Deposition of Highly- crystallized Silicon Films from Inductively-coupled Plasma," Abst. of Joint Intern. Plasma Symp. of 6th APCPST, 15th SPSM, and 11th KAPRA, p. 131 (Cheju, July 1-4, 2002).

[166] S. Miyazaki, H. Takahashi, M. Sagara and M. Hirose, "Growth and Characterization of Amorphous and Microcrystalline Silicon-Germanium Films," 2002 MRS Spring Meeting, A18.1 (San Francisco, April 4, 2002) (Invited).

[167] N. Kosku, F. Kurisu, H. Takahashi and S. Miyazaki, "High-rate Deposition of Highly-Crystallized Silicon Films from Inductively-coupled Plasma," Extended Abst. of The 5th SANKEN Intern. Symp., pp.52-53 (Osaka, March 14, 2002).

[168] S. Miyazaki and H. Murakami, "Characterization of Deposition Process of Microcrystalline Silicon- Germanium Films: In-situ Infrared Attenuated Total Reflection and Ex-situ Raman Scattering Studies," Extended Abst. of The 5th SANKEN Intern. Symp., pp.65-66 (Osaka, March 14, 2002) (Invited).

[169] S. Miyazaki, M. Narasaki and H. Murakami, "Electronic Structure and Energy Band Offsets for Ultrathin Silicon Nitride on Si(100)," Abst of 4th Intern. Symp. on Control of Semiconductor Interfaces, A5-3 (Karuizawa, Oct. 21-25, 2002).

[170] M. Yamaoka, H. Murakami and S. Miyazaki, "Diffusion and Incorporation of Zr into Thermally-Grown SiO_2 on Si(100)", Abst. of 4th Intern. Symp. on Control of Semiconductor Interfaces, A4-3 (Karuizawa, Oct. 21-25, 2002).

[171] A. Suyama, H. Yokoi, M. Narasaki, W. Mizubayashi, H. Murakami and S. Miyazaki, "Photoemission Study of Aluminum Oxynitride/Si(100) Heterostructures- Chemical Bonding Features and Energy Band Lineup," Extended Abst. of Int. Conf. on Solid State Devices and Materials, pp.760-761 (Nagoya, Sept. 17-19, 2002).

[172] H. Murakami, W. Mizubayashi, H. Yokoi, A. Suyama and S. Miyazaki, "Electrical Characterization of Aluminum-Oxynitride Stacked Gate Dielectrics Prepared by a Layer-by-Layer Process of Chemical Vapor Deposition and Rapid Thermal Nitridation," Extended Abst. of Int. Conf. on Solid State Devices and Materials, pp. 712-713 (Nagoya, Sept. 17-19, 2002).

[173] M. Ichioka, S. Miyazaki, M. Taniguchi, H. Namatame, A. Kimura and H. Sato, "Characterization on As^+ Heavily-Implanted Layer on Si(100) by X-ray Photoelectron Spectroscopy," Abst. of 6th Hiroshima Int. Symp. on Synchrotron Radiation, P-11 (Higashi-Hiroshima, March 14, 2002).

[174] S. Miyazaki, "Self-Assembling of Si Quantum Dots and Their Application to Memory Devices," Int. Conf. on Polycrystalline Semiconductors, I05 (Nara, Sept. 10-13, 2002). (Invited).

[175] S. Miyazaki, “Self-Assembling of Si quantum Dots and Their Application to Memory Devices,” 2nd Vacuum & Surf. Sci. Conf. of Asia and Australia, Mo7 (Hong Kong, Aug. 26-30, 2002) (Invited).

[176] ABM H. Rashid, S. Watanabe, T. Kikkawa, X. Guo, and K. O, "Interference suppression of wireless interconnecton in Si integrated antenna," Proc. International Interconnect Technology Conference, 173-175 (IEEE, San Francisco, USA, June 3-5, 2002).

[177] S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, "Influence of Si Substrate Ground on Antenna Transmission Gain for on-chip Wireless Interconnects," Abst. Advanced Metallization for ULSI Application, pp. 94-95, Conference Proceedings, pp.543-548(2002).

[178] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "Wireless Interconnection on Si using Integrated Antenna,” Proceedings of 2002 International Conference on Solid State Devices and Materials, pp.648-649 (Nagoya, Japan, September, 2002).

[179] M. Ooka and S. Yokoyama, “Ultrasmall SiO_2 Hole Etching using PFC Alternative Gas with Small Global Greenhouse Effect,” Digest of Pacific Rim Workshop on Transducers and Micro/Nano Technologies, pp. 111-114 (MEMS2002) (2002).

[180] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, "Evaluation of Surface Contamination by Noncontact Capacitance Method under UV Irradiation," Extend. Abst. Int. Conf. on Solid State Devices and Materials, pp. 724-725 (SSDM2002) (2002).

[181] A. Nakajima and S. Yokoyama, "Atomic-layer-deposition of Si nitride and ZrO_2 for gate dielectrics," Abst. AVS Topical Conference on Atomic Layer Deposition, pp. 6-6 (ALD 2002) (Seoul, August 19-21, 2002) (Invited).

[182] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "A novel method for extracting the energy distribution of Si/SiO_2 interface traps in ultrathin oxide MOS structures," presented in the Second IEEE Conference on Nanotechnology (Washington, D.C., August 26-28, 2002).

[183] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "Time-dependent breakdown of ultrathin SiO_2 gate dielectrics under static and dynamic stress," Abst. 2nd ECS Int. Semiconductor Technology Conf. , Abstract No.71 (Tokyo, September 11-14, 2002).

[184] H. Ishii, T. Kidera, A. Nakajima, and S. Yokoyama, "Atomic-layer deposition of ZrO_2 with a Si nitride barrier layer," 2002 Int. Conf. on Solid State Devices and Materials, pp. 452-453 (Nagoya, September 17-19, 2002).

[185] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "A comparative study of bulk and interface trap generation in ultrathin SiO_2 and atomic-layer-deposited Si-nitride/SiO_2 stack gate dielectrics," Fourth Int. Symposium on Control of Semiconductor Interface (ISCSI-IV) ,pp. A6-3-A6-3 (Karuizawa, October 21-25, 2002).

[186] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "An Effective Method for Obtaining Interface Trap Distribution in MOS capacitors with Tunneling Gate Oxides,” Proceedings 2002 IEEE Int. Conf. on Semiconductor Electronics (ICSE 2002) ,pp. 402-406 (Penang, December 19-21, 2002).

[187] K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno and K. Shibahara, "Defect Density Reduction and Sheet Resistance Improvement by Multi-Pulse KrF-Excimer-Laser Annealing,” Ext. Abst. Fabrication, Characterization, and Modeling of Ultra-Shallow

Doping Profiles in Semiconductors (USJ 2003), pp. 98-103 (2003).

[188] M. Hino, T. Amada, N. Maeda and K. Shibahara, "Influence of Nitrogen Profile on Metal Workfunction in Mo/SiO_2/Si MOS Structure," Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 494-495 (2003).

[189] K. Shibahara, K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino and A. Matsuno, "KrF Excimer Laser Annealing For Ultra Shallow Junction Formation: Approach For Irradiation Energy Density Reduction," Ext. Abst. 11th Int. Conf. on Adv. Thermal Processing of Semiconductors (RTP 2003), pp. 13-16 (2003).

[190] A. Katakami, K. Kobayashi, and H. Sunami, "High-Aspect Ratio gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced oxidation of Silicon Gate," Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. D-5-2, pp. 282-283, Tokyo, Sept. 16-18, (2003).

[191] K. Takeuchi, H. Murakami and S. Miyazaki, "Electronic Charging State of Si Quantum Dots formed on Ultrathin SiO_2 as Evaluated by AFM/Kelvin Probe Method," Proc. of ECS Int. Semicond. Technol. Conf., pp.1-8 (2003).

[192] M. Yamaoka, M. Narasaki, H. Murakami and S. Miyazaki, "Photoemission Study of Ultrathin Hafnium Oxide Films Evaporated on Si(100)," Proc. of ECS Int. Semicond. Technol. Conf., pp. 229-236 (2003).

[193] S. Miyazaki, H. Yamashita, H. Nakagawa and M. Yamaoka, "Photoemission Study of Interfacial Oxidation in ZrO_2/Sub-Nanometer $SiON_x$/Si(100) Stacked Structures," Mat. Res. Soc. Symp. Proc. 747, 281-286 (2003).

[194] A.Sakai, S. Sakashita, M. Sakashita, S. Zaima, Y. Yauda and S. Miyazaki, "Praseodymium Silicate Formation by Post-Growth High Temperature Annealing," Fall Meetings of Mat. Res. Soc., E3.23 (Boston Dec. 1-5, 2003).

[195] H. Nakagawa, A. Ohta, F. Takeno, H. Murakami and S. Miyazaki, "Characterization of Interfacial Oxide Layers in Heterostructures of Zirconium Oxides Formed on Si(100) and NH3-nitrided Si(100) surfaces," Abst. of 7th Int. Conf. on Atomically Controlled Surfaces, Interfaces and Nanostructures ,p. 253 (Nara, Nov. 16-20, 2003).

[196] A. Ohta, S. Miyazaki, H. Murakami, T. Kawahara and K. Torii, "Characterization of Dielectric Stack Structures of Hafnium Aluminate and Silicon Dioxide formed on Si(100)," Abst. of 7th Int. Conf. on Atomically Controlled Surfaces, Interfaces and Nanostructures, p. 255 (Nara, Nov. 16-20, 2003).

[197] S. Miyazaki, "Photoemission Study of High-k Gate Dielectric/Si(100) Heterostructures - Chemical Bonding Features and Energy Band Alignment," Abst. of American Vacuum Society 50th Inter. Symp. and Exhibition, DI-MoM7 (Baltimore U.S.A, Nov. 3, 2003) (Invited).

[198] M. Yamaoka, A. Ohta and S. Miyazaki, "Characterization of Hafnium Diffusion into Thermally-Grown SiO_2 on Si(100)," Extended Abst. of 2003 Int. Conf. on Solid State Devices and Materials, pp. 810-811 (Tokyo, Sept. 16-18, 2003).

[199] Y. Darma and S. Miyazaki, "Characterization of Electronic Transport Through Si Dot with Ge Core Using AFM Conducting Probe," Dig. of Papers of 2003 International Microprocesses and Nanotechnology Conference, pp. 22-23 (Tokyo, Oct. 29-31, 2003).

[200] M. Ikeda, Y. Shimizu, T. Shibaguchi, H. Murakami and S. Miyazaki, “Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs,” Extended Abst. of 2003 Int. Conf. on Solid State Devices and Materials, pp. 846-847 (Tokyo, September 16-18, 2003).

[201] Y. Darma, K. Takeuchi and S. Miyazaki, “Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by AFM/Kelvin Probe Technique,” Extended Abst. of 2003 International Conference on Solid State Devices and Materials, pp. 300-301 (Tokyo, September 16-18, 2003).

[202] Y. Darma and S. Miyazaki, “Thermal Stability of Nanometer Dot Consisting of Si Clad and Ge Core as Detected by Raman and Photoemission Spectroscopy,” Proc of 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, pp. 145-149 (Busan, June 30-July 2, 2003).

[203] T. Shibaguchi, Y. Shimizu, M. Ikeda, H. Murakami and S. Miyazaki, “Analysis of Charging Characteristics in MOSFETs with a Si-Quantum-Dots Floating Gate,” Prod of 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, pp. 151-154 (Busan, June 30-July 2, 2003).

[204] Y. Darma, H. Murakami and S. Miyazaki, “Influence of Thermal Annealing on Compositional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core,” Extended Abst. of 1st Intern. SiGe Technology and Device Meeting, pp. 209-210 (Nagoya, Jan. 15-17, 2003).

[205] K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki, “Local Characterization of Electronic Transport in Microcrystalline Germanium Thin Films by Atomic Force Microscopy Using a Conducting Probe,” Proc. of 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, pp. 37-40 (Busan, June 30-July2, 2003).

[206] K. Makihara, K. Takeuchi, M. Ikeda, H. Murakami and S. Miyazaki" Characterization of Nucleation and Growth of Ge Microcrystallites by AFM (Atomic Force Microscopy) with a Conducting Probe,” Proc of 20th Symposium on Plasma Processing, pp.321-322 (Nagaoka, Jan. 29-31, 2003).

[207] N. Kosku and S. Miyazaki, “Microcrystalline Silicon Films Form Inductively-coupled Plasma,” Proc of 20th Symposium on Plasma Processing, pp.319-320 (Nagaoka, Jan. 29-31, 2003).

[208] A. Ohta, M. Yamaoka and S. Miyazaki, “Photoelectron Spectroscopy of Ultrathin Yttrium Oxide Films on Si(100),” Abst. of 13th Bi-annual Conf. on Insulating Films on Semiconductors, GS20 (Barcelona, June 18-20, 2003).

[209] A. Ohta, M. Yamaoka, S. Miyazaki, A. Ino, M.Taniguchi, H Namatame, M. Nakatake, A. Kimura and H. Sato, “Photoelectron Spectroscopy of Ultrathin Yttrium Oxide Films on Silicon,” Abst. of 7th Hiroshima Int. Symp. on Synchrotron Radiation, p.218 (Higashi-Hiroshima, March 13-14, 2003).

[210] T. Kikkawa, A.B.M. H. Rashid, and S.Watanabe, “Effect of silicon substrate on the transmission characteristics of integrated antenna,” Proc. 2003 IEEE Topical Conference on Wireless Communication Technology, Honolulu,, Oct. 15-17, S06P09, 2003.

[211] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, “Crosstalk Isolation of Monopole

Integrated Antenna on Si for ULSI Wireless Interconnect," Proceedings of 2003 IEEE International Interconnect Technology Conference, 2-4 June, pp.156-158 (2003, SanFrancisco, USA).

[212] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "Inter-chip Wireless Interconnection using Si Integrated Antenna," Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 394-395, Tokyo, Sept. 16-18, (2003).

[213] T. Kitade, K. Ohkura, and A. Nakajima, "Periodic Coulomb oscillation in highly doped Si single-electron transistor," 2003 Int. Conf. on Solid State Devices and Materials (SSDM2003), pp. 584-585 (Tokyo, September 16-18, 2003).

[214] M. Ooka and S. Yokoyama, "Excellent Contact-Hole Etching with NH_3 Added C_5F_8 Pulse-Modulated Plasma," Extend. Abst. Int. Conf. on Solid State Devices and Materials (SSDM2003), pp. 454-455 (2003).

[215] A. Nakajima, H. Ishii, T. Kitade, and S. Yokoyama, "Atomic-Layer-Deposited Ultrathin Si-Nitride Gate Dielectrics ---A Better Choice for Sub-tunneling Gate Dielectrics---," Technical Digest of the 2003 IEEE International Electron Devices Meeting,pp.657-660 (Washington, D.C., Dec. 8-10, 2003).

[216] K. Torii, T. Aoyama, S. Kamiyama, T. Tamura, S. Miyazaki, H. Kitajima, T. Arikado, "Dielectric Breakdown Mechanism of HfSiON/SiO_2 Gate Dielectric," 2004 Symp. on VLSI Technol. 11.4 (Honolulu, June 15-17, 2004).

[217] H. Nakagawa, A. Ohta, F. Takeno, S. Nagamachi, H. Murakami, S. Higashi, S. Miyazaki, "Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on NH_3-nitrided Si(100)," Extended Abst. of 2004 Int. Workshop on DIELECTRIC THIN FILMS FOR FUTURE ULSI DEVICES: SCIENCE AND TECHNOLOGY, pp. 35-36 (Tokyo, May 26-28, 2004).

[218] A. Ohta, S. Miyazaki, H. Murakami, T. Kawahara and K. Torii, "Impact of Rapid Thermal O_2-Anneal on Dielectric Stack Structures of Hafnium Aluminate and Silicon Dioxide Formed on Si(100)," Extended Abst. of 2004 Int. Workshop on DIELECTRIC THIN FILMS FOR FUTURE ULSI DEVICES: SCIENCE AND TECHNOLOGY, pp. 97-98 (Tokyo, May 26-28, 2004).

[219] K. Makihara, H. Deki, H. Murakami, S. Higashi and S. Miyazaki, "Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment," 12th Abst. of 12th Int. Conf. on Solid Films and Surfaces (Hamamatsu, June 21-25, 2004).

[220] H. Kaku, S. Higashi, H. Taniguchi, H. Murakami and S. Miyazaki, "A New Crystallization Technique of Si Flms on Glass Substrate Using Thermal Plasma Jet," Abst. of 12th Int. Conf. on Solid Films and Surfaces (Hamamatsu, June 21-25, 2004).

[221] N. Kosku, H. Murakami, S. Higashi and S. Miyazaki, "Influence of Substrate DC Bias on Crystallinity of Si Films Grown at a High Rate from Inductively-Coupled Plasma CVD," Abst. of 12th Int. Conf. on Solid Films and Surfaces (Hamamatsu, June 21-25, 2004).

[222] Y. Okamoto, K. Makihara, S.Higashi and S.Miyazaki, "Formation of Microcrystalline Germanium (μc-Ge:H) Films from Inductively-Coupled Plasma CVD," Abst. of 12th Int. Conf. on Solid Films and Surfaces (Hamamatsu, June 21-25, 2004).

[223] S. Miyazaki, "Charging/Discharging Characteristics of Silicon Quantum Dots and Their

Application to Memory Devices," Joint Conf. of 7th Int. Conf. on Advanced Surf. Eng. and 2nd Int. Conf. on Surf. and Interface Sci. and Eng., p. 138 (Guangzhou, May 14-16, 2004) (Invited).

[224] S. Yokoyama, "Fabrication Technology for 26 nm Si MOS Transistors," The 1st International Workshop on Nanoscale Semiconductor Devices, pp.105-124 (Seoul, May 18-19, 2004) (Invited).

[225] A. Nakajima and S. Yokoyama, "Atomic-layer-deposition of ultrathin Si Nitride for sub-tunneling gate dielectrics---," to be presented at ECS Symposium I1: First International Symposium on Dielectrics for Nanosystems (Honolulu, Hawaii, October 3-8, 2004) (Invited).

III-3. Books

[226] S. Yokoyama、T. Fujii, "Design,Operation and Maintenance of Clean Room," Chapter11. Section 1, Joho Kiko Co.,(2002. 10) pp.211-222, (in Japanese).

[227] S. Miyazaki, "Hand book for Thin Film Formation and Application, 21st Century Edition," N・T・S(2003)：Coauthor, Chapter2. Section 3.(pp. 384-393) (in Japanese).

[228] S. Miyazaki, "Thin Film Engineering," Maruzen(2003)：Coauthor, 2.3(pp. 95-118)(in Japanese).

[229] M. Hirose, S. Miyazaki, "Fundamentals of Super Lattice," CMC Publishers (2003)：Coauthor, Chapter3.pp. 143-155 (in Japanese).

[230] A. Nakajima, "Silicon Quantum Dots," Encyclopedia of Nanoscience and Nanotechnology (H.S. Nalwa (ED.), American Scientific Publishers, USA) Vol. 9, pp. 837-857, 2004. ISBN:1-58883-001-2.

Beside COE Subject

III-4. Journal Papers

[231] D. Notsu, N. Ikechi, Y. Aoki, N. Kawakami and K. Shibahara, "Fabrication of 100 nm Width Fine Active-Region Using LOCOS Isolation", IEICE Trans. Electron., E.85-C, pp. 1119-1123 (2002).

[232] K. Shibahara, D. Onimatsu, Y. Ishikawa, T. Oda and T. Kikkawa, "Copper Drift in Low Dielectric Constant Insulator Films Caused by O_2^+ Primary Ion Beam", Appl. Surf. Sci., 203-204, pp. 387-390 (2002).

[233] A. Teshima and S. Miyazaki, "Improved Performance of Amorphous Silicon Photoreceptor by Using a Thick Surface Layer with a Graded-Band-Gap Structure", Jpn. J. Appl. Phys., 41, L1294-L1296 (2002).

[234] T. Kikkawa, N. Fujiwara, H. Yamada, S. Miyazaki, M. Hirose and F. Nishiyama, "Energy Band Structure of Ru/(Ba,Sr)TiO_3 /Si Capacitor Deposited by Inductively-Coupled Plasma-Assisted Radio- Frequency-Magnetron Plasma Sputtering," Appl. Phys. Lett.

vol.81, no.15, pp.2821-2823 (2002).

[235] A. Nakajima and M. Ishigame, " Local-hopping mechanism of an oxygen vacancy in ZrO_2 doped with Sc^{3+} studied by measuring quasi-elastic light scattering," Solid State Ionics 146, pp.133-141 (2002).

[236] K. Imai, S. Shishiguchi, K. Shibahara and S. Yokoyama, "Phosphorus-Assisted Low-Energy Arsenic Implantation Technology for N-Channel Metal-Oxide-Semiconductor Field-Effect Transistor Source/Drain Formation Process", Jpn. J. Appl. Phys., 42, No. 5A, pp. 2654-2659 (2003).

[237] S. Nakamura, M. Itano, H. Aoyama, K. Shibahara, S. Yokoyama and M. Hirose, "Comparative Studies of Perfluorocarbon Alternative Gas Plasmas for Contact Hole Etch", Jpn. J. Appl. Phys., 42, No. 9A, pp. 5759-5764 (2003).

[238] N. Mikami, N. Hata, T. Kikkawa and H. Machida, “Robust self-assembled monolayer as diffusion barrier for copper metallization”, Appl. Phys. Lett. Vol.83, No.25, Dec, PP.5181-5183. (2003).

[239] Xia Xiao, N. Hata, K. Yamada, T. Kikkawa, “Mechanical properties of periodic porous silica low-k films determined by the twin transducer surface acoustic wave technique,” Review of Scientific Instruments, vol. 74, No. 10,Oct., pp.4539-4541(2003).

[240] K. Yamada, Y. Oku, N. Hata, S. Takada and T. Kikkawa, "Effects of surfactants on the properties of ordered periodic porous silica films," Japanese Journal of Applied Phys, Vol.42, No. 4B, April, pp.1840-1842(2003).

[241] S. Kuroki, T. Kikkawa, H. Kochiya, and S. Shishiguchi, "Direct Patterning of Low-k Dielectric Films using X-Ray Lithography," Jpn. J. Appl. Phys. , vol.42, No.4B, pp.1907-1910(2003).

[242] Satoru Fujisawa, Takamaro Kikkawa and Tokushi Kizuka, “Direct Observation of Electromigration and Induced Stress in Cu Nanowire,” Jpn. J. Appl. Phys. Vol. 42, pp.L1433-L1435 (2003).

[243] A. Teshima and S. Miyazaki, “A New Analytical Modeling for Photo-induced Discharge Characteristics of Photoreceptors”, Jpn. J. Appl. Phys., (2004) in press.

[244] S. Kuroki, S. Sakamoto and T. Kikkawa, “A novel Photosensitive Porous Low-k Interlayer Dielectric Film,” Japanese Journal of Applied Physics Vol. 43, No. 4B, pp.1820-1824, (2004).

[245] Hidenori Miyoshi, Hisanori Matsuo, Yoshiaki Oku, Hirofumi Tanaka, Kazuhiro Yamada, Noboru Mikami, Syozo Takada, Nobuhiro Hata and Takamaro Kikkawa, “Theoretical Analysis of Elastic Modulus and Dielectric Constant for Low-k Two-Dimensional Periodic Porous Silica Films”, Japanese Journal of Applied Physics Vol. 43, No. 2, pp.498-503, (2004).

[246] Kazuyoshi Uera, Jun Kawahara, Hidenori Miyoshi, Nobuhiro Hata and Takamaro Kikkawa, “Molecular Orbital Calculation of the Elastic Modulus and the Dielectric Constant for Ultra Low-k Organic Polymers,” Japanese Journal of Applied Physics Vol. 43, No. 2, pp.504-507, (2004).

[247] Xia Xiao, Nobuhiro Hata, Kazuhiro Yamada and Takamaro Kikkawa, “Mechanical Property

Determination of Thin Porous Low-k Films by Twin-Transducer Laser Generated Surface Acoustic Waves," Japanese Journal of Applied Physics Vol. 43, No. 2, pp.508-513, (2004).

[248] Nobuhiro Hata, Chie Negoro, Kazuhiro Yamada and Takamaro Kikkawa, "Control of Pore Structures in Periodic Porous Silica Low-k Films," Japanese Journal of Applied Physics Vol. 43, No. 4A, pp.1323-1326, (2004).

[249] Chie Negoro, Nobuhiro Hata, Kazuhiro Yamada and Takamaro Kikkawa, "Nondestructive Characterization of a Series of Periodic Porous Silica Films by in situ Spectroscopic Ellipsometry in a Vapor Cell," Japanese Journal of Applied Physics Vol. 43, No. 4A, pp.1327-1329, (2004).

III-5. Proceedings of International Conferences

[250] T. Kikkawa, "Current and Future Low-k/Cu Interconnect Technologies for ULSIs", Proc. Workshop on Frontiers in Electronics, p.25 (IEEE, St. Croix, Jan. 6-11, 2002) (Invited).

[251] T. Kikkawa and T. Oda, ""Influence of copper ion drift on leakage current in porous methylsilsesquioxane derived from methylpolysilazane," Proc. European Workshop on Materials for Advanced Metallization (Vaals, The Netherlands, March 3-6, 2002).

[252] Y. Oku, N. Nishiyama, S. Tanaka, K. Ueyama, N. Hata, and T. Kikkawa, "Novel periodic nanoporous silicate glass with high structural stability as low-k thin film," Materials Research Society Spring Meeting, April, Symposium Proceedings,Vol.716, pp.587-592, (2002).

[253] N. Hata, Y. Oku, K. Yamada, and T. Kikkawa, "A new approach of thin-film X-ray diffraction / scattering analysis for ultra-low-k dielectrics with periodic pore structures," Materials Research Society Spring Meeting, April 2002, Symposium Proceedings,Vol.716, pp.581-586(2002).

[254] T. Kikkawa, "Present status and future trend of low-k dielectrics/interconnect technologies for ULSI (Invited)," Proc. 2002 7th International Symposium on Plasma-and Process-Induced Damage, (American Vacuum Society, IEEE, Maui, USA) pp.154-157 (2002).

[255] S. Sakamoto, K. Komura, and T. Kikkawa, "Effect of hexamethyldisilazane on the electrical characteristics of a porous silica thin film, "Abstract of 2002 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices,pp.125-129 (2002).

[256] S. Kuroki, T. Kikkawa, H. Kochiya, and S. Shishiguchi, "Direct Patterning of Low-k Dielectric Films using X-Ray Lithography," Extended Abstracts of SSDM, (Japan Society of Applied Phys., Tokyo) , pp.464-465, (2002).

[257] H. Yamada, N. Fujiwara, M. Yamato, S. Miyazaki, F. Nishiyama and T, Kikkawa, "Influence of Electrodes on the Leakage Current In (Ba,Sr)TiO_3 Thin films," Abstract of ECS International Semiconductor Technology Conference, ISTC 2002, E, Abstract No.108.

[258] Y. Oku, K. Yamada, N. Nishiyama, S. Tanaka, K. Ueyama, N. Hata and T. Kikkawa, "Effect of TEOS treatment on the properties of periodic nanoporous silica low-k film," Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 42-43, Nagoya, Sept. 17-19, (2002).

[259] S. Fujisawa, T. Kikkawa, and T. Kizuka, "Novel TEM/AFM/STM Microscopy for Cu

Nano-Wire Electromigration," Extended Abstracts of SSDM, (Japan Society of Applied Phys., Tokyo), pp.50-51, (2002).

[260] K. Yamada, Y. Oku, N. Hata, S. Takada and T. Kikkawa, "Structure control of periodic porous silica film for low-k application," Extended Abstracts of SSDM, (Japan Society of Applied Phys., Tokyo) , pp.40-41, (2002).

[261] N. Hata, C. Negoro, K. Yamada, H. S. Zhou, Y. Oku, and T. Kikkawa, "Analysis of pore structures in ultra low-k dielectrics," Extended Abstracts of SSDM, (Japan Society of Applied Phys., Tokyo) , pp.496-497, (2002).

[262] N. Sasaki, T. Oda, and T. Kikkawa, "Influence of Metal Electrodes on Leakage Current in MSQ Films with or without pores," Advanced Metallization Conference, pp.265-268, (2002).

[263] K. Imai, S. Maruyama, T. Suzuki, T. Kudo, S. Miyake, M. Ikeda, T. Abe, S. Masuda, A. Tanabe, J.-W. Lee, K. Shibahara, S. Yokoyama and H. Ooka, "60-nm Gate Length SOI CMOS Technology Optimized for System-on-a-SOI-Chip Solution," Proc. of the 203rd Meeting of Electrochemical Society, Silicon-on-insulator Technology and Devices XI, pp. 149-158 (2003).

[264] M. Murakawa, K. Shibahara, Y. Oda, T. Higuchi and K. Nishi, "Ultra-Shallow Boron Profile Fitting Compensating for Surface Contamination by Utilizing Genetic Algorithms," Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 504-505 (2003).

[265] Y. Oku, K. Yamada, T. Goto, Y. Seino, A. Ishikawa, T. Ogata, K. Koumura, N. Fujii, N. Hata, R. Ichikawa, T. Yoshino, C. Negoro, A. Nakano, Y. Sonoda, S. Takeda, H. Miyoshi, S. Oike, H. Tanaka, H. Matsuo, K. Kinoshita, and T. Kikkawa, "Novel Self-Assembled Ultra-Low-K Porous Silica Films with High Mechanical Strength for 45nm BEOL Technology," IEEE International Electron Devices Meeting Technical Digest, pp139-142, (2003).

[266] J. Kawahara, A. Nakano, N. Kunimi, K. Kinoshita, Y. Hayashi, A. Ishikawa, Y. Seino, T. Ogata, H. Takahashi, Y. Sonoda, T. Yoshino, T. Goto, S. Takeda, R. Ichikawa, H. Miyoshi, H. Matsuo, S. Adachi, and T. Kikkawa, "A New Plasma-Enhanced Co-Polymerization (PCP)Technology for Reinforcing Mechanical Properties of Organic Silica Low-K/Cu Interconnects on 300mm Wafers," IEEE International Electron Devices Meeting Technical Digest, pp143-146, (2003).

[267] N. Hata, C. Negoro, S. Takada, X. Xiao, K. Yamada and T. Kikkawa "Integrated Characterization of Porous Low-k Films for Identifying Killer Pores and Micropores," Proceedings of 2003 IEEE International Interconnect Technology Conference, 2-4 June, pp.51-53 (2003, SanFrancisco, USA).

[268] Hidenori Miyoshi, Hisanori Matsuo, Yoshiaki Oku, Hirofumi Tanaka, Kazuhiro Yamada, Noboru Mikami, Syozo Takada, Nobuhiro Hata and Takamaro Kikkawa, "Theoretical analysis of ultra low-*k* porous films with periodic pore arrangement and high elastic modulus," Proceedings of 2003 IEEE International Interconnect Technology Conference, 2-4 June, pp.57-59 (2003, SanFrancisco, USA).

[269] N. Mikami, N .Hata, T. Yoshino, T,Kikkawa, and H. Machida, "A new self-assembled monolayer as a robust diffusion for Cu interconnect," Advanced Metallization Conference, pp. 68-69, (2003).

[270] C. Negoro, N. Hata , K. Yamada, and T. Kikkawa, "Non-destructive characterization of a

series of periodic porous silica films by in-situ spectroscopic ellipsometry in a vapor cell," Advanced Metallization Conference, pp. 92-93, (2003).

[271] Y. Takenobu, N. Hata, and T. Kikkawa, “Evaluation of Copper Ion Drift in Low-Dielectric Constant Interlayer Films by Transient Capacitance Spectroscopy,” Materials Research Society, Symposium Proceedings, Vol.766, pp.217-222, (2003).

[272] N. Hata, C. Negoro, S. Takada, K. Yamada, Y. Oku, and T. Kikkawa, “Advanced characterization of ultra- low-k periodic porous silica films-pore size distribution, pore-diameter anisotropy, and size and macroscopic isotropy of domain structure,” Materials Research Society, Symposium Proceedings,Vol.766, pp.191-195, (2003).

[273] C. Negoro, N. Hata and T. Kikkawa, “Nondestructive Characterization of Pore Size Distributions in Porous Low-K Films by in-situ Spectroscopic Ellipsometry in Vapor Cell,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 78-79, Tokyo, Sept. 16-18, (2003).

[274] Y. Seino, R. Ichikawa, H. Tanaka and T. Kikkawa, “Accurate measurement of mechanical properties of nanoporous silica ultra-low-k films,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 80-81, Tokyo, Sept. 16-18, (2003).

[275] S. Takada, N. Hata, Y. Seino, K. Yamada, Y. Oku and T. Kikkawa, “Mechanical Property and Skeletal Silicate Structure of Periodic Porous Silica Films,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 82-83, Tokyo, Sept. 16-18,(2003).

[276] X. Xiao, N. Hata, K. Yamada, H. Tanaka and T. Kikkawa, “Determination of the Mechanical Properties of Thin Periodic Porous Silica Films by Laser-Generated Surface Acoustic Wave Technique,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 84-85, Tokyo, Sept. 16-18, (2003).

[277] H. Matsuo, A. Ishikawa and T. Kikkawa, “In-situ Measurement of Friction Force during Cu Chemical Mechanical Polishing,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 254-255, Tokyo, Sept. 16-18, (2003).

[278] N. Hata, C. Negoro, K. Yamada and T. Kikkawa, “Control of Pore Size and Porosity in Periodic Porous Silica Low-k Films,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 258-259, Tokyo, Sept. 16-18, (2003).

[279] S. Kuroki, T. Hirota and T. Kikkawa, “A Novel Photosensitive Porous Low-k Interlayer Dielectric Film,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 468-469, Tokyo, Sept. 16-18, (2003).

[280] S. Sakamoto, S. Kuroki and T. Kikkawa, “Influence of Humidity on Electrical Characteristics of Porous Silica Films,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 478-479, Tokyo, Sept. 16-18, (2003).

[281] M. Yamato, H. Yamada and T. Kikkawa, “Influence of interface layers and bottom electrodes on (Ba,Sr)TiO_3 thin film leakage current,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 484-485, Tokyo, Sept. 16-18, (2003).

[282] S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, “Effect of High Resistivity Si Substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp. 668-669, Tokyo, Sept. 16-18, (2003).

[283] K. Uera, J. Kawahara, H. Miyoshi, N. Hata, and T. Kikkawa, “Dielectric Constant and Young’s Modulus of Organic Low-k Materials by Molecular Orbital Method,” Abstract of Advanced Metallization for ULSI Application, pp. 20-21, 2002;Conference Proceedings ULSIXVIII, Materials Research Society, pp. 643-648, (2003).

[284] C. Negoro, N. Hata , K. Yamada, H. S. Zhou, and T. Kikkawa, "Characterization of Porous Low-k Dielectrics by Gas Adsorption Techniques," Abstract of Advanced Metallization for ULSI Application (2002) pp.34-35. Conference Proceedings ULSIXVIII, Materials Research Society, pp.273-278 (2003).

[285] M. Shibahara, S. Kotake, T. Inoue, A. Matsuno, K. Kagawa and K. Shibahara, "Molecular Dynamics Simulation On Excimer Laser Annealing Process for Ultra Shallow Junction Formation,” The 1st Int. Symp. on Micro & Nano Technology, to be presented, (2004).

III-3．Books

[286] K. Shibahara, Supervisor of Translation of “Fundamentals of Modern VLSI Devices,” written by Y. Taur and T.H. Ning, Maruzen (2002).

Patents

I. Circuits and Systems

[1] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method,” JPN Patent Application No.2002-165759 (2002.05.31).

[2] H.J. Mattausch and T. Koide, "Self-adjusting winner lineup amplifier,” JPN Patent Application No.2002-159436 (2002.06.06).

[3] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, “Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus,” JPN Patent Application No. 2002-152491, (2002.05.27).

[4] T. Hironaka, H.-J. Mattausch and T. Koide, T. Hirakawa, K. Johguchi, "Multi-port integrated cache,” Japanese Patent Application 2002-320037 (2002.11.11).

[5] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method,” USA Patent Application No.10/453,636 (2003.05.27).

[6] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method,” EPC Patent Application No.03012722.9 (2003.05.27).

[7] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method,” KOR Patent Application No.2003-36263 (2003.05.27).

[8] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method," TWN Patent Application No.92115261 (2003.05.27).

[9] H.J. Mattausch and T. Koide, "Self-adjusting winner lineup amplifier," USA Patent Application No.10/445,033 (2003.06.04).

[10] H.J. Mattausch and T. Koide, "Self-adjusting winner lineup amplifier," EPC Patent Application No.03011724.6 (2003.06.04).

[11] H.J. Mattausch and T. Koide, "Self-adjusting winner lineup amplifier," KOR Patent Application No.2003-34611 (2003.06.05).

[12] H.J. Mattausch and T. Koide, "Self-adjusting winner lineup amplifier," TWN Patent Application No.92114262 (2003.06.05).

[13] H. J. Mattausch, T. Koide, T. Hironaka, H. Uchida, K. Johguchi, Z. Zhu, " Memory with Synchronous Bank Architecture," Japanese Patent Application 2003-167989 (2003.6.12).

[14] H.J. Mattausch, T. Koide, M. Mizokami, "Recognition and Learning Method of Reference Data and Pattern-Recognition System," Japanese Patent Application 2003-434596 (2003.12.26).

[15] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus," USA Patent Application No.10/445,247, (2003.05.26).

[16] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus," EPC Patent Application No.03011840.0, (2003.05.26).

[17] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus," KOR Patent Application No.2003-33324, (2003.05.26).

[18] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus," TWN Patent Application No.92114142, (2003.05.26).

[19] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit," JPN Patent Application No. 2003-322163, (2003.09.12).

[20] T. Hironaka,H.-J. Mattausch and T. Koide, T. Hirakawa, K. Johguchi, "Multi-port integrated cache," USA Patent Application TBD (2003.10.06).

[21] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum," JPN Patent Application No. 2004-017429 (2004.01.26).

[22] H.J. Mattausch, T. Koide, Y. Shirakawa, "Method for Reference-Data Optimization and Pattern-Recognition System," Japanese Patent Application 2004-053433 (2004.2.27).

[23] H. J. Mattausch, T. Koide, T. Hironaka, H. Uchida, K. Johguchi, Z. Zhu, "Memory with Synchronous Bank Architecture," No.TBD, (2004.2).

[24] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum," USA, Patent Application No.TBD (2004.05.31).

[25] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum," EPC Patent Application No.TBD (2004.05.31).

[26] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum," KOR Patent Application No.TBD (2004.05.31).

[27] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum", TWN Patent Application No.TBD (2004.05.31).

[28] H. J. Mattausch, T. Koide and M. Mizokami, "Reference Data Recognition and Learning Method and Pattern Recognition System," USA Patent Application No. TBD. (2004. 6. 15).

[29] H. J. Mattausch, T. Koide and M. Mizokami, "Reference Data Recognition and Learning Method and Pattern Recognition System," EPC Patent Application No. TBD. (2004. 6. 15).

[30] H. J. Mattausch, T. Koide and M. Mizokami, "Reference Data Recognition and Learning Method and Pattern Recognition System," KOR Patent Application No. TBD. (2004. 6. 15).

[31] H. J. Mattausch, T. Koide and M. Mizokami, "Reference Data Recognition and Learning Method and Pattern Recognition System," TWN Patent Application No. TBD. (2004. 6. 15).

[32] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit," USA Patent Application No. TBD, (2004.05.31).

[33] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit," EPC Patent Application No. TBD, (2004.05.31).

[34] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit," KOR Patent Application No. TBD, (2004.05.31).

[35] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, "Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit," TWN Patent Application No. TBD, (2004.05.31).

[36] M. Sasaki, A. Iwata, D. Arizono, "Semiconductor Equipment," Japanese Patent 2004-10053, (2004.01.19)

[37] S. Kameda, A. Iwata, M. Sasaki, K. Kikkawa, Japanese Patent 2004-022317 (Application), (2004.01.28)

II. Device Modeling

[38] M. Miura-Mattausch, D.Kitamaru, Japanese Patent H15-077934, (2003.3.14).

[39] M. Miura-Mattausch, N. Nakayama, Japanese Patent 2003-318947, (2003.9.10).

[40] M. Miura-Mattausch, H.Ueno, S.Hosokawa, Japanese Patent 2003-420845,(2003.12.18).

III. Nanodevices and Processing

[41] T. Fujii, S. Yokoyama, Taiwan Patent, 091109971,(2002.05.14).

[42] A. Nakajima, Japanese Patent, 2002-158788 (2002.05.31).

[43] A. Nakajima, Japanese Patent, 2002-268342 (2002.09.13).

[44] S. Yokoyama, A. Nakajima, Y. Tada, G. Nakamura, M. Imai, T. Yonekawa, "Method of fabricating semiconductor device," International Patent PCT/JP02/05386 (2002.05.31), WO 02/099868 (2002.12.12).

[45] K. Kikkawa, A. Iwata, H. Sunami, Hans Jürgen Mattausch, S. Yokoyama, K. Shibahara, A. Nakajima, T. Koide, A.B.M.H. Rashid, S. Watanabe, Japanese Patent, 2003-117826 (2003.4.23).

[46] A. Nakajima, S. Yokoyama, K. Kikkawa, M. Wake, Japanese Patent, 2003-081181 (2003.03.24).

[47] A. Nakajima, "Semiconductor device and method for manufacturing same" USA Patent, 10/437119 (2003.05.14).

[48] M. Ogiwara, H. Fujiwara, S. Yokoyama, Japanese Patent, MA901355,(2003.09.29).

[49] K. Shibahara, Japanese Patent, 2003-311387, (2003.9.3).

[50] M. Murakawa, K. Shibahara, T. Oda, T. Higuchi, K. Nishi, Japanese Patent, 2003-320495 (2003.9.12).

[51] A. Nakajima, Japanese Patent, 2004-099015 (2004.03.30).

[52] R. Nishibayashi, T. Miyazaki, T. Imai, T. Tabei, S. Yokoyama, Japanese Patent, 2004-123383.

[53] R. Nishibayashi, T. Miyazaki, T. Imai, T. Tabei, S. Yokoyama, Japanese Patent, 2004-123379.

Awards

[1] T. Maeda, A. Iwata, LSI IP Design Award, Development Encouragement Award, "Development of Low Phase Noise CMOS VCO with Frequency Range" (2002).

[2] S. Hosokawa, STARC Symposium, Special Award for Presentation (2002).

[3] Y. Mitani, H. Uchida, T. Hironaka, and H.J. Mattausch, and T. Koide "SuperH Compatible Instruction Set Processor IP for System LSI Research and Education," The 4th LSI IP Design Award, Challenge Award, LSI IP Design Award Committee, 2002.5. URL http://ne.nikkeibp.co.jp/award/

[4] T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "A real-time picture-segmentation

architecture for intelligent information processing, ”The 4th LSI IP Design Award, Development Encouragement Award, LSI IP Design Award Committee, 2002.5. URL http://ne.nikkeibp.co.jp/award/

[5] K. Johguchi, Z. Zhu, H. J. Mattausch, T. Koide, T. Hirakawa, and T. Hironaka, "Multi-Port Cache Design Based on Hierachcal Multi-Bank Memory Architecture", The 4th IEEE Hiroshima Student Symposium (HISS), Research Award, (2002).

[6] Y. Darma, 16th International Microprocesses and Nanotechnology Conference 2002 Award, young Author's Award (2002).

[7] T. Morie, M. Ishidu, H. Ando, A. Iwata, IP Award“Coarse Image Region Segmentation Using Resistive-fuse Networks” (2003).

[8] A. Iwata, Fellow of the Institute of Electronics, Information and Communication Engineers (2003).

[9] T. Koide, H.J. Mattausch, Y. Yano, T. Gyohten and Y. Soda, "A Nearest-Hamming-Distance Search Memory with Fully Parallel Mixed Digital-Analog Match Circuitry," The Asia and South Pacific Design Automation Conference (ASP-DAC2003), Special Feature Award, University Design Contest.

[10] S. Fukae, N. Ohmori, H. J. Mattausch, T. Koide, T. Inoue, and T. Hironaka, "Minimization of Transistor Numbers and Global Wiring Numbers by Distributed Crossbar Function for Realizing Bank-based Multiport Memories“, The Institute of Electrical Engineers of Japan, Conference Paper and Presentation Award of the 54th Annual Technical Conference of the Chugoku Chapter of the Electronics and Information Institute (2003).

[11] K. Johguchi, Z. Zhu, H. J. Mattausch, T. Koide, T. Hirakawa, and T. Hironaka, "Combined Data/Instruction Multi-Port Cache Design Based on Hierachcal Multi-Bank Memory Architecture", The 5th IEEE Hiroshima Student Symposium (HISS), Research Award, (2003).

[12] T. Morimoto, “Research for Real-Time Image Segmentation Architecture and its Digital-CMOS Implementation,” Hiroshima University Student Award, President of Hiroshima University, Taizou Muta, No. 1-0061, 2003.3.

[13] Navarro Dondee (Prof. Miura’s Group), Special Award for Presentation, SRARC Symposium 2003, Poster Session, (2003.9.11).

[14] H. Sunami, Fellow of the Institute of Electronics, Information and Communication Engineers (2003).

[15] Y. Darma (Prof. Miyazaki’s Group), Solid State Devices and Materials, Young Researcher Award (2003).

[16] S. Miyazaki, Japanese Journal of Applied Physics Editorial Contribution Award (2003).

[17] Y. Yano, T. Koide, and H.J. Mattausch, “Fast, Compact, and Low-Power Minimum Hamming/Manhattan Distance Search Associative Memory Macro,” The 6th LSI IP Design Award, IP Award, LSI IP Design Award Committee, 2004.5. URL http://ne.nikkeibp.co.jp/award/

[18] S. Miyazaki, Selete Award 2004, Achievement Award (2004).

[19] Y. Darma (Prof. Miyazaki's Group), Hiroshima University, President's Distinction Award (2004).