Three Dimensional Integration Architecture for Tera-bit Information processing

Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter),
Mamoru Sasaki (Assoc. Prof., Graduate School of Advanced Sciences of Matter)
Seiji Kameda, Hiroshi Ando (COE Researchers),
Takeshi Yoshida, Mitsuru Shiozaki (Graduate School of Advanced Sciences of Matter, D3)
and Masahiro Ono (Graduate School of Advanced Sciences of Matter, D1)

1. Research Target

1.1 New paradigm for future integration systems

There are three major elements of information processing in electronics: (1) operation and judgment, (2) memory and learning, and (3) communication and data transfer. Although a great deal of progress has been made in the field of semiconductor memory, the problem of how best to utilize the huge memory capacity now available to us remains. How do we memorize people's face and objects? Although this question has yet to be resolved, it is clear that we do not simply analyze and recognize the characteristics of pictures. In addition to images, we use other elements to memorize such information. Moreover, it seems that the patterns are distributed to various parts of the brain. Although living systems use slow neural network devices, *i.e.*, the cells of the brain, which are unreliable because of sensitivity to changes in environment or noise, they achieve a sufficient level of information processing capability. This strategy has been utilized based on the results obtained by various methods using super parallel processing. This was most suitable for use of the huge number of neurons in living systems. To mimic the processes occurring in living systems, it is important to establish functions for the collection and processing of the distributed information and to make global judgments. The bottleneck is the information communication capability within and between the chips.[1]

In 21st century, promising solution for breaking Moore's law will be three dimensional integration technologies utilizing nano-devices and advanced interconnect technologies.

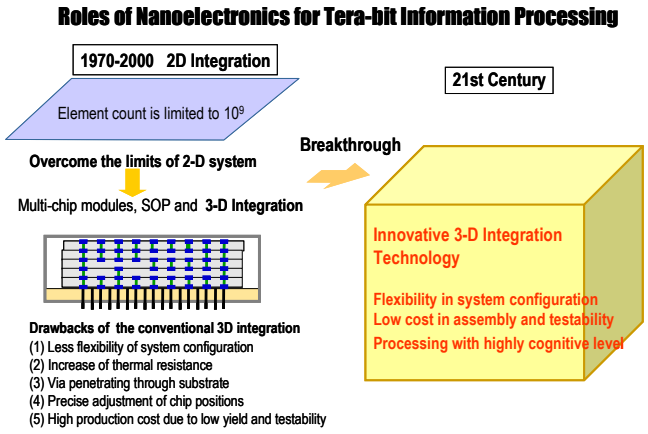

Fig.1 Roles of nanoelectronics for era-bit information processing

How to solve communication bottlenecks

In order to realize Tera-bit information processing system, we have proposed three-dimensional integration technologies utilizing wireless communications between and within the chips at the COE. This enables wiring through multiple chips and new three-dimensional integration without requiring accurate positioning. In addition, we have also attempted to develop optical communication implemented with photonic devices and quantum dots memory devices using light communication and Nano-structures. Integration technology, to integrate both radio and light, will be realized by fusion of device modeling and process technology. We will build further knowledge and strategies by realizing super-parallel processing and conduct research into processing by integration of super-efficient circuit and modeling technology with algorithms reflecting living systems. The ultimate aim of this research is the realization of a brain type processing system.

1.2 Interconnection for three dimensional integration

We intended to realize three-dimensional integration of multi-chips with different kinds of functions and technologies. To achieve the 3D integration, the most important technology is chip-to-chip interconnection. For that purpose, we introduce two types of wireless interconnections for global clock/data transfer and parallel interconnections for distributed data between adjacent chips.Optical interconnection using integrated optical components such as a wave-guide, an optical switch and an optical resonator is also introduced to high-speed and wide-band data transfer.

1.3 Tera-bit information processing system architecture

The target is highly sophisticated multi object recognition system with high speed real-time image analysis capability and flexible data matching and learning functions. Furthermore, we are aiming at a highly sophisticated brain of hyper human robot.

These systems require over 10GHz clock computing and massively parallel processing units accessing to giga byte data base. Thus tera-bit information processing has to be implemented with small size, low power and low cost. We intended to create the solution for the future electronic system with nano-devices.

2. Research Achievementss

2.1 MOSFET Model and circuit design:

HiSIM for high frequency operation and the SOI structure has been developed by Prof. Miura's Group. Its concept is to describe device operation using surface potentials in accordance with basic physical principles. It was selected as a candidate of the international standard MOS model for 60nm node, by Compact Modeling Council.

An 0.18um-CMOS test chip with RF-MOS devices and a voltage controlled oscillator (VCO) was designed and measured for evaluating the HiSIM model in the GHz frequency region. (In Corporation with Prof. Miura's Group)

Low noise and RF analog circuits for neural signal sensing system were investigated. The CMOS chopper stabilization technique was established for uV level signals amplification. Low voltage A-to-D converter and wireless transmitter have bee developed by T. Yoshida , Doctoral student. The image recognition system needs the technology of biometrics and RF interface.

Substrate noise analysis technique in GHz frequency range has also developed for reliable design..

Chip-to-chip flexible interconnection based on CDMA system was studied. CMOS transceiver chip with 2Gbps bit rate was developed by M. Shiozaki, Doctoral student.

2.2 Wireless Interconnection [2,3]

We propose wireless interconnection using integrated antenna and ultla-wide band transceiver for global data communication.

(1) Global wireless interconnection using integrated antenna and ultra-wideband communication systems

Radio wave propagation through a silicon substrate was measured using integrated dipole antennas. A 20GHz radio wave propagates with low loss through a highly resistive Si substrate made by the proton implantation. [4] This technology realizes the new 3D integration utilizing chip-to-chip wireless global interconnects for system clocks and buses for bi-directional data transfer and broadcasting. (Prof. Kikkawa's group)

(2) Local wireless Interconnection using coupled inductors

We have proposed an interconnect scheme between the stacked chips based on resonant coupling of an integrated spiral inductor pair as shown in Fig.4. A data transmitter and receiver were design A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the communication of the spiral inductor pair. The performance, 1Gb/s/channel at 9mW/channel, has been confirmed by SPICE simulation. If we use a 90 nm device technology, 2-5Gbps data transfer with 1mW per connection. By compromising chip area and power dissipation, over 100 localized data are transferred between a pair of adjacent chips. (Prof. Sasaki's Group)

2.3 Three dimensional integration using GWI and LW

We call this three dimensional integration system ***3DCSS:*** 3-dimensional custom stack system.

In the *3DCSS*, stacked chips fabricated by various device technologies are connected by the two types of wireless connections, which are GWI and LWI. GWI is used for distribution of over 10GHz system clocks, bi-directional data transfer and broadcasting of address or control data to multi-chip database. LWI provides highly parallel multi-channel communication enabling 2D data transfer such as visions and neural information.

Both use of GWI and LWI will become a promising solution for realizing intelligent tera-bit information processing.

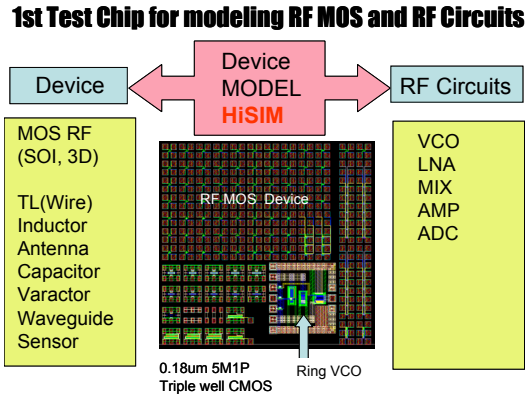

Fig.2 Test chip for modeling RF MOS and RF circuitss

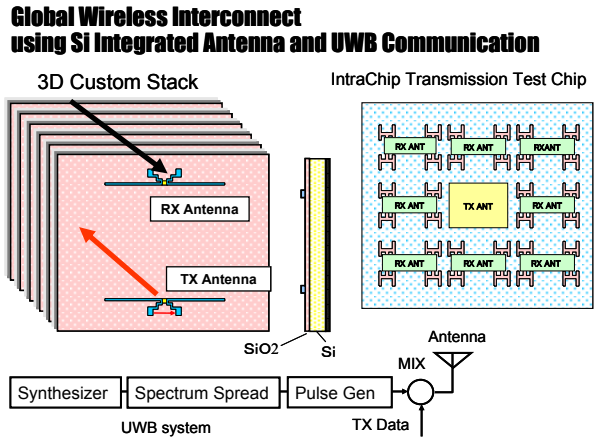

Fig.3 Wireless interconnection using integrated antennas

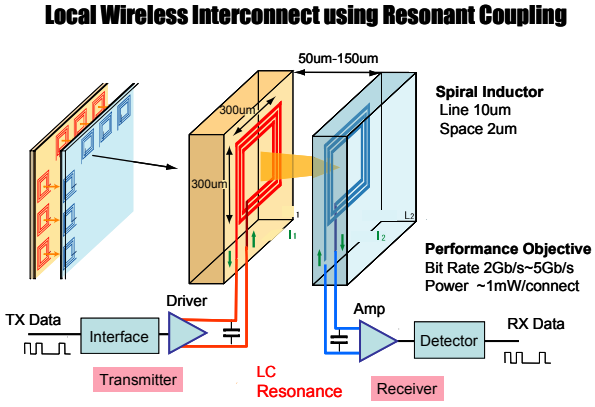

Fig.4 Wireless interconnection using resonance coupling of an inductor pairs

2.3 Algorithm and Architecture

(1)Vision system based on biological processing [5,6,7]

In the stacked multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. Due to the wireless connections, the 3DCSS overcomes a wiring complexity that is the demerit of the multi-chip system generally. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system.

Multi-chip vision system architecture using PWM signals [8] and the local wireless interconnection was proposed by Dr. S. Kameda, COE researcher. 2D image processing for image enhancement and feature detection is implemented on the multi-chip with parallel analog data transfer as shown in Fig. 5. As the first step toward fabrication of the visual processing system, a prototype visual processing chip is fabricated with a PWM-based line parallel interconnection. In the next step, we will have to verify the operation of the multi-chip system with wireless interconnection and consider visual processing algorithms.

(2) Image recognition based on the Principal Component Analysis [9,10]

A Concept of Multi-object Recognition System

For the purpose of developing a real-time/high-level recognition technology, a concept of multi-object recognition system composed of 3DCSS was proposed by Dr. H. Ando, COE researcher.

The hierarchical and massively-parallel processing of human brain are achieved using multi-functional chips and local/global wireless interconnects among LSIs based on pixel-parallel circuit architecture. 3DCSS systems composed of image sensor, image normalizer, objects detector, objects recognizer and multi-object database (DB) chips are shown in Fig. 6. We also have confirmed human face detection in a natural scene and recognition under some variations using the eigenfaces method by numerical simulation. We developed a prototype real-time human face recognition system composed of personal USB camera and software based on Win32API as shown in Fig. 5. This system can operate about 10 frame/s and recognize one or more human faces between each frame

We are scheduled to extend the eigenfaces method to multi-object recognition and realize their VLSI implementation.

(3) Robot Brain

The first target is to propose a strategy learning model for the Robot Brain of game robot. The second target is to implement the model by the custom LSI which is very compact and has low power consumptions. Strategy learning model for brain of game robot have been developed by Masahiro Ono, Doctoral student.

By extending LVQ learning algorithm, the model to create strategy of attack adaptively changing environment have been obtained. The model will be applied to architecture of brain chip for 3DCSS.

3. Conclusion and future schedule

We proposed the tera-bit information system architecture using three-dimensional integration system. (3DCSS). It features new wireless interconnection technologies which enables flexible data/clock transfer. To realize the system, we developed circuits design using MOS device model *HiSIM,* architecture of image processing, and concept of the multi-object recognition system c

We will design system architecture of 3D integrated vi-

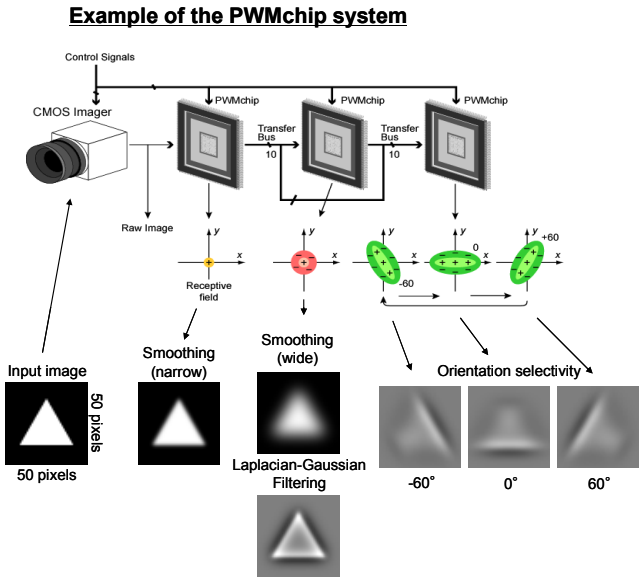

Fig.5 Example of image processing of multi-chip vision

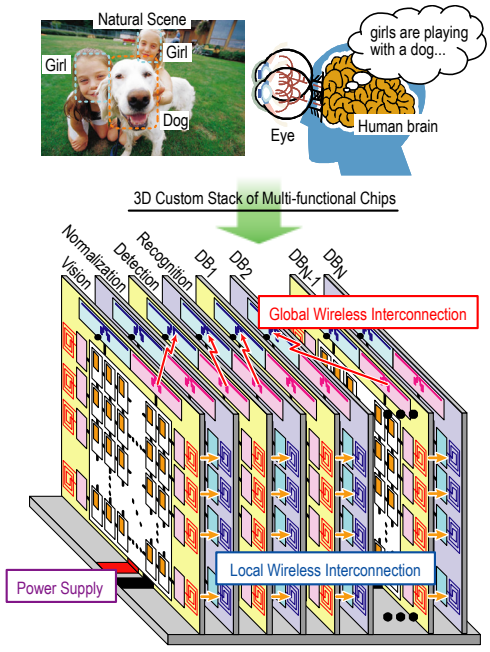

Fig.6 A concept of multi-object recognition system . using 3DCSS

sion systems and implement a proto type system.

References

[1] Burnss et al. ISSCC2001, .pp268-269, Konayagi et al. ISSCC2001, pp.270-271

[2] Kanda et al. ISSCC2003, pp.186-187

[3] Mizoguchi et al. ISSCC2004, pp142-143

[4] A.B.M.H. Rashid, *et al*., IEEE Electron Device Letters. 23(12) (2002) pp.731-733.

[5] S. Kameda, *et al*., Proc. IJCNN'03. (2003) pp.387-392.

[6] S. Kameda, *et al*., IEEE Trans. Neural Networks. 14(5) (2003) pp.1405-1412.

[7] A. Moini, *Vision Chips* (2000).

[8] A. Iwata, *et al.*, IEICE Trans. Fundamentals. E84-A(2) (2001) pp.486-496.

[9] M. Yang, *et al*., IEEE Trans. Pattern Analysis and Machine Intelligence, vol. 24, pp. 34-58, 2002.

[10] M. A. Turk, *et al*., CVPR'91, pp.5860591, 1991.

.

Published Papers and Patents

Published Papers

1. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels", IEICE Trans. Fundamentals., vol.E87-A, pp.376-383, Feb. 2004.
2. H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata "Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques", IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, 2002.
3. H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata "Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques", IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, 2002.
4. K. Katayama, M. Nagata, T. Morie and A. Iwata, An Hadamard Transform Chip Using the PWM Circuit Technique and Its Application to Image Processing, IEICE Trans. Electron., Vol. E85-C, NO.8, pp. 1596-1603, Aug. 2002.
5. K. Katayama, and A. Iwata, A High-Resolution CMOS Image Sensor with Hadamard Transform Function, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences E86-ANO.2, pp. 396-403、Aug.2003.
6. T. Yoshida, M. Akagi, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu, A Design of Wireless Neural-Sensing LSI, IEICE Trans. Electronics, vol.E87-C, pp.996-1002. June 2004.
7. T. Morie, T. Nakano, J. Umezawa, and A. Iwata, Gabor-Type Filtering Using Transient States of Cellular Neural Networks, Intelligent Automation and Soft Computing, in press, 2004.

Proceedings

1. M. Nagata, Y. Murasaka, Y. Nishimori, T. Morie, and A. Iwata Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models, Proc. 7th Asia and South Pacific Design Automation Conf, pp. 71-76, Bangalore, Jan. 2002.
2. T. Morie, J. Umezawa, T. Nakano, H. Ando, M. Nagata, and A. Iwata, A Biologically-Inspired Object Recognition System Using Pixel-Parallel Feature Extraction VLSIs, International Invitational Workshop on Intelligent Interface Devices, pp. 35-37, Kitakyushu, March 14, 2002.
3. M. Nagata, T. Morie, and A. Iwata, Modeling Substrate Noise Generation in CMOS Digital Integrated Circuits, IEEE 2002 Custom Integrated Circuit Conf, Orlando, May 2002.
4. K. Katayama and A. Iwata, A High-Resolution Hadamard Transform Chip, International Conference on Solid State Devices and Materials (SSDM), pp. 372-373, Nagoya, September17-19, 2002
5. T. Maeda, A. Iwata, M. Kawabata, and S. Orisaka A 10-GHz Bipolar VCO with Reduced Phase Noise, International Conference on Solid State Devices and Materials (SSDM), pp. 370-371, Nagoya, September17-19, 2002
6. H. Ando, T. Morie, M. Nagata, and A. Iwata, An Image Region Extraction LSI Based on a Merged/Mixed-Signal Nonlinear Oscillator Network Circuit, 28th European Solid-State Circuits Conference (ESSCIRC 2002), CP.11, pp. 703-706, Florence, Italy, Sept. 26, 2002
7. K. Katayama and A. Iwata, Pulse Coupled Neural Network using Coupled Phase Locked Loop, International Symposium on Nonlinear Theory and its Applications (NOLTA), pp. 853-856, Xi'an,October 7-11, 2002
8. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels", Proc. of Workshop on SASIMI, pp. 206-210, 2003.
9. A. Iwata, (Invited) Advanced Design for Analog-RF and Digital Mixed LSIs- Crosstalknoise Evaluaiton and Reduction, Proc. of the Workshop on SASIMI, pp.17-22, Hiroshima, 2003.
10. H.-J. Cho, W. K. Chu, N. Verghese,K. Shimazaki, H. Tsujikawa, S. Hirano, S. Doushoh, M. Nagata, A. Iwata, T. Ohmoto, A Substrate Noise Analysis Methodology for Large-Scale Mixed-Signal ICs, Proceedings of IEEE 2003 Custom Integrated Circuits Conference (CICC 2003),pp. 369-372, Sept. 2003.
11. Seiji Kameda and Tetsuya Yagi, A silicon retina system that calculates direction of motion, Proc. The 2003 IEEE International Symposium on Circuits and Systems, vol.IV, pp.792-795, Bangkok, 2003.
12. Seiji Kameda and Tetsuya Yagi, An analog silicon retina with multi-chip configuration, International Joint Conference on Neural Networks 2003 Conference Proceedings, pp.387-392, Oregon, 2003.7.
13. T. Morie, J. Umezawa, and A. Iwata, A Pixel-Parallel Image Processor for Gabor Filtering Based on Merged Analog-Digital Architecture, Accepted for presentation in 2004 Symposium on VLSI Circuits, Honolulu, Hawaii, June 17-19, 2004.
14. M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, "A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System," Accepted for presentation in 2004 Symposium on VLSI Circuits, Honolulu, Hawaii, June 17-19, 2004. .
15. T.. Morie, T. Nakano, J. Umezawa, and A. Iwata Gabor Filtering Using Cellular Neural Networks and its Application to Face/Object Recognition, Accepted for presentation in World Automation Congress, Seville, Spain, June, 2004.
16. K. Sasaki, T. Morie, and A. Iwata, A Spiking Neural Network with Negative Thresholding and Its Application to Associative Memory, Accepted for presentation in 2004 IEEE Int. Midwest Symposium on Circuits and Systems (MWCAS2004), Hiroshima, July 25-28, 2004.

Patents

1. Japanese Patent 2004-10053, "Semiconductor Equipment"
2. Japanese Patent 2004-22317, 2004.01.28