

# A Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors

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## 1. Research Target

With the continuous downsizing of CMOS technology, various components such as processors, memories, analog circuits, RF interface, are integrated in a single chip. It is called a system LSI. However, it takes considerable time to develop system LSIs, and the integration of a wide variety of system functions on a single chip invites considerable low yield. As an alternative, attention has been drawn to the System-in-Package. Also in our COE program, development of the 3-Dimensional Custom-Stack System (3DCSS) is one of the significant themes. In conventional 3D IC fabrication technique, vias with large aspect-ratio are required, in order to connect the stacked chips [1]. A wireless interconnect utilizing capacitor coupling has been proposed and it may avoid forming the vias [2]. However, the distance between the stacked chips can not be extended so as cool the internal circuits, because of the capacitive coupling. Thus, the heat dissipation issue is still unsolved. Two types of wireless connection are studied in our COE program. One is global connection, which communicates beyond neighboring chips using microwave [3]. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. The global connection is useful for broadcasting, global control, etc. On the other hand, the local connection can handle huge data volumes due to the massive parallel structure, and it is useful for communication of 2D vision information. In this manuscript, we propose a wireless interconnect for the local connection utilizing resonant coupling between spiral inductors (see Fig.1).

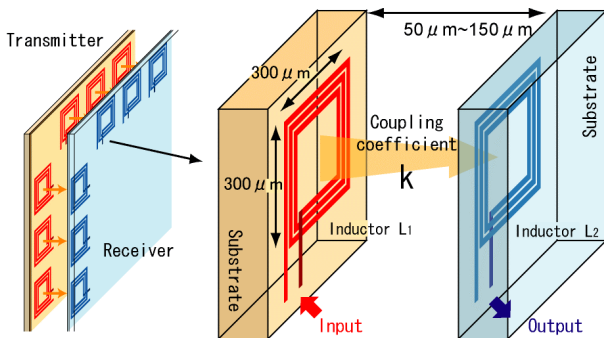


Fig.1 Spiral inductor based wireless interconnect.

## 2. Research Results

### 2-1. Analysis and modeling of spiral inductor pair

In order to utilize circuit simulators for the design, we introduce an equivalent circuit of the spiral inductor pair.

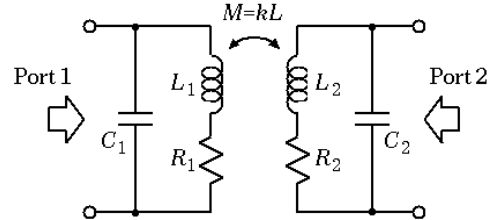


Fig.2 An equivalent model of spiral inductor pair.

Fig.2 shows the simple equivalent circuit.  $L$ ,  $C$ , and  $R$  are the self-inductance, parasitic capacitance and loss resistance of the spiral inductor, respectively.  $M$  and  $k$  are the mutual inductance and the coupling coefficient between the spiral inductor pair. 2-port S-parameter data has been obtained from FDTD 3D electromagnetic-field analysis. Then, the element values in Fig.2 were calculated by data-fitting to the 2-port S-parameter data. The result is shown in Fig.3. In layout of the spiral inductor, line width and space were  $10\mu\text{m}$  and  $2\mu\text{m}$ , respectively. The shape was square and the outer diameter was fixed at  $300\mu\text{m}$ . As parameters, the number of turns and distance between the spiral inductor pair were selected. Fig.3 shows the relationship between the self-inductance and the number of turns. It also shows the relationship of the coupling coefficient. The three curves are drawn, when the distance between the spiral inductor pair is  $50\mu\text{m}$ ,  $100\mu\text{m}$  and  $150\mu\text{m}$ , respectively.

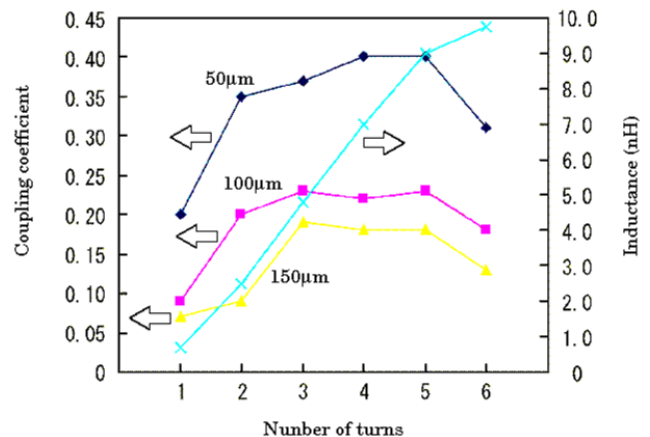


Fig.3 Results of 3D electromagnetic-field simulation.

### 2-2. Circuit configuration and SPICE simulations

Figure.4 shows a circuit diagram including the model of the spiral inductor pair. Note that capacitors  $C_{a1}$  and  $C_{a2}$

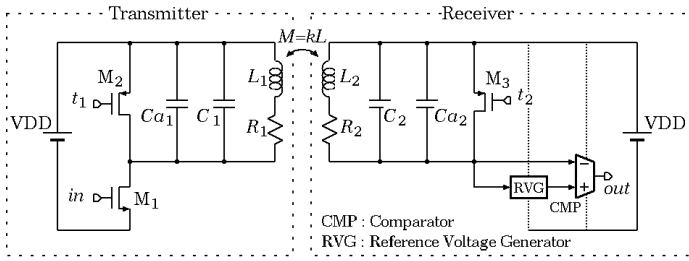


Fig.4 Circuit diagram.

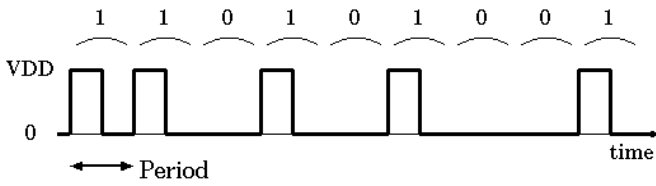


Fig.5 Return zero signal.

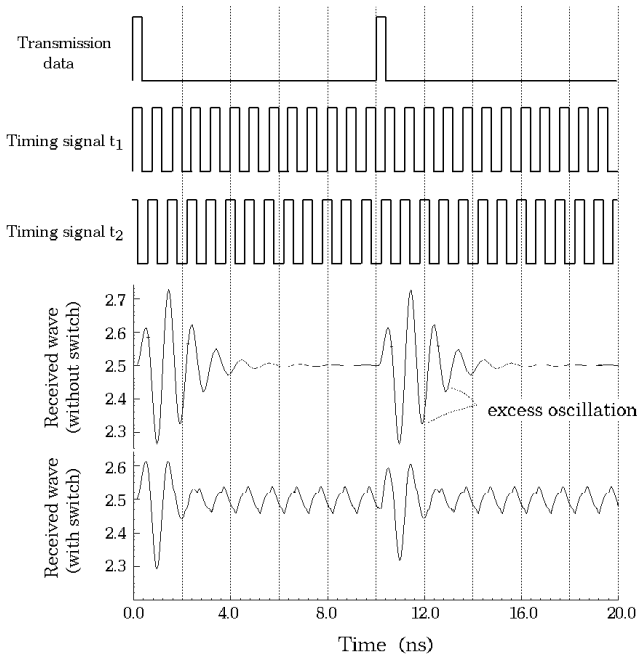


Fig.6 Simulation results.

are connected to the inductors  $L_1$  and  $L_2$ , in order to implement resonators in both the transmitter and the receiver. Although the spiral inductor without the additional capacitor has self-resonant frequency,  $C_{a1}$  and  $C_{a2}$  reduce the resonant frequencies until the convenient frequency for typical communications. A MOSFET  $M_1$  works as driver in the transmitter. A return zero signal shown in Fig.5 is given to the gate of  $M_1$ . The resonant frequencies of the resonators in both the transmitter and the receiver are made equal to the transmission frequency of the return zero signal, by connecting the capacitors  $C_{a1}$  and  $C_{a2}$ . The resonance

property enlarges the received signal. On the other hand, it causes the excess oscillation due to the resonance phenomenon as shown in Fig.6. In order to suppress the excess oscillation, MOSFETs  $M_2$  and  $M_3$  are employed. Timing signals  $t_1$  and  $t_2$  in Fig.6 control the  $M_2$  and  $M_3$ , respectively. Thus, they short out  $L_1$  and  $L_2$  at the timing as shown in Fig.6 and can suppress the excess oscillation.

The timing signal  $t_1$  for transmitter has same phase of transmission data. On the other hand, the timing signal  $t_2$  should be tuned to the timing of the receiving data. The timing tuning can be realized by multiple phase oscillator and multiplexer as shown in Fig.7. Data-transmitting cycle is divided into eight phase by the ring oscillator composed of differential delay cells in 4 stages, as shown in Fig.8. The multiplexer selects the optimum clock phase among the eight phase clocks. The 125ps phase resolution is sufficient for 1Gbps transmitting and the timing control can be achieved digitally.

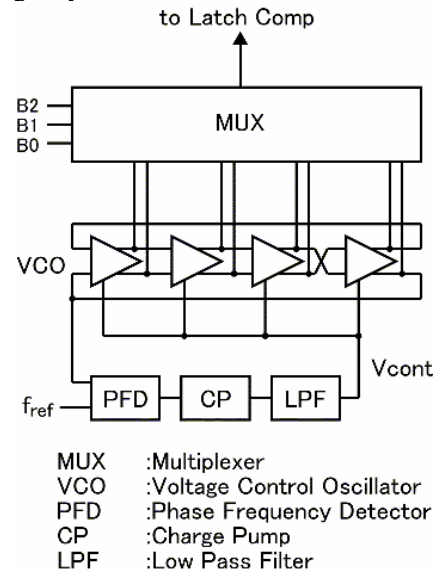


Fig.7 Timing tuning circuit

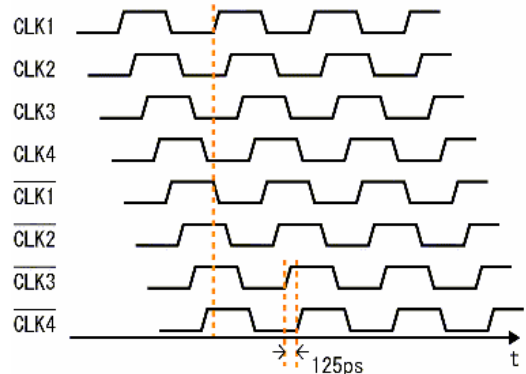
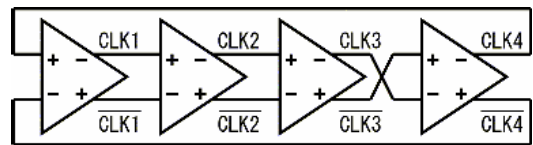


Fig.8 Ring oscillator and eight phase clocks.

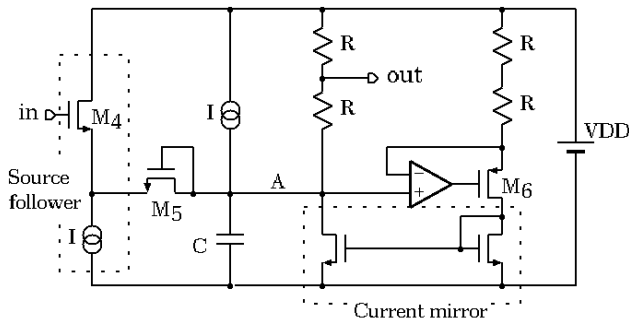


Fig.9 Reference-voltage generator.

The transmitter circuit and the receiver circuit including spiral inductors have been designed in TSMC 0.25 $\mu\text{m}$  mixed-signal CMOS technology and they were simulated by SPICE. In the simulation, the equivalent model of the spiral inductor pair is used. The supply voltage VDD is 2.5V, in all simulations. Fig.6 shows the simulation results. As shown in the lowest stage of Fig.6, the excess oscillation can be successfully suppressed, although the leakage of the timing signal  $t_2$  through the parasitic element of  $M_3$  causes a slight oscillation. The resonance property can enlarge the amplitude of the received signal and it results in lower power consumption. In fact, an average of the current flowing into the driver  $M_1$ , which consumes the most power, can be reduced down to 2.4mA.

The distance between stacked chips should be varied due to system level restrictions such as heat dissipation. It affects especially the amplitude of the received signal. In order to suppress the affection, a reference-voltage generator is proposed. Fig.9 shows the circuit diagram. It can generate a reference voltage for the comparator from the amplitude of the current received signal. A source follower buffers the received signal. Simultaneously, the voltage level is shifted down by the threshold voltage of the MOSFET  $M_4$ . Moreover, a peak voltage is detected by a MOSFET  $M_5$  which operates as diode. Because the level-shift voltage of the source follower is equal to the threshold voltage of  $M_5$  working as diode, a peak voltage

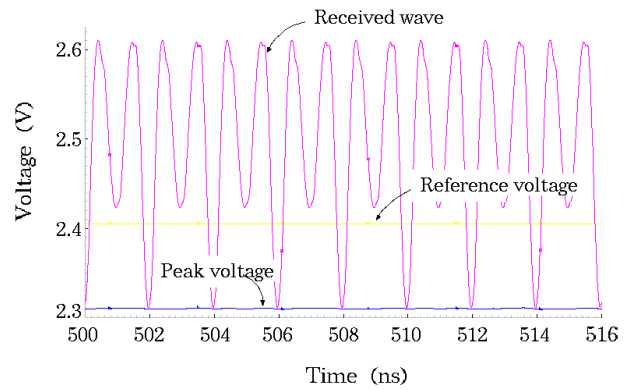


Fig.11 Simulation result of the reference-voltage generator.

of the received signal can be obtained at the node A. The reference voltage for the comparator is generated by dividing the peak voltage into 1/2. However, the behavior of the reference-voltage generator is influenced by data sequence pattern. The good operation can be achieved in the sequence "...1,0,1,0,1,0,...". In order to overcome this phenomena, channel bank is employed, in which one channel is exclusively used for the reference-voltage generation. The channel bank is illustrated in Fig.10. The control channel transmits the data sequence "...1,0,1,0,1,0,..." and it is exclusively used for the reference-voltage generation. In the other channels, the latched-comparators in the receivers evaluate the data via the reference voltage generated by RVG in the control channel. The simulated results of the reference-voltage generator are shown in Fig.11 and a proper reference voltage can be obtained.

A simulation result of the communication channel including the output of the comparator is shown in Fig.12. In the first stage, the data sequence in the transmitter is described. In the middle stage, the received wave and the reference voltage are described. In the bottom stage, the received data sequence is described and it is same as the transmitted data sequence except the phase shift. Thus, the good performance has been confirmed.

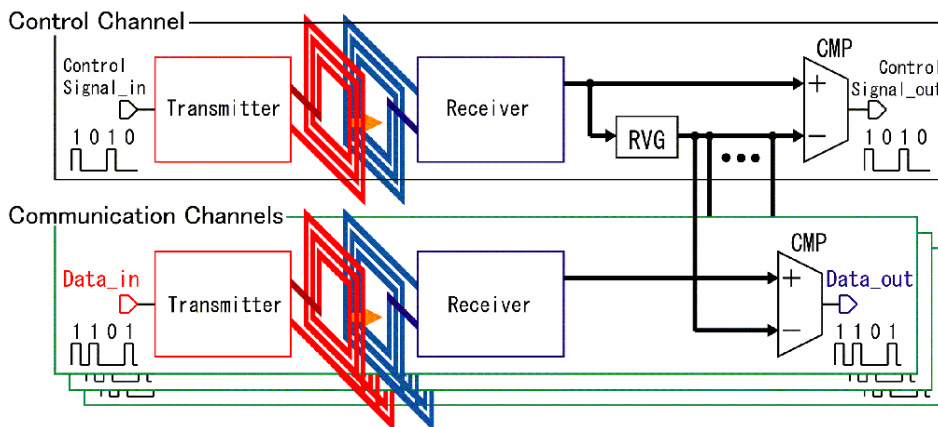


Fig.10 Channel bank employing same reference voltage

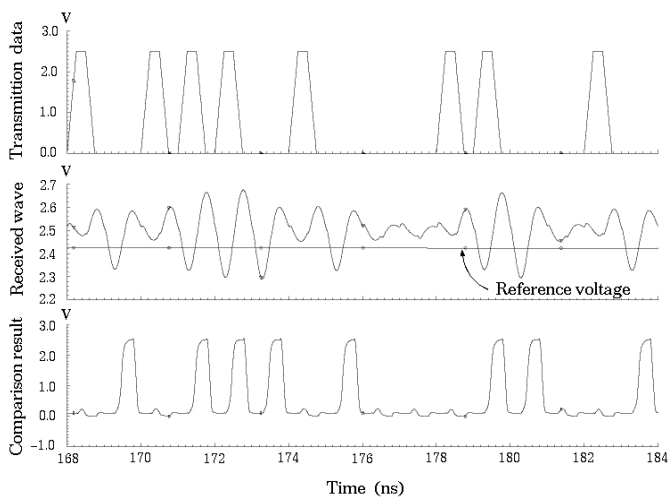


Fig.12 Simulation result of the communication channel.

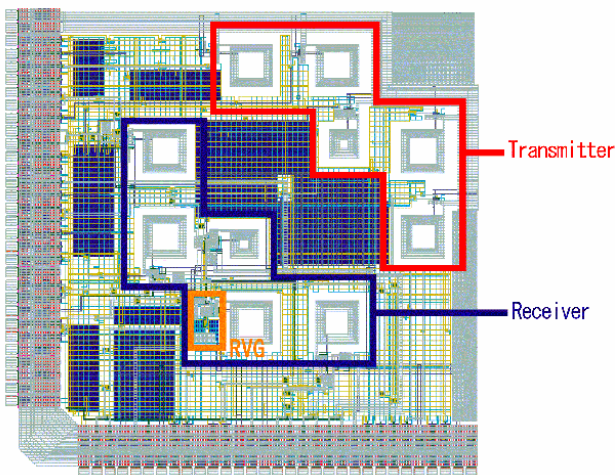


Fig.13 Chip layout

A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the proposed concept. The chip layout is shown in Fig.13. The evaluation board also has been developed and it is shown in Fig.14. Two evaluation boards are placed in face-to-face and the performance of the communication will be evaluated.

### 3. Conclusions

We have presented an interconnect scheme between the stacked chips based on resonant coupling of the integrated spiral inductor pair. The performance, 1Gb/s/channel at 9mW/channel, has been confirmed by SPICE simulation. A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the communication of the spiral inductor pair. The experiment with the fabricated chips will be accomplished soon.

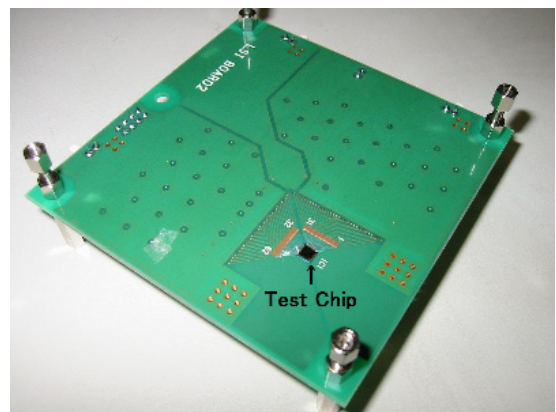


Fig.14 Evaluation board

### 4. Future plan

The next studies are "Size-reduction of the spiral inductor" and "less power consumption", which are necessary conditions for more multiplex channel communication. 100 channels for multiplex communication, 100mmx100mm size for spiral inductor, and 1mW power consumption per channel are next targets.

### References

- [1] J.Burns, *et al.*, *ISSCC Digest of Tech Papers*, pp.142-143, Feb. 2001.
- [2] K.Kanda *et al.*, *ISSCC Digest of Tech. Papers*, pp.186-187, Feb. 2003.
- [3] A.B.M.H.Rashid, *et al.*, *IEEE Electron Device Letters*, Vol.23, No.12, pp.731-733, Dec. 2002.
- [4] D. Mizoguchi, *et al.*, *ISSCC Digest of Tech. Papers*, pp.142-143, Feb. 2004.

### 5. Published Papers and Patents

#### ① Published Papers

#### ② Proceedings

1. M. Sasaki, D. Arizono, A. Iwata, "A wireless chip interconnection using resonant coupling between spiral inductors," *Proc. of Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing*, (2004) pp.104-108.
2. M. Sasaki, *et al.*, "At-speed self-test LSI for high-speed serial link," submitted to *2004 International Conference on Solid State Devices and Materials (SSDM)*.

#### ③ Patents

1. Japanese Patent 2004-10053, "Semiconductor Equipment"