A Study on Neural Sensing System

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1. Research Target

For advanced clinical and biometrics applications, various implantable neural sensors are fabricated by CMOS-LSI technologies [1, 2]. However the CMOS device has a large flicker noise and deviation of threshold voltage, CMOS Operational-amplifier (Opamp) hardly amplifies a weak neural signal. Thus the system has to implement a low-noise amplifier which can reduce these noises. Moreover, the implantable systems need a reception of system control-commands and a transmission of sensor data using a wireless communication.

In this paper, we propose the architecture of a neural sensing system, which includes low-noise amplifier and wireless transceiver implemented with a conventional CMOS technology. This study is related to RF analog circuits technology of 21st century COE program Hiroshima University.

2. Research Results

2.1 Neural Sensing System Architecture

The block diagram of the proposed neural sensing system is shown in Fig. 1. The system consists of the MUX/AMP block, 10-bit ADC, wireless TX/RX block and system control block. The multi-channel probe and wireless antenna are implemented by discrete devices.

The MUX/AMP block needs about 80-dB voltage-gain and a reduction of a flicker noise and a voltage offset, because the neural signals are typically a few ten-μV and a few kHz. In addition, the MUX/AMP block chooses any 5-channels from the multi-ch probe and the selected channels are multiplexed at a pulse width of 20-μs in order to observe the neural signals simultaneously. The ADC converts the multiplexed signal to digital data at 10-bit resolution and 10-k-sampling-per-sec (ksps) sampling rate per channel. Therefore, the system can analyze a propagation of neural signals in the large neural network.

The TX/RX block needs to transmit a measurement data to the external receiver; and the block also receives a system control data, such as a measurement channel selection and voltage-gain control, from the external transmitter. Therefore the TX/RX block consists of transmitter (TX), receiver (RX) and voltage-controlled oscillator (VCO). The data transmission rate of neural sensing system is 500-kbps, because the ADC is operated at 10-bit resolution and 10-ksps sampling rate. In order to achieve the high-transmission rate, the VCO supplies a carrier signal of 100-MHz to the TX/RX block.

2.2 Design and Test-Chip Evaluation Results

A test-chip of the proposed neural sensing system was designed and fabricated with a 0.35-μm 2-poly 3-metal CMOS technology.

The block diagram of MUX/AMP block is shown in Fig. 2. The MUX/AMP block, which is implemented using a direct chopper input scheme, is possible to detect a neural signal through a polarized charge of probe interface. Moreover, the chopper technique reduces the flicker noise and dc-offset voltage of Opamps. The MUX/AMP block amplifies a difference between a detected voltage nearby focused neuron and a reference voltage (Vref) defines a voltage of cell liquid far from the observation neuron cell. From the SPICE simulation, the chopper amplifier achieved an equivalent input noise of 23 nV/root-Hz at a 400-kHz chopper frequency. A total in-band noise (~100 kHz) was 7.2 μV.

The TX/RX block diagram is shown in Fig. 3. The TX block transmits the ADC output data to the external receiver using the binary phase-shift-keying (BPSK) modulation. And this block equipped with the modified frequency-modulation (MFM) encoder, because the MFM achieves about 50-% mark ratio of transmission data.

Figure 4 shows the microphotograph of the test chip. The test chip includes a MUX/AMP block, an ADC block and a TX block, and the chip area is 25-mm^2. Measured Output spectra of TX block with BPSK modulation is shown in Fig. 5. The VCO operated at a frequency of 110.6-MHz, and the TX block achieved the data transmission rate of 1 Mbps. The power dissipation of VCO is 0.6-mW at a supply voltage of 3 V.

We evaluated the proposed MUX/AMP block to measure a nerve fascicle of cricket foot. Figure 6 shows the measured waveforms of (a) an amplifier implemented by commercially discrete Opamps and (b) the proposed MUX/AMP. The amplifier has a 66-dB DC-gain and band-pass-filter with 20-Hz to 5-kHz bandwidth. The external curve of pulse signal shows a measured neural signal. The proposed neural sensing system achieved a detection of the neural signal. The MUX/AMP accomplished a 66-dB voltage-gain, 3.2-μV in-band noise (~100 kHz) and 6.0-mW power dissipation at a supply voltage of 3-V.

3. Relation between COE Program and Results

The Planned image recognition system implemented by 3-dimensional custom stack of multi-chip that needs the technology of biometrics and RF interface. Therefore, these research results are adapted to the circuit design and the architecture in the planned prototype system.

4. Conclusions and Plan for the Future

We proposed the architecture of a neural sensing system, which includes low-noise amplifier and wireless transceiver implemented with a conventional CMOS technology. The proposed system achieved the RF data transmission rate of 1-Mbps and observation of

neural signals. In the future, we study for lowering noise of sensing system, in order to realize an observation of a few-μV neural signal.

References

[1] K. D. Wise, Symp. on VLSI Circuits Dig. of Tech. Papers, pp.106-109, 2002.

[2] J. A. V. Arx, et al., ISSCC Dig. of Tech. Papers, pp.214-215, 1999.

3. Published Papers and Patents

① Published Papers

1. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels", IEICE Trans. Fundamentals., vol.E87-A, pp.376-383, Feb. 2004.

② Proceedings

1. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels", Proc. of Workshop on SASIMI, pp. 206-210, 2003.
2. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, "Neural-Sensing LSI with Wireless Interface", Proc. of the 2nd Hiroshima International Workshop on Nanoelectronics for tera bit Information Processing, pp.22-23, Hiroshima, 2004.1.

③ Patents and Others

1. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Wireless-Neural Sensing LSI", Tech. Report of IEICE, ICD2003-86, Toyohashi, 2003. 9.

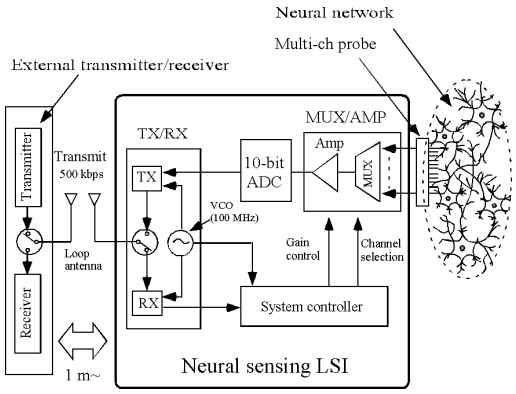

Fig.1 Proposed system architecture.

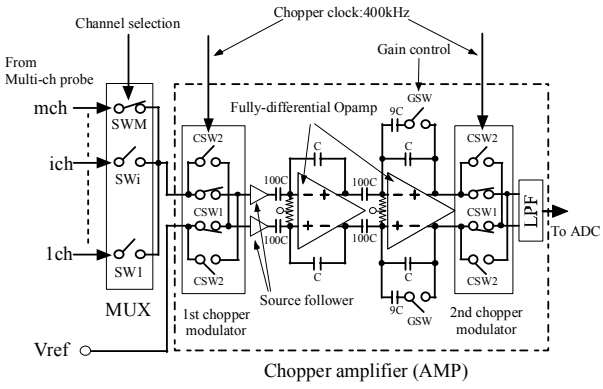

Fig.2 Schematic of the MUX/AMP block.

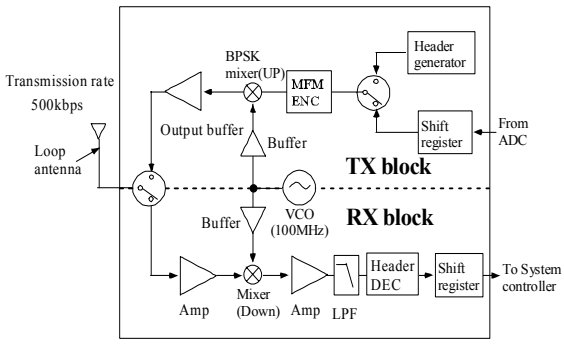

Fig.3 TX/RX block diagram.

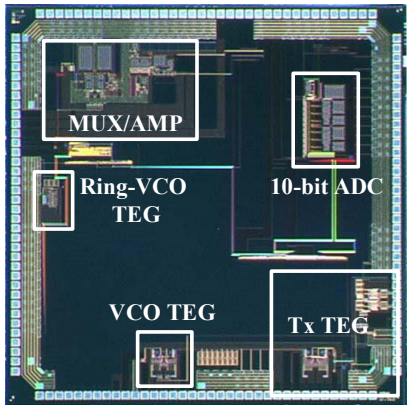

Fig.4 Microphotograph of the test chip.

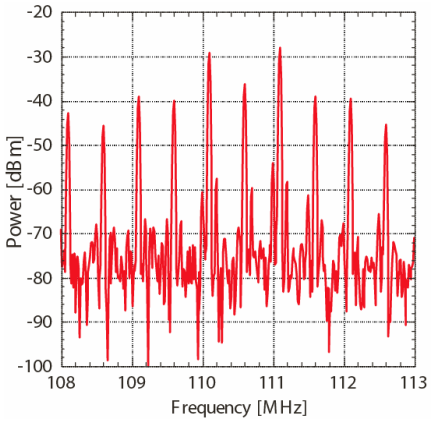

Fig.5 Measured output spectra of TX block.

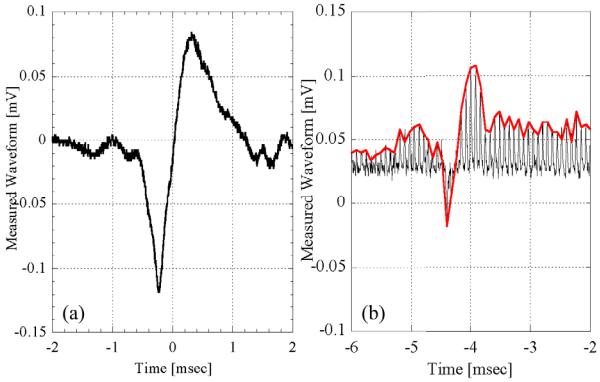

Fig.6 Measured nerve facile waveform of (a) the amplifier implemented by the discrete Opamps and (b) the proposed MUX/AMP.