# CDMA Serial Communication Chips for Highly Flexible Robot Brain

Mitsuru Shiozaki(Graduate School of Advanced Sciences of Matter, D4),
Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter),
Mamoru Sasaki (Associate Prof., Graduate School of Advanced Sciences of Matter)

## 1. Research Target

Various serial interface standards, e.g., USB, IEEE-1394, etc have been established for multimedia applications. However, they do not have sufficient feature for robot control systems, in which various sensors, imagers, actuators and processors are connected as network. The robot control network requires real-time communication so as satisfy the restriction on the sampling time. Furthermore, it has communicated various amounts of data, e.g., commands to the actuators being little amount and huge image data from the imagers, etc. In addition, the network should be implemented with a few wiring lines, so that the actuators can smoothly move.

We propose a communication scheme suitable for the robot control system. A key idea is CDMA serial communication. The CDMA technique is used for data multiplexing and it realizes many virtual paths on the single wiring.

Several researches have been reported, in which CDMA scheme has been implemented with wired communication [1] [2]. CDMA has been implemented with bus configuration in [1]. In the case of the robot control system, if the bus configuration is adopted, the impedance matching becomes very difficult and it results in low data-transfer rate. CDMA scheme has been employed on serial link in [2] and high data transfer rate can be expected in the combination. However, if the number of multiplexing increases, the synchronization between the transmitter and the receiver becomes difficult. Although CDMA scheme has been employed, it has not achieved a lot of multiplex communication in [2]. It is very difficult that the synchronization technique developed for conventional serial link is employed for the CDMA serial link, because it seems to be PAM (pulse amplitude modulation) system with many amplitude steps. We propose a two-step synchronization technique, code synchronization and chip synchronization, which is based on the technique in the conventional CDMA system, not in the conventional serial link.

## 2. Research Results

The code synchronization can adjust the start timing for the decoding (despreaded) operation to the received sequence and it corresponds with the initial acquisition process in conventional CDMA system. The chip synchronization employs DLL (Delay Lock Loop) with a 2-delta delay discriminator and it can adjust the pulse timing. The receiver chip's block diagram is shown in figure 1. The number of the wave samplers is equal to the length of the spread codes. The multiple clocks control the de-interleaved timing and they are given by the ring oscillator, although the MUX and the voltage-controlled delay circuits exist between the wave samplers and the ring oscillator. The MUX and the voltage-controlled delay circuits are needed for the synchronization.

The receiver chip was fabricated in a 0.25um digital CMOS technology to demonstrate a 2Gbps, 7-multiplexing CDMA serial link. The 2.4mmX4.0mm die photo is shown in Figure 2. The amplitude of the transmitted differential signal for one code is set to 100mVp-p and the multiplexed wave has 800mVp-p swing because the number of codes is 8. Because the 2Gbps signal is de-interleaved into the 8 wave samplers, the decoders operate at the 250MHz system clock. The ring oscillator consists of 8 stages.

Figure 3 shows the measurement results of the first one of the sampler clocks. The left and right are the sampler clocks during the code synchronization and during the chip synchronization, respectively. Because the clock is always shifted by MUX during the code synchronization, the 8 phases of the clock overlap each other. On the other hand, the phase is fixed during the chip synchronization. The measurement results of the differential control voltages Cnt+ and Cnt- for the voltage-controlled delay circuits are also shown in Fig.3. They are fixed at 1.9V and 0.7V during the phase of the code synchronization. Cnt+ and Cnt- are adjusted and locked in the DLL, during the phase of the chip synchronization.

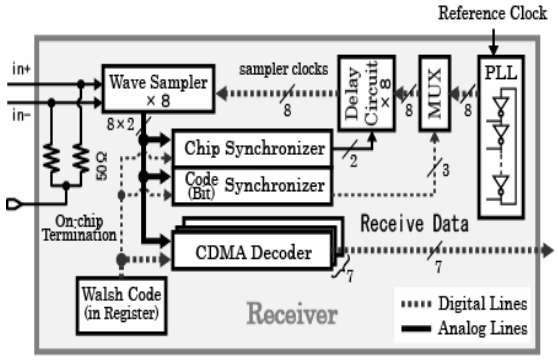


Fig.1 A block diagram of the CDMA serial receiver chip.

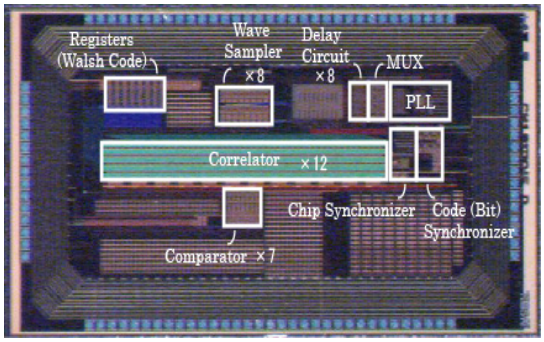


Fig.2 Chip micrograph.

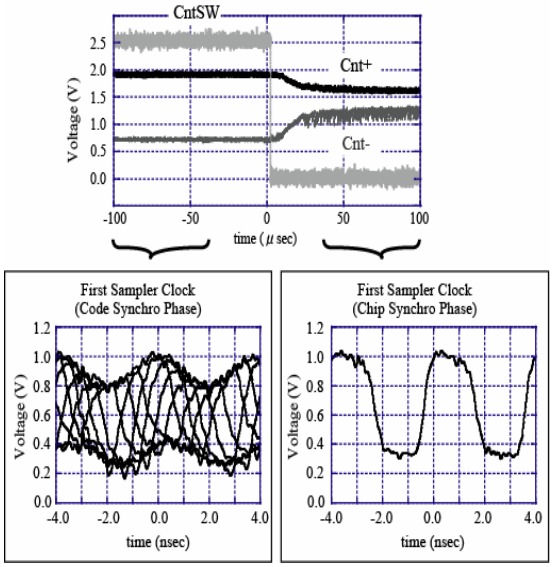


Fig.3 Measurement results.

## 3. Summary and future plans

A 2Gbps and 7-multi-plexing CDMA serial interface and the receiver circuit are proposed. The key techniques of the receiver chip are the two-step synchronization and its circuit implementation. The receiver chip fabricated in a 0.25um digital CMOS technology achieves a 2Gb/s data-transfer rate and synchronization of 7 multiplex communications.

Now, we are designing a transmitter chip based on the proposed serial CDMA scheme in order to demonstrate the CDMA serial link in the completed form.

## 4. Relation between COE program and our results

A network in the robot has few examples of use other than wired communication. These reasons are that an incorrect operation and reckless run of the robot are caused by the noise generated from other equipments. So, wired communications are excellent in an intelligence leak, a noise or cost. But it is not suitable for real-time communication with the 3D-integrated-system developed by the COE program. In addition, there is also a physical problem of wiring. In such a case, chips of this research are effective.

## References

[1] R.Yoshimura et al. "DS-CDMA Wired Bus with Simple Interconnection Topology for Parallel Processing System LSIs," ISSCC Digest of Tech. Papers, pp.370-371, Feb. 2000

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## 5. Published Papers and Patents

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2. M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, “A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System,” 2004 Symposium on VLSI Circuits. (This will be presented on Jun. 18, 2004. [Session 13-1])