TEG Design for HiSIM Model-Parameter Extraction and Parameter Extraction with Single Structures

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1. Research Target

Our COE project aims at fusion of silicon-based nanodevice, circuit and chip-architecture research. For realizing the fusion, we develop HiSIM-Microwave, a transistor model valid for RF applications including possibility to simulate optical responses as well as electromagnetic response . As a first step for the realization, we have designed TEGs (Test Element Groups) with the 0.18μm TSMC technology for extracting HiSIM model parameters to be used both for circuit design and device design. The designed TEG was fabricated by TSMC, and measurements and their analysis were performed.

For accurate RF-circuit simulation, HiSIM has to be accurate, and the model parameter values have to be reliable. With TEG measurements, we will check the quality of HiSIM for advanced devices such as for RF devices, as well as the reliability of model parameter extracted from measurements.

2. Research Results

Fig. 1 shows designed TEG blocks in 3x3mm^2 area. A large area, about 1/3 of the total area, is used for single MOSFET structures. These blocks consist of different single-MOSFET sizes, different gate lengths and widths. These measurements are used to extract general device features valid for any sizes. Since HiSIM description is scalable for any MOSFET sizes, the number of the transistors required in TEGs is not so many as usually prepared.

We have also designed couple of TEG blocks for high-frequency measurements. For the accurate measurements, to exclude external contribution is the key. TEGs have been designed to fulfill the requirements.

Additionally a block was designed by a designer group, where real RF-circuit-performance tests are available.

Fig. 2 shows statistics of measured threshold voltage from 16 chips of p-MOSFET with gate length of 0.18μm. Extremely large variations are observed. This means the technology is not yet mature for the shortest design rule.

3. Summary

Figs. 3-7 show comparison of measured current-voltage characteristics with HiSIM calculation results for five different gate lengths, from long to short . For the calculation only one model parameter set is applied for any device sizes. It is seen that the extracted HiSIM parameters reproduce measurements within variations among chips.

4. Future Plan

As the second step, high-frequency measurements will be performed and the HiSIM validity for the measurements will tested.

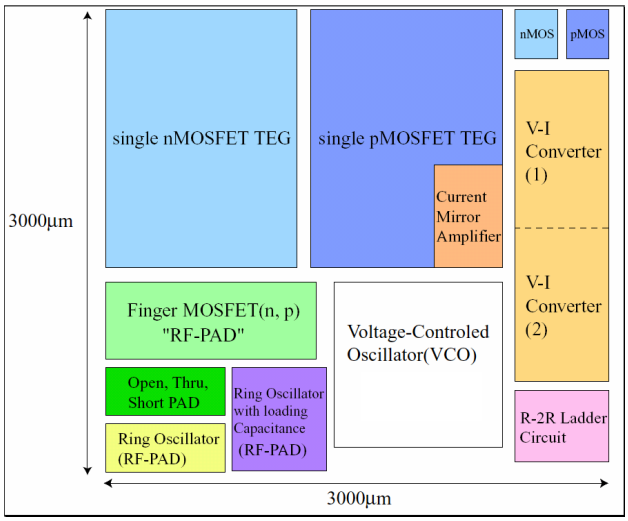

Fig. 1. Designed chip layout

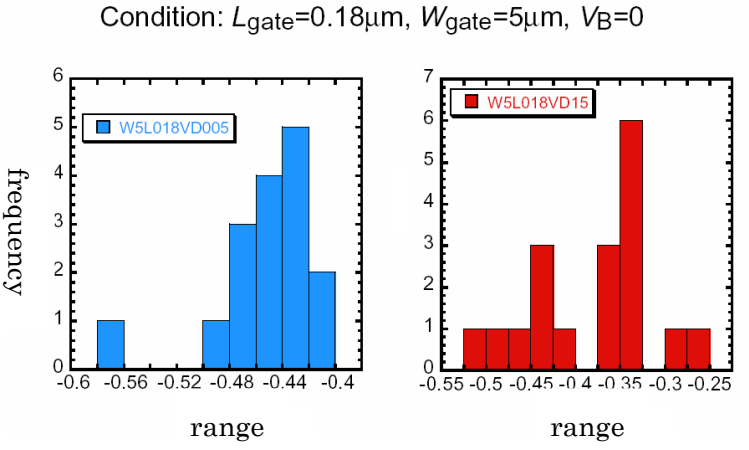

Fig. 2. Measured statistics from 16 chips.

Figs. 3-7. Comparison of measured I-V characteristics with HiSIM calculation results.

Fig3.

$L_{channel}$=2.0μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

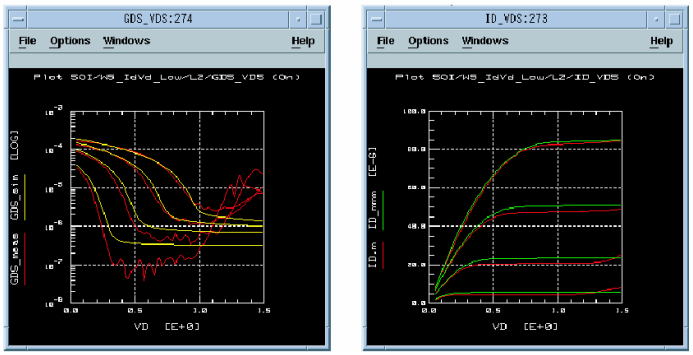

Fig4.

$L_{channel}$=0.70μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

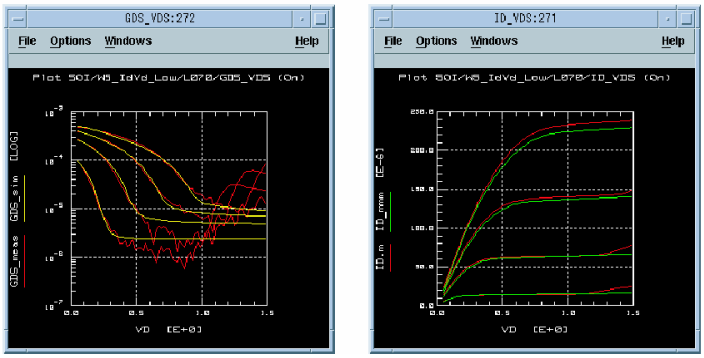

Fig5.

$L_{channel}$=0.50μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

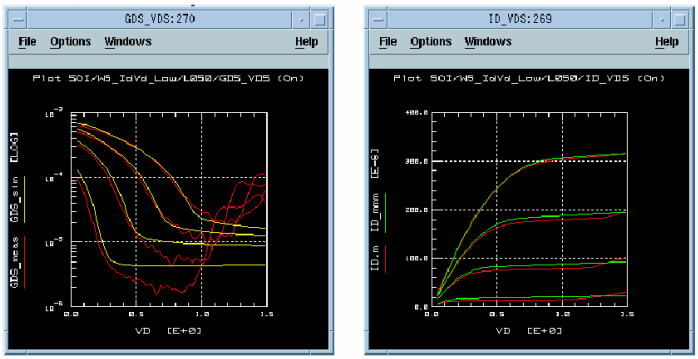

Fig6.

$L_{channel}$=0.30μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

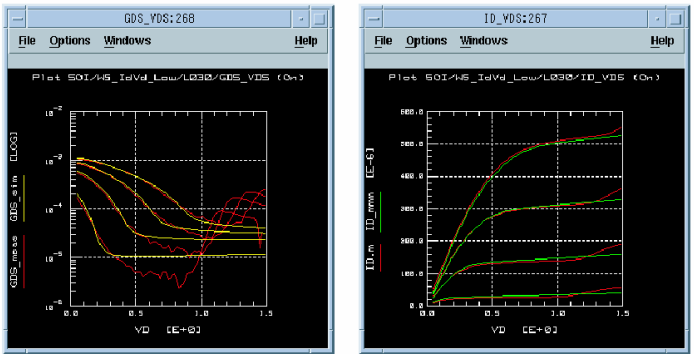

Fig7.

$L_{channel}$=0.18μm, W=5.0μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step