Inversion Charge Model of SOI-MOSFET for Circuit Simulation and 1/*f* Noise Analysis

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1. Research Target

The MOSFET is the most widely applied device, and possible future variations such as double-gate MOSFET as well as FinFET have been intensively investigated [1]. Their models for circuit applications are now under development with different applications[2]. Our objective is to develop a circuit simulation model for the fully-depleted SOI-MOSFET as the first step for describing phenomena caused by the channel confinement between two oxide layers. Advantage of pursuing the fully-depleted SOI-MOSFET is that the modeling accuracy is easily verified by measured characteristics of production-level SOI-MOSFET technologies.

Existing SOI-MOSFET models are suffering convergence problems in circuit simulation. The main reason is a violation of the charge conservation. The SOI-MOSFET has three important Si-SiO_2surfaces as can be seen in Fig. 1 . Charges are induced at all surfaces. Thus surface-potential-based modeling is the only solution for the SOI-MOSFET to secure the charge conservation in a consistent way. We have developed the SOI-MOSFET model HiSIM-SOI based on this charge conservation guideline. Our investigation here focuses on carrier density changes in the SOI channel in comparison to the bulk-MOSFET. For this purpose the 1/*f* characteristics are studied, since the 1/*f* noise is sensitive to the carrier concentration as well as its density distribution in the channel[3].

2. Research Results

To include all device features of the SOI-MOSFET accurately, HiSIM-SOI determines not only the surface-potential at the channel surface, but also at the back side, as well as at the bulk back-gate self-consistently as schematically depicted in Fig. 1 [4]. The total iterative potential calculation requires only about twice as much calculation time as for the bulk-MOSFET case, solving just at the channel-surface. Fig. 2 demonstrates the accuracy of the three calculated

Surface potentials in comparison to the results with the 2D-device simulator MEDICI. Fig. 3 compares HiSIM-SOI simulation results of the channel-inversion charge with MEDICI for two silicon-layer thicknesses T_{SOI}. The bulk-MOSFET result is also depicted for comparison. Enhancement of the carrier concentration is obvious. The model reproduces measured *I-V* characteristics within numerical accuracy as shown in Fig. 4, and is verified to show stable convergence in circuit simulation.

Fig. 5 compares simulation result of the 1/*f* noise with measurements. For the HiSIM-SOI simulation two model parameters are fitted: *NFTRP* determining the magnitude of the 1/*f* noise; and *NFALP* determining the contribution of the mobility fluctuation due to carrier trap/detrap. The fitted *NFTRP* value is the nearly the same as that of the bulk-MOSFET, and *NFALP* is very small in comparison with *NFTRP* but about 10 times larger than for the bulk-MOSFET. Good agreement of the measured and simulated noise-voltage characteristics is the proof of accurate calculation of the carrier concentration and its distribution along the channel. Deviation of three measurement points (open triangles) from simulation results is attributed to impact ionization, which is not yet included in HiSIM-SOI.

Comparison with the bulk-MOSFET is shown in Fig. 6. Increased noise density is obvious and explained by the higher carrier concentration in the channel, as evident from Fig 3. Fig. 7 shows the expected noise increase for reduced T_{SOI}, which will cause serious problems in circuit applications.

3. Summary

Reduction of T_{SOI} enhances the driving capability of the SOI-MOSFET. However, we have found the necessity of considering a trade-off between the driving capability and the 1/*f* noise. The enhanced noise due to the increased carrier concentration, caused by the inversion-layer confinement, will also cause serious problems in future devices such as the double-gate MOSFET and the FinFET.

4. Future Plan

Accuracy and stable convergence of the developed HiSIM-SOI will be checked with real circuits.

Reference

[1]T. –J. King, Ext. Abs. SSDM, p.280, 2003.
[2]M. Chan et al., Proc. MSM, p.280, 2003;
T. Nakagawa et al., ibid, p.330, 2003.
[3]S. Matsumoto, Master Thesis, Hiroshima University, March 2003.
[4]D. Kitamaru et al., Jpn. J. Appl. Phys., in press, April 2004.

5. Papers and Presentation

Presentation

N. Sadachika, Y. Uetsuji, D. Kitamaru, L. Weiss, U. Feldmann, S. Baba, H. J. Mattausch, M. Miura-Mattausch, “Fully-Depleted SOI-MOSFET Model for Circuit Simulation and Its Applications to 1/f Noise Analysis,” Proc. Simulation on Semiconductor Processes and Devices, 2004.

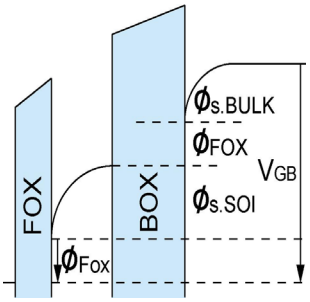

Fig. 1. Schematics of the fully-depleted SOI-MOSFET. The three surface potentials are solved iteratively with the Poisson equation.

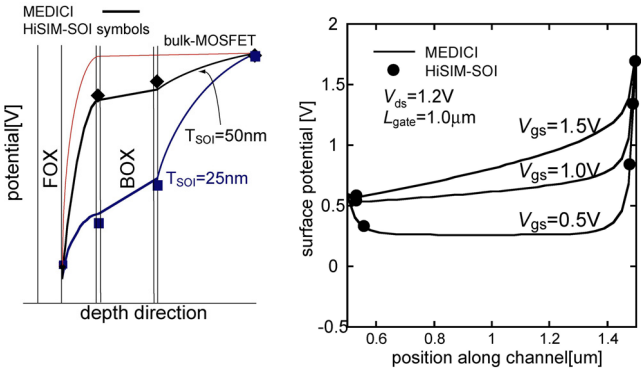

Fig. 2. Comparison of HiSIM-SOI calculated surface potentials with the results of the 2D-device simulator MEDICI.

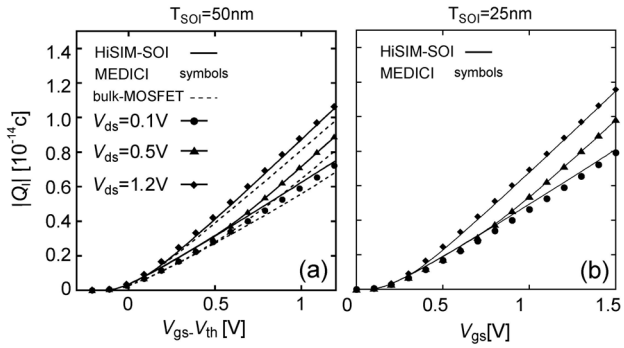

Fig. 3. Comparison of calculated inversion charge Q_I with MEDICI results, for a silicon-layer thickness of (a) 50nm and (b) 25nm. The bulk-MOSFET result is plotted in addition in (a).

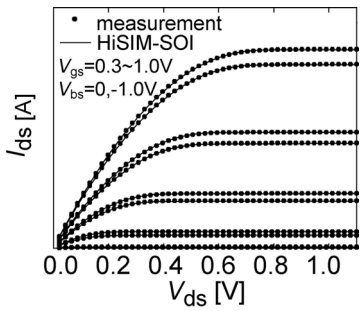

Fig. 4. Calculated drain current I_{ds} as a function of drain voltage V_{ds}. Symbols are measurements.

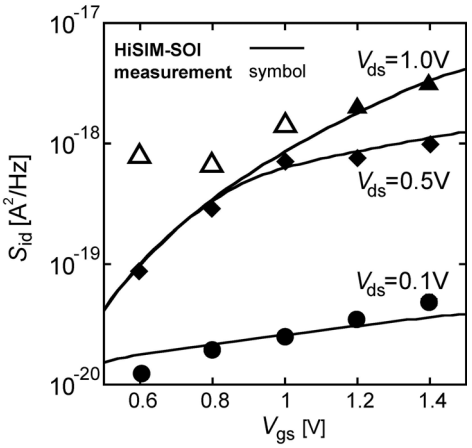

Fig. 5. Calculated 1/*f* noise density as a function of gate voltage V_{gs}. Symbols are measurements. Deviation of the three open triangles from the HiSIM-SOI result is attributed to impact ionization, which is not yet included in HiSIM-SOI.

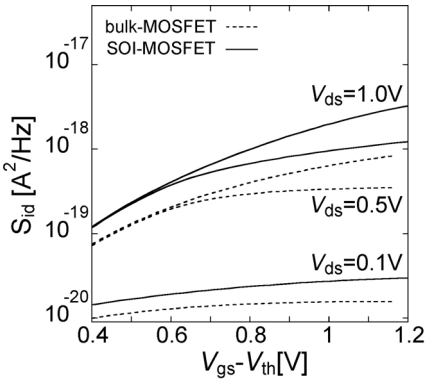

Fig. 6. Comparison of calculated 1/*f* noise for the fully-depleted SOI-MOSFET with that of the bulk MOSFET.

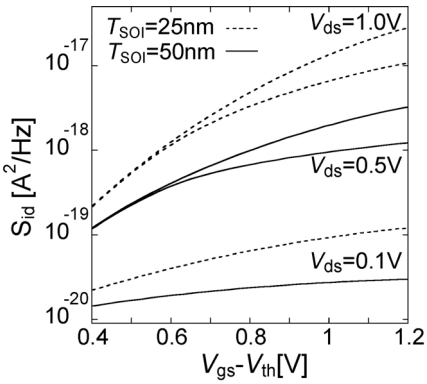

Fig. 7. Comparison of calculated 1/*f* noise for the different SOI-layer thicknesses.