Investigation on hard breakdown mechanism of high-k gate by conductive-AFM

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1. Research Target

Following the device scaling laws, continuing scaling down of the MOSFET device with the minimum feature size of 90 nm and below would require equivalent oxide thickness of less than 15A. SiO_2 will soon reach its physical limitation such as high leakage current and reliability concerns. High-k materials with high physical thickness have been widely researched as gate to alternative Silicon oxide. So far, a lot of works focus on silicon oxide breakdown mechanism, but it is few for high-k dielectric, which is very important to high-k transistor reliability.

In ours work, high-k MIS structure hard breakdown path was investigated by conductive-AFM with conductive tip. According to the path area, leakage path density and the I-V curve of leak spot from conductive-AFM result, high-k hard breakdown mechanism will be analyzed following the experiment data.

2. The Connection with COE Program and Achievements

High-k material will be applied to quantum dot memory device as the control oxide layer. In my group this work is in progressing. High-k breakdown mechanism will supply theoretical support with the application of high-k to dot memory.

3. Research Results

MIS capacitance with stack high-k gate of HfAlO/SiON were made in this work. Fig.1 shows the MIS structure.

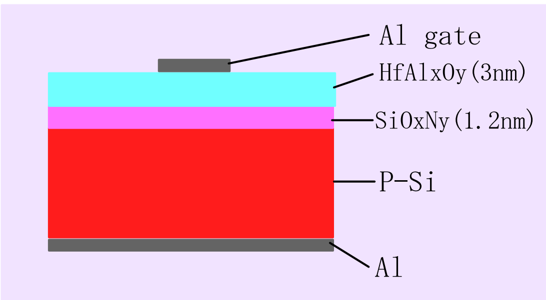

Fig.1 Schematic diagram of stacked high-k gate MIS structure

Hard breakdown was happened at about –4.5 volt showed as fig. 2, the EOT of high-k film was estimated about 2.1nm by C-V characteristic curve (fig. 3). The breakdown electric field was about 20MV/cm. The leakage current was increased significantly after hard breakdown.

Conductive filament path was employed as hard breakdown mode. In this mode, silicon and metal filament path was supposed. According this mode, the leakage current density function after hard breakdown is given by

JpostHD＝(1-Aratio)JFN＋AratioJSM

Where Aratio is the proportion of hard breakdown path area with gate total area, JSM is the schottky current density at breakdown leakage spot.

The Aratio was estimated about less than10^{-7}, in gate area, presumably there are only one or two leakage spot, which means one or two leakage channel through the hard breakdown. In the work, samples with 1 mm diameter gate were fabricated, but searching the leakage spot will be difficult. Because the resolution limit of equip, By far I haven’t found the spot by conductive-AFM.

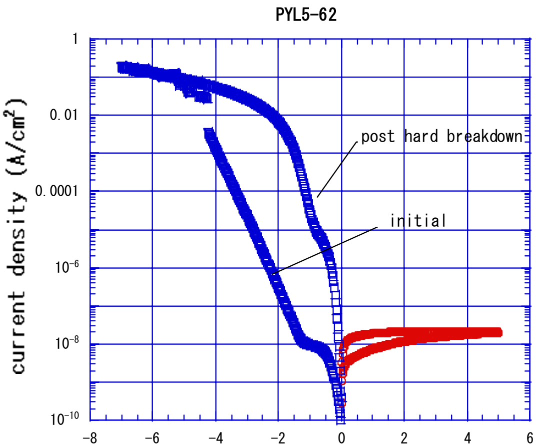

Fig.2 characteristic of current-voltage

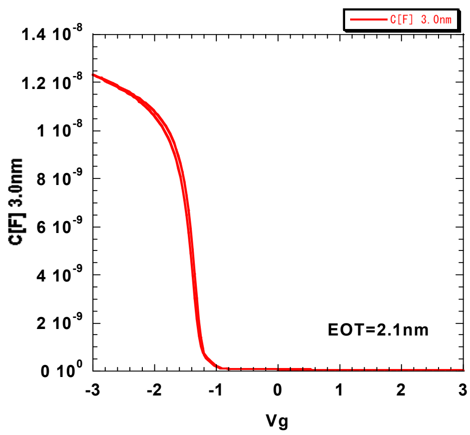

Fig.3 characteristic of capacitance-voltage

4. Research Plan in Future

We consider shrinking the gate area, and then search the hard breakdown path by conductive-AFM to confirm the mechanism of high-k breakdown.

In further, we will apply the high-k to dot memory, and study the characteristic of high-k dot memory (high-k as alternative of CVD silicon oxide in conventional dot memory device).

Reference

1. Breakdown Modes and Their Evolution in Ultrathin Gate Oxide, Jpn. J. App. Phys. Vol. 41 (2002) pp. 5957-5963.