Intra/Inter Chip Wireless Interconnect System for ULSI (2)
－A CMOS Ultra Wideband Transmitter－

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1. Research Target

The delay time associated with the parasitic resistance, capacitance and inductance of conventional interconnect system will become the primary obstacle for high speed data and clock distribution among different sub-circuits within a chip and among the chips for future ULSI. Thus a new design or technology solution must be adopted to overcome the delay problem of conventional interconnect system. An ultra wideband (UWB) wireless interconnect systems using integrated antenna shown in Fig. 1 could be a novel solution to avoid any parasitics delay [1] for future ULSI.

In this study we report a single chip UWB transmitter circuit based on time hopping spread spectrum technique [2] for wireless interconnect system as shown in Fig. 2. Thus a new technique based on CMOS technology is also developed to generate the monocycle pulse with a target monocycle pulse center frequency of 5 GHz. As a result, it leads us to design a single chip transmitter for developing the intra/interchip wireless interconnect system of future ULSI.

2. Research Results

This transmitter transmits very short duration Gaussian monocycle pulses with wide bandwidth as a signal without a sinusoidal carrier. The circuit simulation is done from the extracted layout netlist of designed transmitter by HSPICE for TSMC 0.18 μm CMOS process. The simulation results are shown in Figs. 3–10. The frequency stability of the frame clock generated by VCO is an important factor in UWB system. From simulation it is found that the frequency stability with change of V_{dd} and temperature is about 5% in the worst case. The phase noise of the VCO for 100KHz offset is found as about –93.6 dBc/Hz. Precise delay generation is required to generate the time shifting frame clock. Thus voltage controlled delay line is used and its response is shown in Fig. 5. Linear feedback shift registers which consists of four clocked D-type Flip-Flop along with an exclusive-or logic is designed to generate pseudorandom (PN) sequence. It is observed that the generated PN sequence satisfies all its randomness properties such as balance , run and co-relation property. The 8 to 1 multiplexer which is designed using NAND and NOR gate selects the time hopped frame clock according to PN sequence. The time shifted pulse train due to PN sequence and PPM is obtained from the output of 2 to 1 multiplexer. The monocycle pulse generator circuit consists of RLC network with RC filter, pass gate and short rectangular pulse (SRP) and Gate Control Pulse (GCP) generator is designed as shown in Fig. 8 to produce damped sinusoidal like waveform from the time hopped signal (THS) which contains information. The Fig. 9 shows that the generated monocycle pulse (MCP) is symmetry. The FFT of the generated monocycle pulse reveals that it has wide bandwidth characteristics as shown in Fig. 10. The designed transmitter performance data are given in Table. I. The chip die photograph is shown in Fig. 11.

Table I: Transmitter performance data

UWB system	Time hopping Impulse
Carrier Frequency	No carrier
Transmitter Signal bandwidth	3.3 GHz
Data rate	50 Mbps
Single Channel bandwidth	400 MHz
Modulation	Pulse position modulation
Average power consumption	12.5 mW @1.8v
Architecture	All digital except pulse generator
Technology	TSMC 1.8v, 0.18 μm CMOS mixed signal
Implementation	Single chip
Circuit Size	0.729 mm^2 (excluding antenna)
Application	Short distance (on chip wireless interconnection for future ULSI)

3. Summary and Future Plan

A single chip UWB transmitter circuit based on time hopping spread spectrum technique for wireless interconnect system has been developed based on CMOS technology to generate the monocycle pulse with a target monocycle pulse center frequency of 5 GHz. The chip is now under evaluation process.

4. References:

[1] A B M H Rashid, S Watanabe and T. Kikkawa, IEEE Electron device letter, Vol.23, No.12, Dec 2002, pp. 731-733.
[2] Moe Z Win and Robert A. Scholtz, IEEE Transactions on communications, vol 48, No. 4, April 2000, pp. 679-691.
[3] Jeongwoo Han and Cam Nguyen, IEEE microwave, wireless and components Letters, vol. 12, No. 6, June 2002, pp. 206-208.

5. Achievement

Proceeding Papers

1. P. K. Saha . Nobuo Sasaki, and Takamaro Kikkawa, " A Single Chip UWB Transmitter based on 0.18 μm CMOS Technology for Wireless interconnection," Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing, Jan. 30, 2004, pp. 28-29.
2. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa, " A CMOS UWB Transmitter for Intra/Inter-chip Wireless Communication" paper accepted, IEEE 2004 International Symposium on Spread Spectrum Techniques and Application (ISSSTA 2004), Australia, Aug. 30-Sep 2, 2004.
3. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa**, "** A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter-chip Wireless Interconnection", paper submitted, SSDM 2004, Tokyo, Japan.

Oral presentation

1. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa ,"UWB Transmitter Circuit design for on chip wireless interconnection: Theoretical aspects and simulation," Presented at Mini-symposium and RF technical workshop , 7 October 2003, Osaka University, Japan.

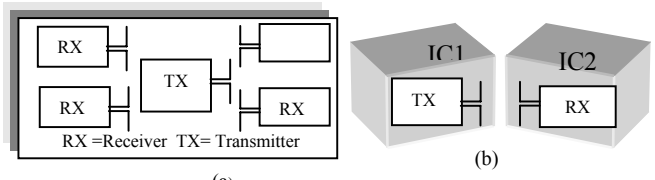


Fig. 1 Wireless interconnect (a) Intrachip ; (b) Interchip

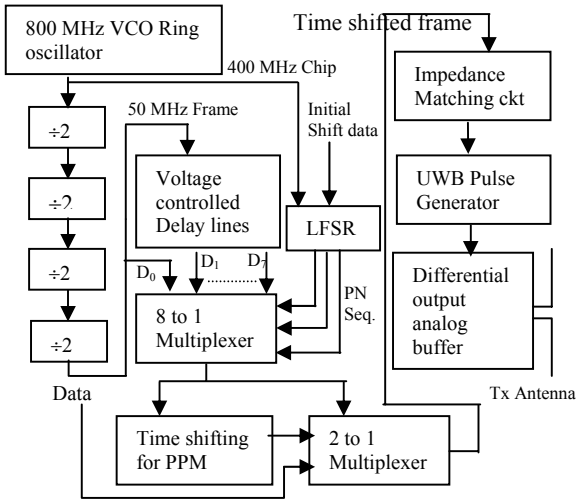
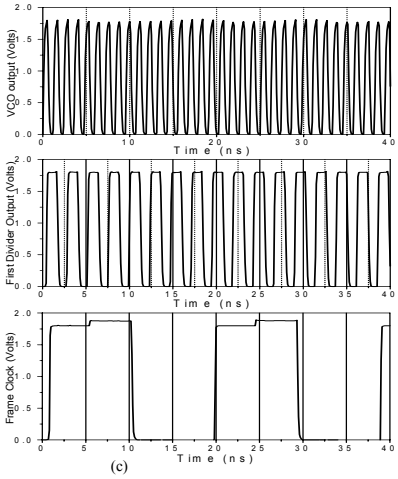


Fig.2 Transmitter circuit Schematic.



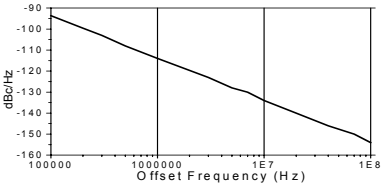


Fig.4 VCO Phase noise.

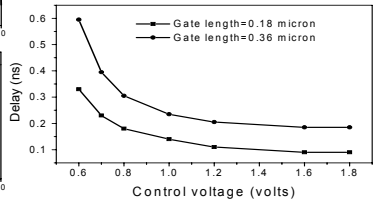


Fig. 5 Voltage controlled delay response.

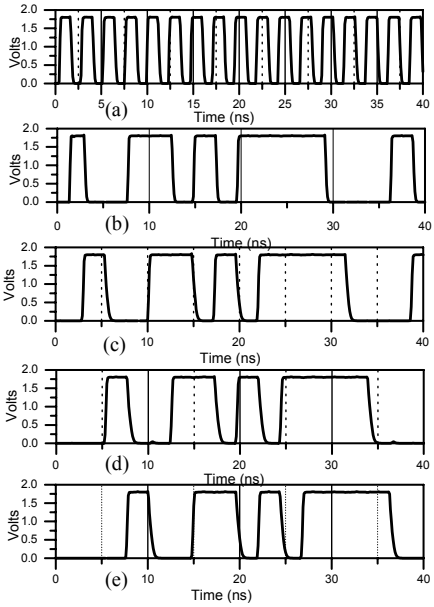


Fig.6 (a) 400 MHz Chip; (b) first tap; (c) second tap ; (d) third tap and (e) last tap outputs of LFSR.

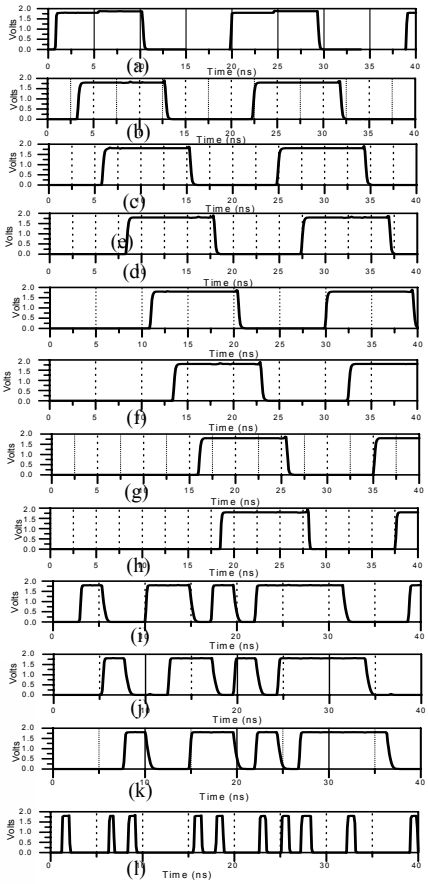


Fig. 7 (a) 50 MHz frame ; (b)-(h) shifted frame (2.5ns-17.5ns); (i)-(k) hopping bits ; (l) 8 to1 multiplexer output according to hopping bits

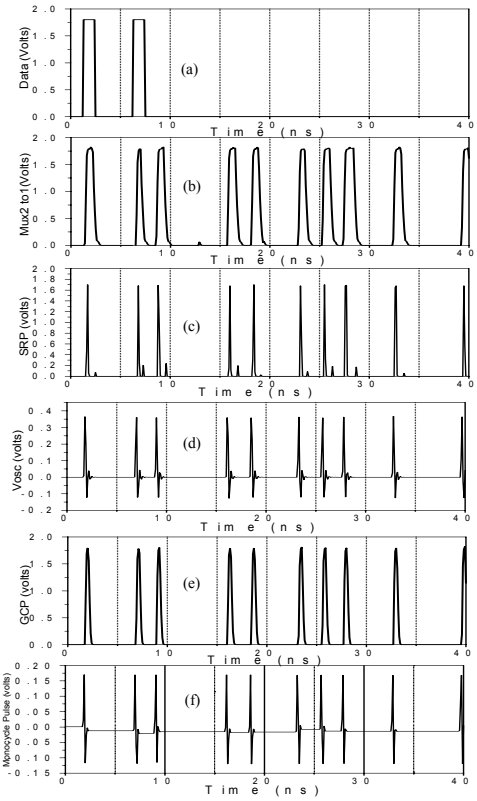


Fig. 9 (a) RZ Data (b) THS ; (c) SRP ; (d) damped sinusoidal signal (Vosc); (e) GCP and (f) Monocycle pulse.

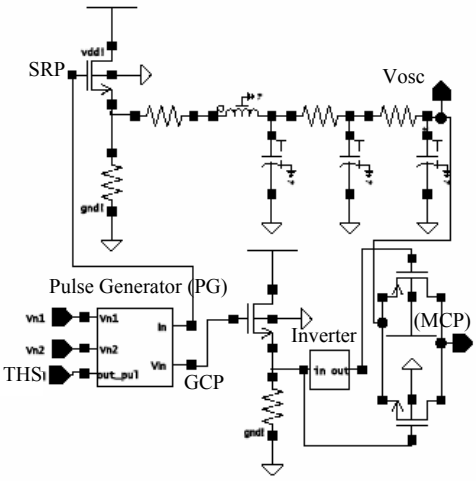


Fig. 8 CMOS monocycle pulse generator circuit

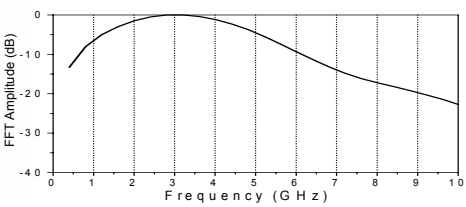


Fig. 10 FFT of Monocycle pulse.

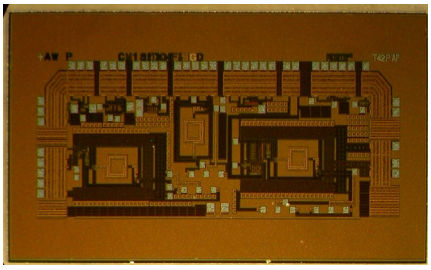


Fig. 11 Die photograph of Transmitter.