Intra/Inter-Chip Wireless Interconnect System for ULSI (3)
－A CMOS Ultra Wideband Receiver－

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1. Research Targets

A wireless interconnect technology has been developed and it can provide a better answer for RC delay problem in future ULSI [1,2]. Recently, UWB (Ultra Wide Band) technology has been developed for indoor communications [3,4]. However, single chip CMOS UWB integrated circuits have not been developed yet. In this study, a prototype of single-chip UWB receiver integrated with dipole antennas is developed based on 0.18μm CMOS technology. The target operation frequency is 4-5 GHz.

2. Research Results

Figures 1 and 2 show a photograph and block diagram of a prototype of single-chip UWB receiver based on 0.18-μm CMOS technology, respectively. It is composed of 200Ω (1GHz) - 107Ω (10GHz) impedance matching circuit (IMC), 15.6dB two stage differential low noise amplifiers (LNA), pulse correlation circuit (mixer + integrator) and analog/digital converter (sample/hold + comparator). An input signal $V_{in}(t)$ is a periodic Gaussian monocycle pulse train (center frequency f_c= 5GHz, pulse width=0.2ns and 3dB bandwidth = 5.8GHz). Fourier expansion and Fourier coefficient F_n of such signals are given as follows,

$$\mathrm{V_{in}}(t) = -\frac{\sqrt{2\pi}}{T}\sum_{n=1}^{+\infty} F_n \sin(2\pi f_n t) \tag{1}$$

$$F_n = \frac{A}{2}\left(\frac{f_n}{f_c}\right) e^{-\frac{1}{2}\left(\frac{f_n}{f_c}\right)^2}\left[erf\left\{\frac{i}{\sqrt{2}}\left(\frac{f_n}{f_c}\right)+\sqrt{2}\pi f_c T\right\} - erf\left\{\frac{i}{\sqrt{2}}\left(\frac{f_n}{f_c}\right)-\sqrt{2}\pi f_c T\right\}\right] \tag{2}$$

where $2T$: cycle time, $f_n = n/2T$: frequency and f_c : center frequency, respectively. The modulation method is pulse position modulation (PPM), i.e., in the case of data d=1, the arrival of the pulse is delayed for a short period of time δ. Pulse correlation circuit performs a demodulation as follows

$$\int_{-T0/2}^{T0/2} V_{in}(t)\cdot V_{template}(t)dt \begin{cases} >0 \ for & d=1 \\ <0 \ for & d=0 \end{cases} \tag{3}$$

where T_0 is a integration time (> pulse width), and $V_{template}$ is called as a template signal, which is defined as a differentiation of input signal. HSPICE simulation data are shown in Figs.3 and 4.

The schematic diagram of differential LNA is shown in Fig. 5. The output signal of the circuit is calculated as follows

$$V_{out}(t) \approx -\frac{A\sqrt{2\pi}}{\mathrm{T}}\sum_{n=1}^{\infty} e^{-\frac{1}{2}\left(\frac{f_n}{f_c}\right)^2}\left(\frac{f_n}{f_c}\right)|A_v(f_n)|\sin(2\pi f_n t+\theta(f_n)) \tag{4}$$

where $|A_v(f_n)|$: transfer function and $\theta(f_n)$: phase shift. Frequency responses of the amplification stage show a monotonous roll-off of the gain in the frequency range of 1-10GHz as shown in Fig. 6. It gives rise to the distortion and phase shift of Gaussian monocycle pulse so that it leads to an increase of bit error rate in pulse position modulation (PPM). Thus, the group-delay characteristics of Gaussian monocycle pulse are studied in detail. Small signal analysis shows almost the same frequency response as HSPICE as shown in Fig. 6. Figure 7 shows the output signal of LNA. It is found that pulse width becomes longer after the LNA because its frequency response rolls off monotonically and higher frequency components of monocycle pulse are cut off. Figure 8 shows that the center frequency of the LNA frequency spectrum shifts from 5GHz to 4GHz, and corresponding pulse width is 0.25ns. It indicates that the template signal should be modified by the LNA roll-off characteristics to reduce bit error rate.

3. Summary and Future Plan

A prototype of single-chip UWB receiver integrated with dipole antennas was designed based on 0.18μm CMOS technology. Small signal analyses and HSPICE simulation of CMOS UWB receiver circuit using Gaussian monocycle pulse were conducted. High frequency roll-off due to parasitics of LNA resulted in the increase of monocycle pulse width. Accordingly, the template signal should be shifted to reduce bit error rate. The results of theoretical analysis were submitted to SSDM 2004.

4. References

[1] B. A. Floyd and Kenneth K. O., IEEE J. of Solid State Circuits, 37 (2002) pp543-592.
[2] A. B. M. H. Rashid, S. Watanabe and T. Kikkawa, Jpn. J. Appl. Phys. Part 1, 4B, 42(2003) 2204.
[3] M. Z. Win and R. Scholtz, IEEE Trans. on Comm. 48 (2000) pp679-691.
[4] S. Yoshizumi. T. Terada, J. Furukawa, Y. Sanada and T. Kuroda, IEEE Ultra Wideband Systems and Technologies (UWBST' 03), pp.438-442.

5. Achievement

Proceedings

1. N. Sasaki, P.K. Saha and T. Kikkawa, “Small Signal Analysis of Gaussian Monocycle Pulse for CMOS UWB Receiver Circuits”, submitted to International Solid-State Devices and Materials SSDM2004, Tokyo, Japan.
2. Pran Kanai Saha, N. Sasaki and T. Kikkawa, “A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter-chip Wireless Interconnection”, submitted to SSDM 2004, Tokyo, Japan.
3. N. Sasaki, P.K. Saha and T. Kikkawa, “A single chip UWB receiver based on 0.18 um CMOS technology for wireless interconnection”, Proceedings of 2nd Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing, pp98-103.

Oral presentations

1. N. Sasaki, P.K. Saha and T. Kikkawa, " UWB receiver circuit design ", The 1st workshop of analog RF circuits, Osaka University., 2003.10.7.
2. N. Sasaki, P.K. Saha and T. Kikkawa, "A single chip UWB receiver circuit design and simulation", The 51st Spring meeting of JSAP, Tokyo University of Technology, Abstract 28aZH10, p. 958, 2004.

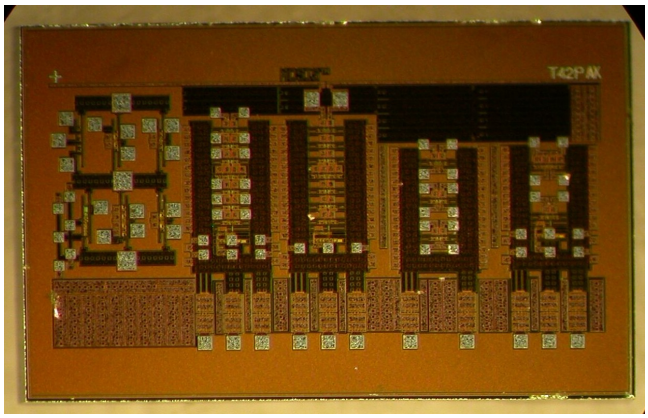

Fig.1. The Photograph of UWB receiver (TSMC CMOS 0.18-μm mixed signal, V_{dd}=1.8V).

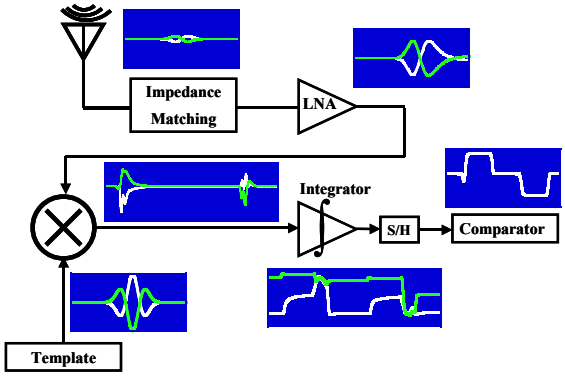

Fig.2. Functional block diagram of UWB receiver.

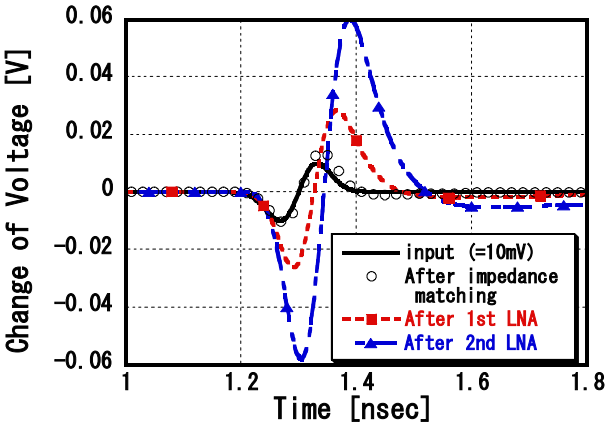

Fig.3 Output of UWB receiver (HSPICE simulation).

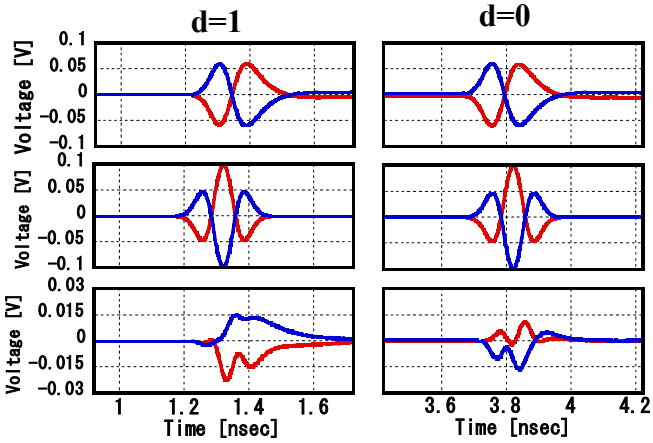

Fig.4. Input , template and output signals of Mixer in the case of d=1 (left) and d=0 (right).

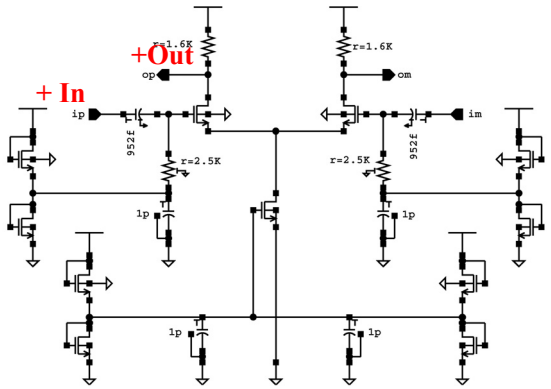

Fig.5. Schematic diagram of differential low noise amplifier.

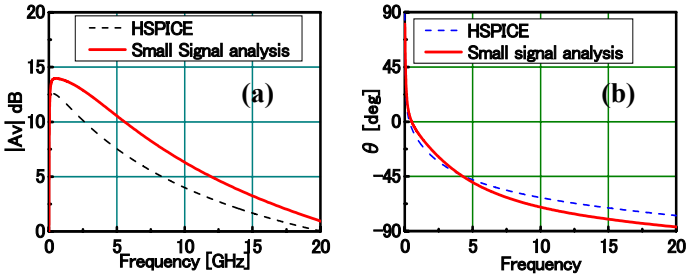

Fig.6. Frequency response of LNA. (a) Voltage gain (b) Phase shift.

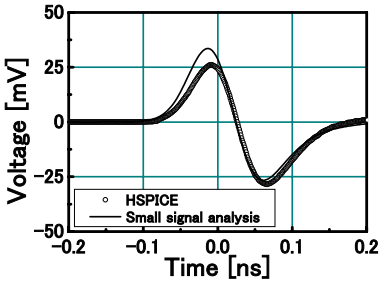

Fig.7. Output signal of LNA.

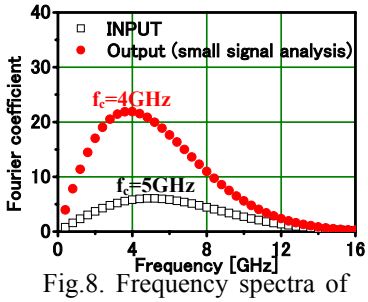

Fig.8. Frequency spectra of Input and output signals of LNA.