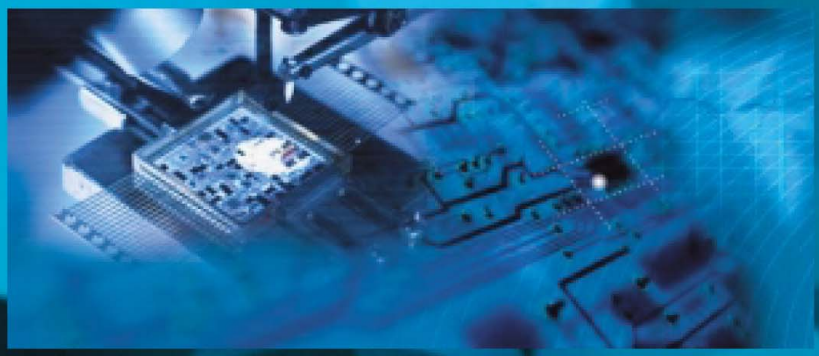

Hiroshima University

21st Century COE Program

Nanoelectronics for Tera-bit Information Processing

Progress Report
June 2004 (Volume 1)

Hiroshima University 21st Century COE Program
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Contents

Foreword

Taizo Muta

Hiroshima University President

Hiroshima University is a university that promotes freedom and peace and is open to the community. Under its five guiding principles, the University is aiming to become a top-level comprehensive university that is distinguished throughout the world and has established a long-term vision in order to realize this goal.

Hiroshima University is an integrated research university with ten faculties, ten graduate schools and one research institute, along with many education and research facilities. As a leading university, it has an excellent record of education and research achievements.

Along with perfecting the fundamental academic fields in which the University has already obtained an excellent international standing, the University contributes to the creation of an intellectual civilization by intensively promoting the importance of pioneer research and aims to establish a world position in a variety of fields of academic research. For this reason, we have established four special research centers including the Research Center for Nanodevices and Systems and are examining ways to promote centers that have been selected as a 21st Century Center of Excellence (COE) and would be research groups.

Based on the University's string of excellent educational achievements and traditions, we shape educational content to meet the needs of society and develop new educational methods in order to send out to society, students who have a wide field of vision, highly specialized abilities and are rich in human qualities. Universities, along with showing a particular image to society, must progress with society and meet society's various needs. Contributions to society are viewed as an important function of this University. Through its various activities, the University promotes co-operation with regional society and international enterprises. The University is located in the peace city of Hiroshima and so it is especially important that we take the lead in providing the means to, and in sending out, a message of peace. Within the University, we aim to create an invigorating, co-operative campus that allows individuals to display their strengths.

Universities need to progress in making their own reforms in order to establish the society demanded by the 21st century. Hiroshima University has already made various reforms in anticipation of the times, but it must endeavor to sternly judge and evaluate itself and make continual reforms in the future too.

Message from COE Leader

The Research Center for Nanodevices and Systems (RCNS) has been selected as the Center of Excellence (COE) on "Nanoelectronics for Tera-Bit Information Processing" based on the 21st COE program, in 2002. The scientific staff of RCNS and the cooperating member of the Graduate School of Advanced sciences of Matter intend to form the COE for innovative research and education on information electronics by extending their world-class research position.

Through the technical fusion of the three research fields: (1) Semiconductor devices and process, (2) Nano-device modeling and (3) Integrated circuit design and Architecture, a worldwide leading COE for information-electronics research and education has been constructed. A wide band wireless interconnection technique and 10GHz RF circuits design based on the MOS model (HiSIM), 3-dimensional system-integration using ultimately small devices have been developed as an innovative technical vision for realizing highly intelligent moving object recognition and robot control systems .

A further important goal is to bring-up a large number of young researchers, capable of doing self-defined and independent high-quality research, through the participation in leading-edge research programs of the COE. For this purpose, new department of "Semiconductor Electronics and Integration Sciences" will be established in April 2004, in the Graduate school of Advanced Sciences of Matter. In the department, the staff of RCNS will practice distinguishing education programmed by the COE, and enlarge its duties in the graduate education program of Hiroshima University.

This report has the purpose to offer information about the research activities and achievements of the COE in 2002 and 2003, to those engaged in the fields of advanced integration sciences including circuit design and system architecture, semiconductor devices and processing. We hope, the report will further enhance the mutual exchange of ideas and contribute to the future progress of the research on advanced integrated devices and systems.

June 1, 2004

Atsushi Iwata
COE Leader
Research Center for Nanodevices and Systems
Hiroshima University

The outlines of COE formation and Research Achievements

1. Principle behind the COE

For more than twenty years, we have focused our attention on mainstream progress in silicon integrated circuit technology along with the world's top-level research and developments in VLSI technology, which are seen to be the keys to the realization of an advanced information society. Building upon this solid foundation, the objectives of the COE are the development of fundamental technologies and new academic fields for a new integration system based on the design principles of both physical and information processing theory. We also plan to establish a novel, highly innovative system with advanced recognition/learning functions utilizing the integration of silicon Nano-devices, circuits, and architectures.

From an academic perspective, we aim to construct new fields of research by integrating circuit design and device processing technologies, currently disparate disciplines, using device modeling techniques as cross-linkers. It is important to educate many specialists with the critical abilities necessary to both research and develop a wide range of information and electronics-based academic fields. Such researchers will become future leaders in these new fields, which will produce a wide range of technological benefits from individual devices to entire systems. Therefore, we aim to foster and support promising individuals with the ability to approach technological challenges with a deep understanding and practical capability to facilitate the promotion of advanced independent research.

2. COE Objectives

2.1 Research Objectives

-Unification of silicon-based system, circuit, device-modeling and device-fabrication research.

-Solution of the persistent 3-diminsional-integration problems by a wireless integration methodology.

-Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures.

2.2 Education Objectives

-Increase the number of doctoral students (10 students per year) and improve their quality.

3. COE member and Research subjects

3.1 Previous major achievements of the COE group

Over the past 30 years, our group has achieved top-level results in the following three fields in the area of research and education of silicon integrated circuits.

First, in the field of "Circuit and System Architecture," Professor Iwata proposed the analog-digital fusion circuit architecture utilizing pulse modulation signals. He has developed a picture function associative processor, and demonstrated its technical functionality and high level of performance.

Professor Mattaushe has studied functional memory, devised an analog full-parallel comparison circuit, and developed analog-digital merged associative memory. Moreover, he has developed a multi-port memory circuit for parallel processing systems and successfully developed a test chip.

Professor Yokoyama proposed a photoelectron-fusion integration system with optical wiring. Students of the Research Center for Nano-devices and Systems assembled an image recognition test chip and demonstrated its basic operation.

Thus, our COE has top-level researchers in the fields of analog circuits, memory, digital circuits,

and optical devices.

In the second field, that of "Device Modeling," Professor Miura devised the MOS-transistor model HiSIM based on drift and diffusion physics. The HiSIM model has better accuracy than the BSIM model developed at UC Berkeley, which is the current global standard model, although the parameter counts of HiSIM are 1/5 or less. In addition, HiSIM has outstanding simulation function when advancing device segmentations, which can be used to estimate the high-frequency characteristics of the device without conducting any experiments. In January 2002, this model was released as free software and has been incorporated as a standard model into the simulators produced by almost all CAD vendors. We aim to replace BSIM and become the *de facto* standard in the next generation of CAD products.

In the third field, "Nano-device processors," Professors Miyazaki and Sunami have successfully developed an experimental small-MOS transistor, and evaluated its properties, including its reliability. They have built and evaluated a detailed experimental device with a gate length of 30 nm and gate oxide thickness of 1.2 nm. Their research is competitive with the technology produced by the world's top companies, a claim that other universities throughout the world cannot match.

Professor Kikkawa has studied the multilayer-interconnection system of integrated circuits and has developed technology to utilize materials with low dielectric constants. Moreover, this technology has been developed into wiring technology using electromagnetic waves or light.

3.2 Research fields and core members

Field I Circuits and system architecture

I-1. Radio frequency and analog circuits for wireless interconnections and signal processing
by Prof. A. Iwata & Assoc. Assoc. Prof. M. Sasaki

I-2. Associative-memory-based systems with recognition and learning capability
for image feature detection and recognition by Prof. H. J. Mattausch & Assoc. Prof. T. Koide

I-3. Processing system architecture with highly cognitive level by Prof. A. Iwata

Field II. Device Modeling

II-1 MOS device model for RF frequency range and SOI structure
by Prof. M. Miura-Mattausch & Res. Assoc. Dr. H. Ueno

II-2. Device model with RF and light response
by Prof. M. Miura-Mattausch & Res. Assoc. Dr. H. Ueno

Field III Nanodevices and Processes

III-1. Fundamental miniaturization techniques for Si-MOS transistors
by Assoc. Prof. K. Shibahara, and Prof. Miyazaki

III-2. Three-dimensional ultra-small SOI-MOS transistors
by Prof. H. Sunami & Prof. M. Miura-Mattausch

III-3. Functional nano-devices with multilayer dots:
by Prof. S. Miyazaki, Assoc. Prof. Higashi & Res. Assoc. Mr. H. Murakami

III-4. Integration technologies of wireless interconnect for chip-to-chip
by Prof. T. Kikkawa & Assoc. Prof. M. Sasaki)

III-5. Integration technologies of optical interconnection
by Prof. S. Yokoyama & Assoc. Prof. A. Nakajima

4. Formation of the COE

4.1 Basic Plan

The objectives are investigated in parallel in three independent fields at the beginning, and merged a year after a year. Following are overview of our development plan:

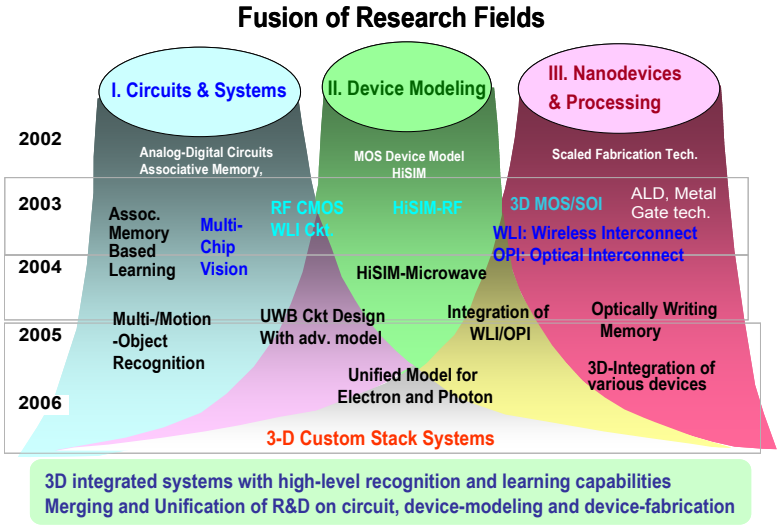
2002- Extension of the worldwide top-level basic-technology position. Accelerated fusion of the research activities of the program's three research pillars. Young program-member research proposals: Start of 2 cooperative projects on devices and modeling.

2003- Expansion of the cooperative research between the research fields. Promotion of research on wireless interconnects between chips. Young program-member research proposals: 2 additional cooperative projects between the device and circuit/system fields.

2004-Upgrading of the technology level in the light-interconnect and functional-memory fields to introduce them as new elementary technologies for integrated circuits.

2005- Highly efficient method for integrated device and circuit design. Basic 3-dimensional design technology for integrated circuit (vertical device) and electrical/optical integration.

2006- Establishment of the research-field organization and future-plan.



4.2 Progress of the COE

The research cooperation has started aiming at the fusion of the research fields. The researches for combining (1) high frequency MOS device modeling and RF circuit design, and (2) radio wave transmission system and integrated antenna structure have progressed. The researches on architecture utilizing wireless interconnection for associative memory based image processing, and bio-inspired visual processing have started. Furthermore, the research efforts on new devices and fabrication technologies for implementing 3 dimensional integration systems have also progressed.

For publicity of the concept of our COE, the 1st International Workshop on Nano-electronics was held in March, 2003. the 2nd International workshop was held in January, 2004, focusing on the device modeling.

In 2003, we have been awarded a large Grant in Aid for basic research (S) on "3 dimensional integration architecture using radio communication between chips for high recognition processing system", and many other grants. COE members have also accomplished cooperative research projects cooperation with public laboratories and companies.

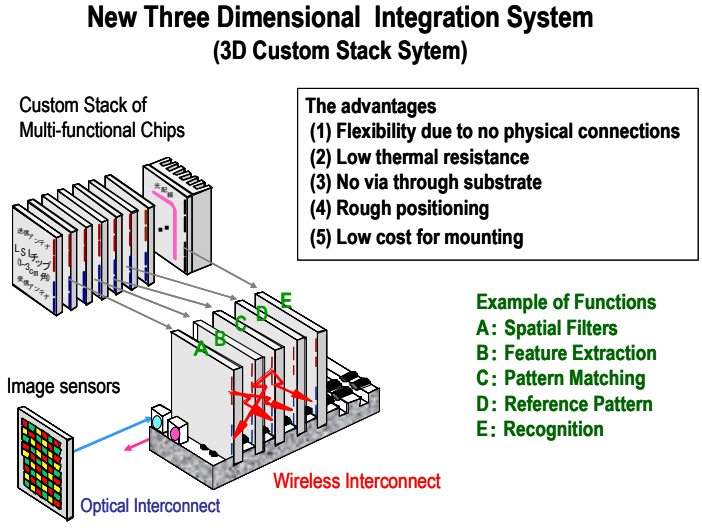
4.3 Three research fields are integrated to create new interdisciplinary fields.

HiSIM device modeling is situated between these three-research areas. At present, we are integrating these three research pillars to create new academic and technical fields of study.
The HiSIM model has been extended and is now applicable to the microwave frequency domain. Ongoing research at the COE will result in further extensions to light and electronic fusion device models. Our research fields will be united with this HiSIM device model as a major focal point. Currently, we are engaged in research into super high-frequency circuit design technologies utilizing the microwave HiSIM model and broadband wireless interconnections with low power dissipation. We are also studying the architecture of the vision system and algorithms for moving object recognition to establish a system with advanced recognition/learning capabilities.

In device processing by SOI, we have developed three-dimensional MOS devices, integrated antennas, integrated optical components, and optical sensor devices using quantum dot research. Furthermore, the establishment of the base technologies of wireless and optical integration will allow us to address the problem of reconfigurable system integration with wireless interconnection technology.

Currently, we are engaged in attempts to realize a three-dimensional integration system capable of interconnection between stacked multiple chips using electromagnetic waves. In this system, light interconnection will be used for long-distance connections between sensors.
This technology realizes (1) high level learning and recognition capabilities utilizing multi-chips, (2) image sensing capability of vision close to that of the human eye, and (3) flexible system configuration due to wireless interconnections.

As an example of such a system, the diagram shows the planned image recognition system consisting of multiple chips with various functions, including a spatial filter, feature extraction, and matching. New academic areas of interest include electromagnetic wave transmission theory in semiconductors, integration design techniques of integration antennas and circuits, and techniques for the integration of Ultra Wide Band communication technology.



4.4 New department in the graduate school of Advanced Sciences of Matters

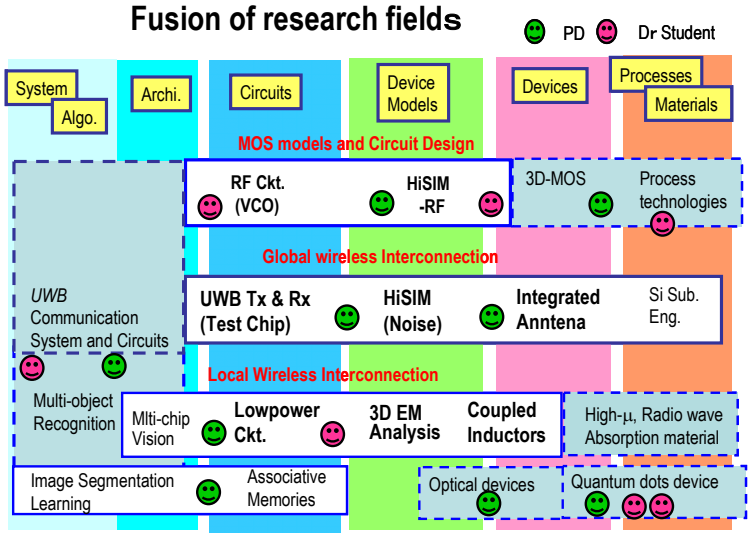
An important aim of the COE is to bring-up a large number of young researchers, capable of doing self-defined and independent high-quality research, through the participation in leading-edge research programs of the COE. For this purpose, we established the new department of "**Semiconductor Electronics and Integration Sciences**", in April 2004, in the Graduate School of Advanced Sciences of Matter, Hiroshima University. We have already developed the new program for high-level education through advanced research and practical training.

By extending graduate school education linked directly to advanced research, we intend to produce highly capable doctorate-level researchers who will make great contributions as future leaders in the fields of science and technology. Utilizing device fabrication equipment, such as the Super Clean Room and LSI Circuit Tester, we will foster the development of talented individuals with proven ability to perform valuable research in a wide range of fields, from devices to systems. A training program has been established to provide opportunities for high-level doctorate students to master not only advanced technology but also to develop a global point of view. Moreover, we have designed the new educational training program to further the development of logical thinking and planning abilities.

4.5 Establishment of research system for fusing research fields

The COE has advertised for postdoctoral COE researchers and employed 9 persons (3 foreigners) as additional core members of the COE in 2003. We also employ 6 doctoral course students as COE researchers.

We have set the research theme of each COE researcher on the boundary of existing research field in order to fuse the three research fields. We encourage co-operative research and free discussion between COE researchers. Our plan is to increase the COE researchers to 15 for postdoctoral researchers and to 16 for doctoral students in 2004.



5. Outline of research achievements

5.1 MOSFET Model: *HiSIM* for high frequency operation and the SOI structure has been developed. Its concept is to describe devices in accordance with basic physical principles. An 0.18um-CMOS testchip with RF-MOS devices and a voltage controlled oscillator (VCO) was designed and measured for evaluating the HiSIM model in the GHz frequency region.

5.2 Wireless Interconnection: Radio wave propagation through a silicon substrate was measured using integrated dipole antennas. A 20GHz radio wave propagates with low loss through a highly resistive Si substrate made by the proton implantation. This technology realizes the new 3 dimensional integration utilizing chip-to-chip wireless global interconnects for system clocks and buses for bi-directional data transfer and broadcasting.
Another complementary solution for wireless interconnects using resonant coupling of a spiral inductor pair was proposed. It realizes low power multi-giga bit/s wireless interconnects with highly parallel multi-channel communication suitable to transfer 2D data such as visions and neural information.

5.3 Associative memory based learning algorithm and integration of learning capability have been developed. It is applicable after image segmentation for various kinds of objects and recognition.

5.4 Multi-chip vision system architecture is proposed using PWM signals and wireless interconnection. Image recognition based on the Principal Component Analysis was also studied, and its applicability to multi-object recognition systems has been confirmed.

5.5 New MOS devices using new structures and materials, three dimensional MOS devices on SOI as well as, single metal-gate CMOS devices using the metal work function control are under investigation.

5.6 Optoelectronic merged technology:
The optical waveguides using EO materials were proposed for implementing an optical switch using resonance.

5.7 Functional nano-devices with multilayer dots
Floating gate devices with multi-layer quantum dot structure have been successively fabricated, and single electron charging behavior has been studied. Its application to a direct-optical-writing memory device is also proposed.

6. Future Plan

We have proposed the new concepts of chip-to-chip wireless interconnections, information processing architecture and new device technologies from the fused research fields. We will establish innovative basic technologies based on the concepts by simulation with theoretical models and experimental research by design and fabrication of proto-type systems. Through the advanced research, we will educate many doctoral researchers with the critical abilities necessary to both research and develop a wide range of information and electronics-based academic fields.

Members of the 21st Century COE Program
Nanoelectronics for Tera-bit Information Processing（14 core members）

COE Leader

Atsushi Iwata（58）

Professor

Department of Semiconductor Electronics and Integration Science,

Graduate School of Advanced Sciences of Matter;

Director of Research Center for Nanodevices and Systems

Research Field: System architecture and circuit design

Mamoru Sasaki（41）

Associate Professor

Department of Semiconductor Electronics and Integration Science,

Graduate School of Advanced Sciences of Matter

Research Field: Wireless interconnect scheme for 3-dimensional stack systems

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Mattausch Hans Jürgen（51）

Professor

Research Center for Nanodevices and Systems;

Department of Semiconductor Electronics and Integration Science,

Graduate School of Advanced Sciences of Matter

Research Field: Associative-memory-based systems with recognition and learning capability: Research on the required functional memories

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Tetsushi Koide（36）

Associate Professor

Research Center for Nanodevices and Systems;

Department of Semiconductor Electronics and Integration Science,

Graduate School of Advanced Sciences of Matter

Research Field: Image processing front end for associative memory-based systems with recognition and learning capability

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Michiko Miura-Mattausch（54）

Professor

Department of Semiconductor Electronics and Integration Science,

Graduate School of Advanced Sciences of Matter

Research Field: Modeling, linking process/device and circuit

Hiroaki Ueno（31）（～2004.3.31）
Research Associate
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Modeling of 1/*f* noise with HiSIM for 100 nm CMOS technology

Kentaro Shibahara（44）
Associate Professor
Research Center for Nanodevices and Systems;
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Fundamental device scaling techniques

Hideo Sunami（60）
Professor
Research Center for Nanodevices and Systems;
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Research of 3D SOI transistors

Seiichi Miyazaki（45）
Professor
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Development of novel functional Si-based devices using self-assembled nanostructures for multivalued memory operation, and ultimate photo-sensing

Seiichiro Higashi（37）
Associate Professor
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Si quantum dot formation process technology and optically coupled MOS devices

Hideki Murakami（31）
Research Associate
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Low resistive gate electrode/high-k gate dielectrics stacked structure and its device application

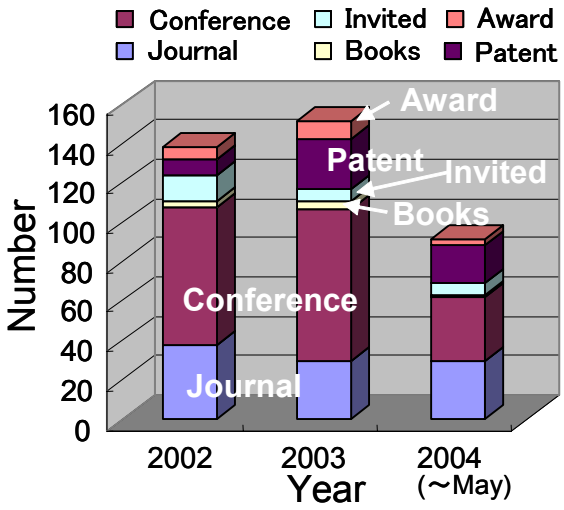
Takamaro Kikkawa（52）
Professor
Research Center for Nanodevices and Systems;
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Wireless interconnects for high-speed data transmission

Shin Yokoyama（50）
Professor
Research Center for Nanodevices and Systems;
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: Development of optically interconnected LSI

Anri Nakajima（43）
Associate Professor
Research Center for Nanodevices and Systems;
Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter
Research Field: High-k gate dielectrics for scaled MOS transistors

3. Achievements, Published Papers, Patents, and Awards

Achievements of this COE Program Group



Year	Journal	Conf. Paper	Book	Invited Presentation	Patent	Award
2002	38	70	3	13	8	6
2003	30	77	4	6	25	10
2004 (~May)	30	32	1	6	20	3

The present achievements (journal papers, international conference papers, books, invited presentations, patents, and awards) of this 21st century COE program group are summarized in the above histogram and table. In 2003 we had an increase in the total number, summed over all categories, but a mixed detailed development. On one hand the number of journal papers and invited presentations reduced by about 20% and 50%, respectively. On the other hand we had an increase of 10% for international conference papers and very substantial improvements in the numbers of patents by about 210% as well as awards by 70%. In 2004 a strong recovery, in particular in the number of journal papers and invited presentations is observed, both of which are after only 5 month already at the same level as in 2003. We therefore expect the journal papers and invited presentations to approximately double in comparison to 2003 during this year. Also the number of patent applications, which is already near to the value of the previous year, is expected to increase substantially. The number of international conference papers is expected to reach the same level as in 2003. In summary we can say that the achievement level of our group is steadily increasing, reflecting the continuous progress in the formation of our COE program on “Nanoelectronics for Tera-bit Information Processing”.

List of Publications, Patents, and Awards

I. Circuits and Systems

COE Subject

I-1. Journal Papers

[1] H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata, "Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques," IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, 2002.

[2] T. Morie and T. Matsuura and M. Nagata and A. Iwata, "A Multi-Nano-Dot Circuit and Structure Using Thermal-Noise Assisted Tunneling for Stochastic Associative Processing," J. Nanosci. Nanotech., Vol. 2, No. 3, pp. 343-349, June, 2002

[3] K. Katayama, M. Nagata, T. Morie and A. Iwata, An Hadamard, "Transform Chip Using the PWM Circuit Technique and Its Application to Image Processing," IEICE Trans. Electron., Vol. E85-C, NO.8, pp. 1596-1603, Aug. 2002.

[4] H.J. Mattausch, T. Gyohten, Y. Soda and T. Koide, "Compact Associative-Memory Architecture with Fully-Parallel Search Capability for the Minimum Hamming Distance," IEEE Journal of Solid-State Circuits, 37, 218-227 (2002).

[5] K. Katayama, and A. Iwata, "A High-Resolution CMOS Image Sensor with Hadamard Transform Function," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences E86-ANO.2, pp. 396-403、Aug.2003.

[6] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, "A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models," IEEE Trans. Nanotechnology, Vol. 2, No. 3, pp. 158-164, Sept. 2003

[7] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels," IEICE Trans. Fundamentals., vol.E87-A, pp.376-383, Feb. 2004.

[8] T. Yoshida, M. Akagi, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Wireless Neural-Sensing LSI," IEICE Trans. Electronics, vol.E87-C, pp.996-1002, June 2004.

[9] T. Morie, T. Nakano, J. Umezawa, and A. Iwata, "Gabor-Type Filtering Using Transient States of Cellular Neural Networks," Intelligent Automation and Soft Computing, in press, 2004.

[10] K. Korekado, T. Morie, O. Nomura, H. Ando, T. Nakano, M. Matsugu, and A. Iwata, "A VLSI Convolutional Neural Network for Image Recognition Using Merged/Mixed Analog-Digital Architecture," Int. J. Fuzzy and Intelligent Systems, in press, 2004.

[11] T. Sasaki, T. Inoue, N, Omori, T. Hironaka, H.J. Mattausch, and T. Koide, "Chip Size and Performance Evaluations of Shared Cache for On-chip Multiprocessors," IEICE Trans. on Information & Systems Part 1, vol. J87-D-I, 350-363 (2004) (in Japanese).

[12] S. Fukae, T. Inoue, H.J. Mattausch, T. Koide, and T. Hironaka, “Distributed against centralized crossbar function for realizing bank-based multiport memories,” IEE Electronics Letters 40, 101-103 (2004)

[13] K. Johguchi, Z. Zhu, T. Hirakawa, T. Koide, T. Hironaka, and H.J. Mattausch, “Distributed-crossbar architecture for area-efficient combined data/instruction caches with multiple ports,” IEE Electronics Letters 40, 160-162 (2004).

[14] H. Noda, K. Inoue, M. Kuroiwa, F. Igaue, K. Yamamoto, H.J. Mattausch, T. Koide, A. Amo, A. Hachisuka, S. Soeda, F. Morishita, K. Dosaka, K. Arimoto, and T. Yoshihara, “ A Cost-Efficient High-Performance Dynamic TCAM with Pipelined Hierarchical Searching and Shift Redundancy Architecture,” IEEE Journal of Solid-State Circuits, 39, in press (2004).

[15] T. Morimoto, Y. Harada, T. Koide, and H.J. Mattausch, “Efficient Video-Picture Segmentation Algorithm for Cell-Network-Based Digital CMOS Implementation,” IEICE Trans. on Information & Systems, vol. E87-D, 500-503 (2004).

I-2. Proceedings of International Conferences

[16] M. Nagata, Y. Murasaka, Y. Nishimori, T. Morie, and A. Iwata, “Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models,” Proc. 7th Asia and South Pacific Design Automation Conf, pp. 71-76, Bangalore, Jan. 2002.

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[19] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models,” 2002 IEEE Silicon Nanoelectronics Workshop, pp.53-54, Honolulu, June 9, 2002.

[20] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “An Efficient Clustering Algorithm Using Stochastic Association Model and Its Implementation Using Nanostructures,” Advances in Neural Information Processing Systems 14, Ed. T. G. Dietterich, S. Becker and Z. Ghahramani, MIT Press, Cambridge, MA, 2002.

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4. Research Results of Each Subject
4-I. Circuits and Systems

Three Dimensional Integration Architecture for Tera-bit Information processing

Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter),
Mamoru Sasaki (Assoc. Prof., Graduate School of Advanced Sciences of Matter)
Seiji Kameda, Hiroshi Ando (COE Researchers),
Takeshi Yoshida, Mitsuru Shiozaki (Graduate School of Advanced Sciences of Matter, D3)
and Masahiro Ono (Graduate School of Advanced Sciences of Matter, D1)

1. Research Target

1.1 New paradigm for future integration systems

There are three major elements of information processing in electronics: (1) operation and judgment, (2) memory and learning, and (3) communication and data transfer. Although a great deal of progress has been made in the field of semiconductor memory, the problem of how best to utilize the huge memory capacity now available to us remains. How do we memorize people's face and objects? Although this question has yet to be resolved, it is clear that we do not simply analyze and recognize the characteristics of pictures. In addition to images, we use other elements to memorize such information. Moreover, it seems that the patterns are distributed to various parts of the brain. Although living systems use slow neural network devices, *i.e.*, the cells of the brain, which are unreliable because of sensitivity to changes in environment or noise, they achieve a sufficient level of information processing capability. This strategy has been utilized based on the results obtained by various methods using super parallel processing. This was most suitable for use of the huge number of neurons in living systems. To mimic the processes occurring in living systems, it is important to establish functions for the collection and processing of the distributed information and to make global judgments. The bottleneck is the information communication capability within and between the chips.[1]

In 21st century, promising solution for breaking Moore's law will be three dimensional integration technologies utilizing nano-devices and advanced interconnect technologies.

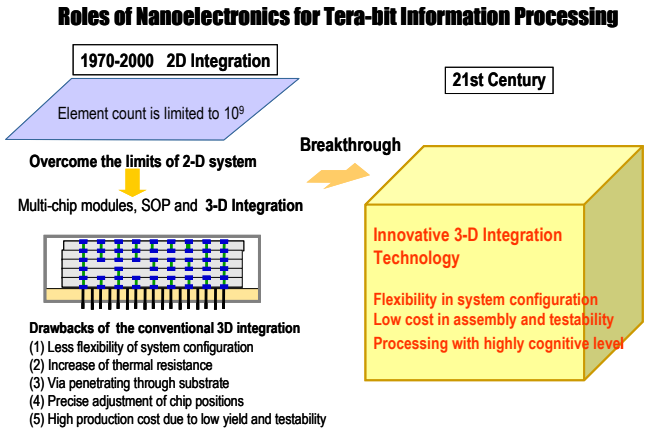

Fig.1 Roles of nanoelectronics for era-bit information processing

How to solve communication bottlenecks

In order to realize Tera-bit information processing system, we have proposed three-dimensional integration technologies utilizing wireless communications between and within the chips at the COE. This enables wiring through multiple chips and new three-dimensional integration without requiring accurate positioning. In addition, we have also attempted to develop optical communication implemented with photonic devices and quantum dots memory devices using light communication and Nano-structures. Integration technology, to integrate both radio and light, will be realized by fusion of device modeling and process technology. We will build further knowledge and strategies by realizing super-parallel processing and conduct research into processing by integration of super-efficient circuit and modeling technology with algorithms reflecting living systems. The ultimate aim of this research is the realization of a brain type processing system.

1.2 Interconnection for three dimensional integration

We intended to realize three-dimensional integration of multi-chips with different kinds of functions and technologies. To achieve the 3D integration, the most important technology is chip-to-chip interconnection. For that purpose, we introduce two types of wireless interconnections for global clock/data transfer and parallel interconnections for distributed data between adjacent chips.Optical interconnection using integrated optical components such as a wave-guide, an optical switch and an optical resonator is also introduced to high-speed and wide-band data transfer.

1.3 Tera-bit information processing system architecture

The target is highly sophisticated multi object recognition system with high speed real-time image analysis capability and flexible data matching and learning functions. Furthermore, we are aiming at a highly sophisticated brain of hyper human robot.

These systems require over 10GHz clock computing and massively parallel processing units accessing to giga byte data base. Thus tera-bit information processing has to be implemented with small size, low power and low cost. We intended to create the solution for the future electronic system with nano-devices.

2. Research Achievementss

2.1 MOSFET Model and circuit design:

HiSIM for high frequency operation and the SOI structure has been developed by Prof. Miura's Group. Its concept is to describe device operation using surface potentials in accordance with basic physical principles. It was selected as a candidate of the international standard MOS model for 60nm node, by Compact Modeling Council.

An 0.18um-CMOS test chip with RF-MOS devices and a voltage controlled oscillator (VCO) was designed and measured for evaluating the HiSIM model in the GHz frequency region. (In Corporation with Prof. Miura's Group)

Low noise and RF analog circuits for neural signal sensing system were investigated. The CMOS chopper stabilization technique was established for uV level signals amplification. Low voltage A-to-D converter and wireless transmitter have bee developed by T. Yoshida , Doctoral student. The image recognition system needs the technology of biometrics and RF interface.

Substrate noise analysis technique in GHz frequency range has also developed for reliable design..

Chip-to-chip flexible interconnection based on CDMA system was studied. CMOS transceiver chip with 2Gbps bit rate was developed by M. Shiozaki, Doctoral student.

2.2 Wireless Interconnection [2,3]

We propose wireless interconnection using integrated antenna and ultla-wide band transceiver for global data communication.

(1) Global wireless interconnection using integrated antenna and ultra-wideband communication systems

Radio wave propagation through a silicon substrate was measured using integrated dipole antennas. A 20GHz radio wave propagates with low loss through a highly resistive Si substrate made by the proton implantation. [4] This technology realizes the new 3D integration utilizing chip-to-chip wireless global interconnects for system clocks and buses for bi-directional data transfer and broadcasting. (Prof. Kikkawa's group)

(2) Local wireless Interconnection using coupled inductors

We have proposed an interconnect scheme between the stacked chips based on resonant coupling of an integrated spiral inductor pair as shown in Fig.4. A data transmitter and receiver were design A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the communication of the spiral inductor pair. The performance, 1Gb/s/channel at 9mW/channel, has been confirmed by SPICE simulation. If we use a 90 nm device technology, 2-5Gbps data transfer with 1mW per connection. By compromising chip area and power dissipation, over 100 localized data are transferred between a pair of adjacent chips. (Prof. Sasaki's Group)

2.3 Three dimensional integration using GWI and LW

We call this three dimensional integration system ***3DCSS:*** 3-dimensional custom stack system.

In the *3DCSS*, stacked chips fabricated by various device technologies are connected by the two types of wireless connections, which are GWI and LWI. GWI is used for distribution of over 10GHz system clocks, bi-directional data transfer and broadcasting of address or control data to multi-chip database. LWI provides highly parallel multi-channel communication enabling 2D data transfer such as visions and neural information.

Both use of GWI and LWI will become a promising solution for realizing intelligent tera-bit information processing.

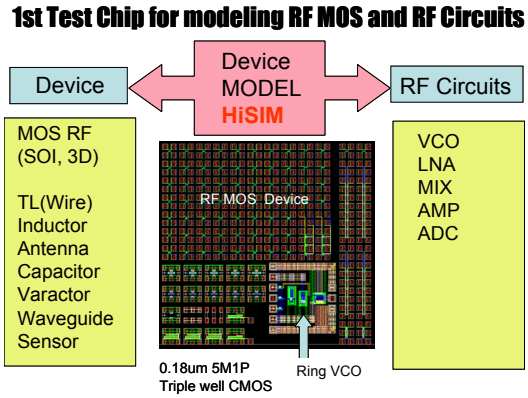

Fig.2 Test chip for modeling RF MOS and RF circuitss

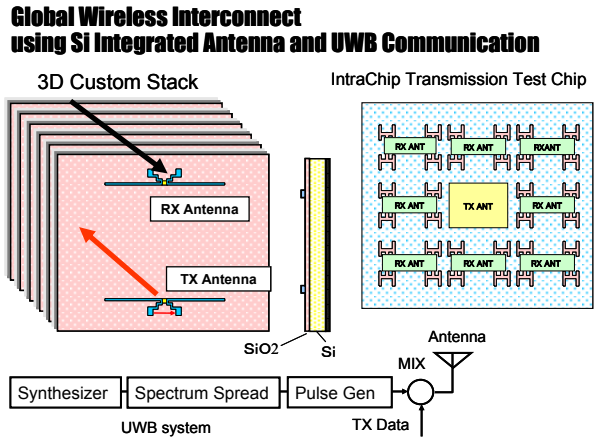

Fig.3 Wireless interconnection using integrated antennas

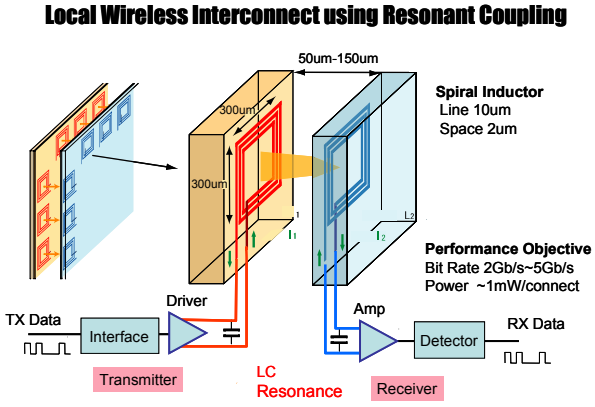

Fig.4 Wireless interconnection using resonance coupling of an inductor pairs

2.3 Algorithm and Architecture

(1)Vision system based on biological processing [5,6,7]

In the stacked multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. Due to the wireless connections, the 3DCSS overcomes a wiring complexity that is the demerit of the multi-chip system generally. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system.

Multi-chip vision system architecture using PWM signals [8] and the local wireless interconnection was proposed by Dr. S. Kameda, COE researcher. 2D image processing for image enhancement and feature detection is implemented on the multi-chip with parallel analog data transfer as shown in Fig. 5. As the first step toward fabrication of the visual processing system, a prototype visual processing chip is fabricated with a PWM-based line parallel interconnection. In the next step, we will have to verify the operation of the multi-chip system with wireless interconnection and consider visual processing algorithms.

(2) Image recognition based on the Principal Component Analysis [9,10]

A Concept of Multi-object Recognition System

For the purpose of developing a real-time/high-level recognition technology, a concept of multi-object recognition system composed of 3DCSS was proposed by Dr. H. Ando, COE researcher.

The hierarchical and massively-parallel processing of human brain are achieved using multi-functional chips and local/global wireless interconnects among LSIs based on pixel-parallel circuit architecture. 3DCSS systems composed of image sensor, image normalizer, objects detector, objects recognizer and multi-object database (DB) chips are shown in Fig. 6. We also have confirmed human face detection in a natural scene and recognition under some variations using the eigenfaces method by numerical simulation. We developed a prototype real-time human face recognition system composed of personal USB camera and software based on Win32API as shown in Fig. 5. This system can operate about 10 frame/s and recognize one or more human faces between each frame

We are scheduled to extend the eigenfaces method to multi-object recognition and realize their VLSI implementation.

(3) Robot Brain

The first target is to propose a strategy learning model for the Robot Brain of game robot. The second target is to implement the model by the custom LSI which is very compact and has low power consumptions. Strategy learning model for brain of game robot have been developed by Masahiro Ono, Doctoral student.

By extending LVQ learning algorithm, the model to create strategy of attack adaptively changing environment have been obtained. The model will be applied to architecture of brain chip for 3DCSS.

3. Conclusion and future schedule

We proposed the tera-bit information system architecture using three-dimensional integration system. (3DCSS). It features new wireless interconnection technologies which enables flexible data/clock transfer. To realize the system, we developed circuits design using MOS device model *HiSIM,* architecture of image processing, and concept of the multi-object recognition system c

We will design system architecture of 3D integrated vi-

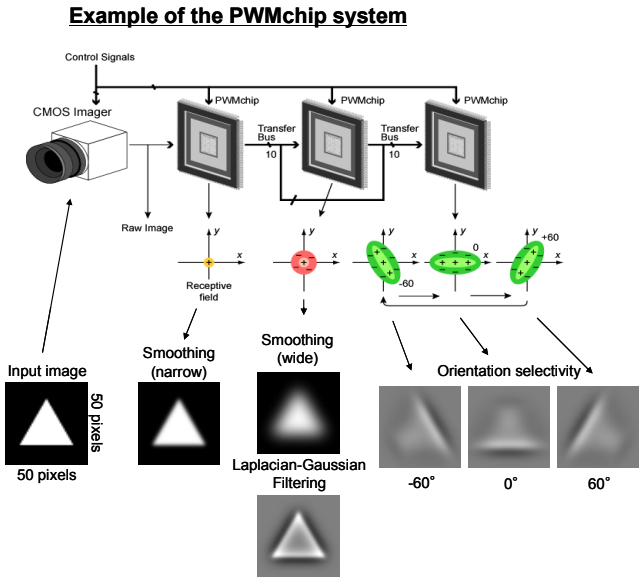

Fig.5 Example of image processing of multi-chip vision

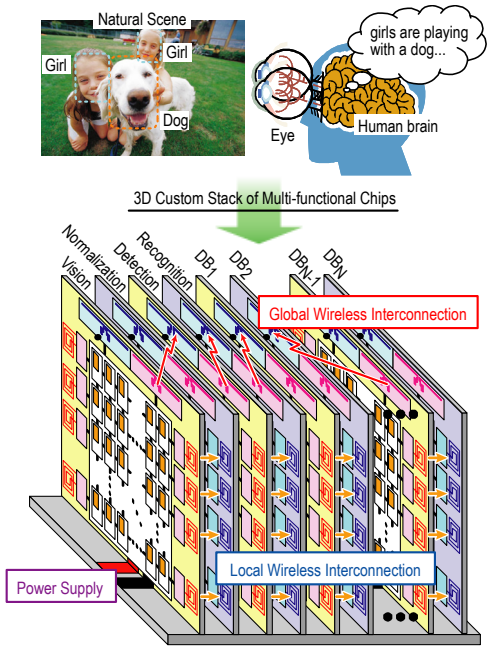

Fig.6 A concept of multi-object recognition system . using 3DCSS

sion systems and implement a proto type system.

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Patents

1. Japanese Patent 2004-10053, "Semiconductor Equipment"
2. Japanese Patent 2004-22317, 2004.01.28

A Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors

Mamoru Sasaki (Associate Prof., Graduate School of Advanced Sciences of Matter),
Daisuke Arizono (Faculty of Engineering, B4),
Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter)

1. Research Target

With the continuous downsizing of CMOS technology, various components such as processors, memories, analog circuits, RF interface, are integrated in a single chip. It is called a system LSI. However, it takes considerable time to develop system LSIs, and the integration of a wide variety of system functions on a single chip invites considerable low yield. As an alternative, attention has been drawn to the System-in-Package. Also in our COE program, development of the 3-Dimensional Custom-Stack System (3DCSS) is one of the significant themes. In conventional 3D IC fabrication technique, vias with large aspect-ratio are required, in order to connect the stacked chips [1]. A wireless interconnect utilizing capacitor coupling has been proposed and it may avoid forming the vias [2]. However, the distance between the stacked chips can not be extended so as cool the internal circuits, because of the capacitive coupling. Thus, the heat dissipation issue is still unsolved. Two types of wireless connection are studied in our COE program. One is global connection, which communicates beyond neighboring chips using microwave [3]. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. The global connection is useful for broadcasting, global control, etc. On the other hand, the local connection can handle huge data volumes due to the massive parallel structure, and it is useful for communication of 2D vision information. In this manuscript, we propose a wireless interconnect for the local connection utilizing resonant coupling between spiral inductors (see Fig.1).

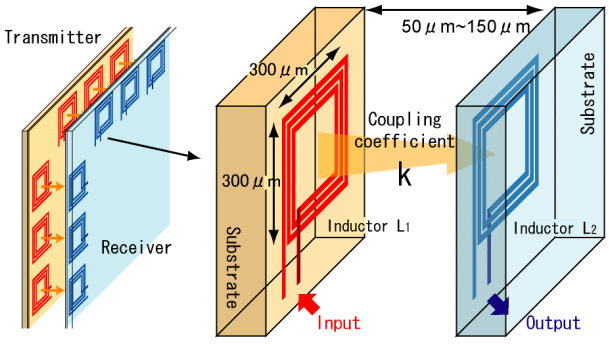

Fig.1 Spiral inductor based wireless interconnect.

2. Research Results

2-1. Analysis and modeling of spiral inductor pair

In order to utilize circuit simulators for the design, we introduce an equivalent circuit of the spiral inductor pair.

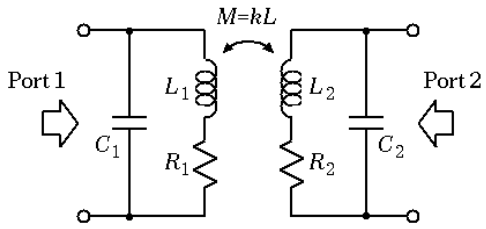

Fig.2 An equivalent model of spiral inductor pair.

Fig.2 shows the simple equivalent circuit. L, C, and R are the self-inductance, parasitic capacitance and loss resistance of the spiral inductor, respectively. M and k are the mutual inductance and the coupling coefficient between the spiral inductor pair. 2-port S-parameter data has been obtained from FDTD 3D electromagnetic-field analysis. Then, the element values in Fig.2 were calculated by data-fitting to the 2-port S-parameter data. The result is shown in Fig.3. In layout of the spiral inductor, line width and space were 10μm and 2μm, respectively. The shape was square and the outer diameter was fixed at 300μm. As parameters, the number of turns and distance between the spiral inductor pair were selected. Fig.3 shows the relationship between the self-inductance and the number of turns. It also shows the relationship of the coupling coefficient. The three curves are drawn, when the distance between the spiral inductor pair is 50μm, 100μm and 150μm, respectively.

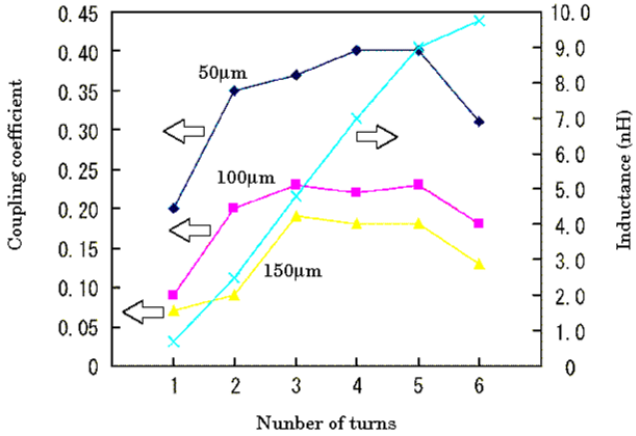

Fig.3 Results of 3D electromagnetic-field simulation.

2-2. Circuit configuration and SPICE simulations

Figure.4 shows a circuit diagram including the model of the spiral inductor pair. Note that capacitors Ca_1 and Ca_2

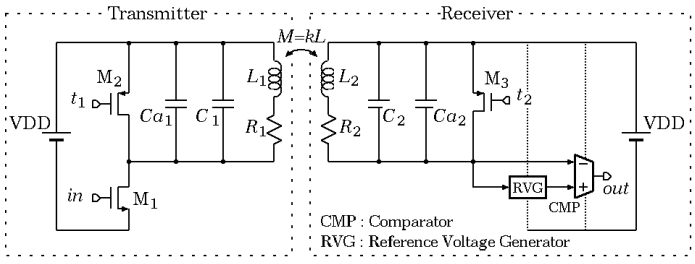

Fig.4 Circuit diagram.

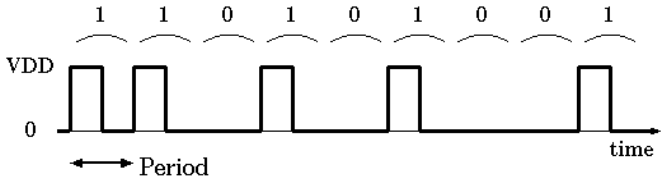

Fig.5 Return zero signal.

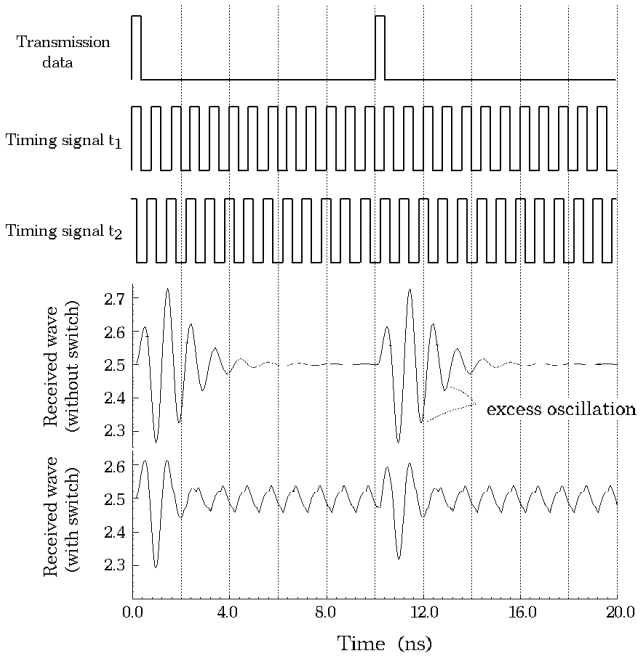

Fig.6 Simulation results.

are connected to the inductors L_1 and L_2, in order to implement resonators in both the transmitter and the receiver. Although the spiral inductor without the additional capacitor has self-resonant frequency, Ca_1 and Ca_2 reduce the resonant frequencies until the convenient frequency for typical communications. A MOSFET M_1 works as driver in the transmitter. A return zero signal shown in Fig.5 is given to the gate of M_1. The resonant frequencies of the resonators in both the transmitter and the receiver are made equal to the transmission frequency of the return zero signal, by connecting the capacitors Ca_1 and Ca_2. The resonance property enlarges the received signal. On the other hand, it causes the excess oscillation due to the resonance phenomenon as shown in Fig.6. In order to suppress the excess oscillation, MOSFETs M_2 and M_3 are employed. Timing signals t_1 and t_2 in Fig.6 control the M_2 and M_3, respectively. Thus, they short out L_1 and L_2 at the timing as shown in Fig.6 and can suppress the excess oscillation.

The timing signal t_1 for transmitter has same phase of transmission data. On the other hand, the timing signal t_2 should be tuned to the timing of the receiving data. The timing tuning can be realized by multiple phase oscillator and multiplexer as shown in Fig.7. Data-transmitting cycle is divided into eight phase by the ring oscillator composed of differential delay cells in 4 stages, as shown in Fig.8. The multiplexer selects the optimum clock phase among the eight phase clocks. The 125ps phase resolution is sufficient for 1Gbps transmitting and the timing control can be achieved digitally.

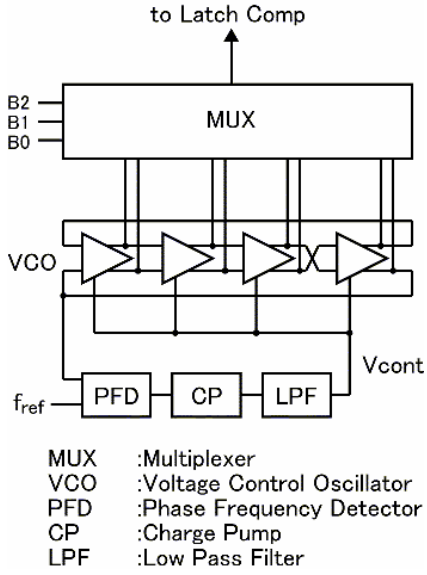

Fig.7 Timing tuning circuit

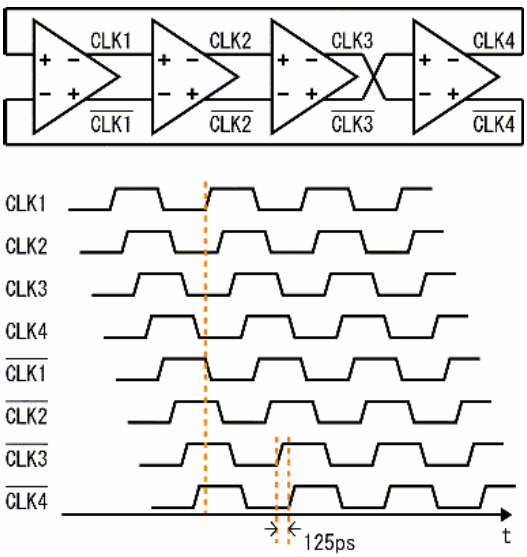

Fig.8 Ring oscillator and eight phase clocks.

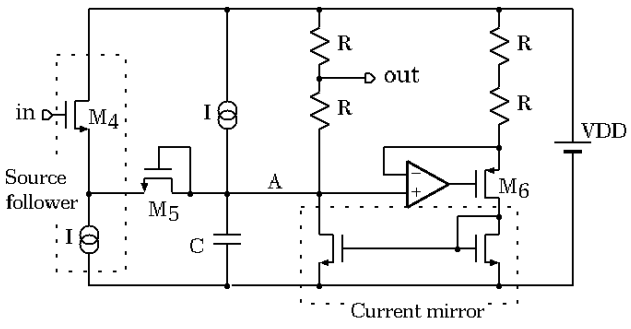

Fig.9 Reference-voltage generator.

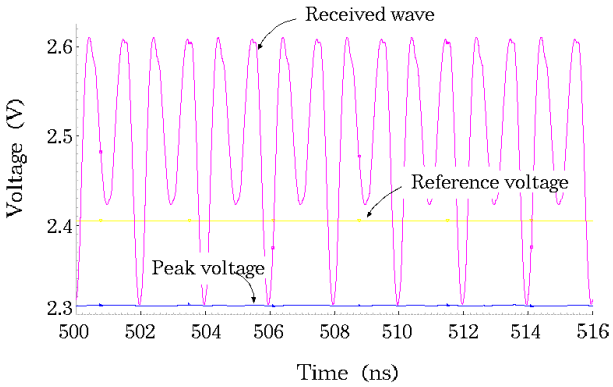

Fig.11 Simulation result of the reference-voltage generator.

The transmitter circuit and the receiver circuit including spiral inductors have been designed in TSMC 0.25μm mixed-signal CMOS technology and they were simulated by SPICE. In the simulation, the equivalent model of the spiral inductor pair is used. The supply voltage VDD is 2.5V, in all simulations. Fig.6 shows the simulation results. As shown in the lowest stage of Fig.6, the excess oscillation can be successfully suppressed, although the leakage of the timing signal t_2 through the parasitic element of M_3 causes a slight oscillation. The resonance property can enlarge the amplitude of the received signal and it results in lower power consumption. In fact, an average of the current flowing into the driver M_1, which consumes the most power, can be reduced down to 2.4mA.

The distance between stacked chips should be varied due to system level restrictions such as heat dissipation. It affects especially the amplitude of the received signal. In order to suppress the affection, a reference-voltage generator is proposed. Fig.9 shows the circuit diagram. It can generate a reference voltage for the comparator from the amplitude of the current received signal. A source follower buffers the received signal. Simultaneously, the voltage level is shifted down by the threshold voltage of the MOSFET M_4. Moreover, a peak voltage is detected by a MOSFET M_5 which operates as diode. Because the level-shift voltage of the source follower is equal to the threshold voltage of M5 working as diode, a peak voltage of the received signal can be obtained at the node A. The reference voltage for the comparator is generated by dividing the peak voltage into 1/2. However, the behavior of the reference-voltage generator is influenced by data sequence pattern. The good operation can be achieved in the sequence "…,1,0,1,0,1,0,…". In order to overcome this phenomena, channel bank is employed, in which one channel is exclusively used for the reference-voltage generation. The channel bank is illustrated in Fig.10. The control channel transmits the data sequence "…,1,0,1,0,1,0,…" and it is exclusively used for the reference-voltage generation. In the other channels, the latched-comparators in the receivers evaluate the data via the reference voltage generated by RVG in the control channel. The simulated results of the reference-voltage generator are shown in Fig.11 and a proper reference voltage can be obtained.

A simulation result of the communication channel including the output of the comparator is shown in Fig.12. In the first stage, the data sequence in the transmitter is described. In the middle stage, the received wave and the reference voltage are described. In the bottom stage, the received data sequence is described and it is same as the transmitted data sequence except the phase shift. Thus, the good performance has been confirmed.

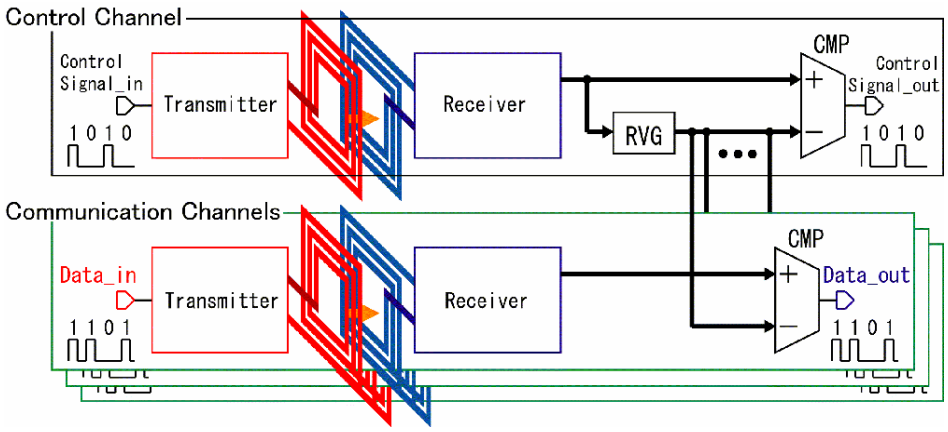

Fig.10 Channel bank employing same reference voltage

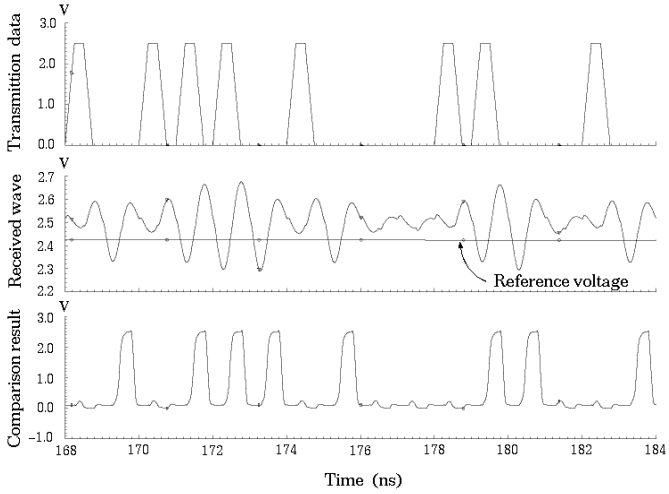

Fig.12 Simulation result of the communication channel.

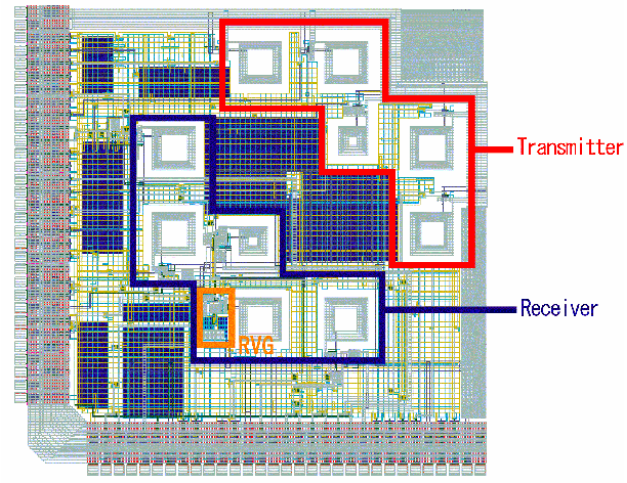

Fig.13 Chip layout

A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the proposed concept. The chip layout is shown in Fig.13. The evaluation board also has been developed and it is shown in Fig.14. Two evaluation boards are placed in face-to-face and the performance of the communication will be evaluated.

3. Conclusions

We have presented an interconnect scheme between the stacked chips based on resonant coupling of the integrated spiral inductor pair. The performance, 1Gb/s/channel at 9mW/channel, has been confirmed by SPICE simulation. A test chip has been fabricated in TSMC 0.25mm mixed-signal CMOS technology for evaluating the communication of the spiral inductor pair. The experiment with the fabricated chips will be accomplished soon.

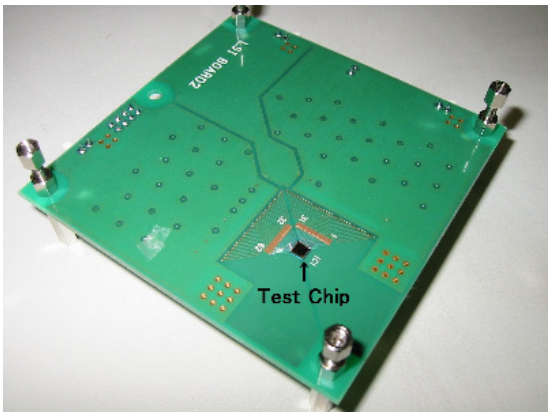

Fig.14 Evaluation board

4. Future plan

The next studies are "Size-reduction of the spiral inductor" and "less power consumption", which are necessary conditions for more multiplex channel communication. 100 channels for multiplex communication, 100mmx100mm size for spiral inductor, and 1mW power consumption per channel are next targets.

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5. Published Papers and Patents

① Published Papers

② Proceedings

1. M. Sasaki, D. Arizono, A. Iwata, "A wireless chip interconnection using resonant coupling between spiral inductors," *Proc. of Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing*, (2004) pp.104-108.
2. M. Sasaki, *et al*., "At-speed self-test LSI for high-speed serial link," submitted to *2004 International Conference on Solid State Devices and Materials* (*SSDM*).

③ Patents

1. Japanese Patent 2004-10053, "Semiconductor Equipment"

A Brain-type Vision System with Wireless Interconnections

Seiji Kameda (COE Researcher) ,
Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter)

1. Research Target

The vertebrate visual system processes huge visual information in real-time by massively parallel neural networks arranged hierarchically and adapts to a rapidly changing visual environment by an adaptive mechanism. Inspired by the unique architecture and algorithm of the vertebrate visual system, the neuromorphic vision chips or brain-type vision device, novel analog Very Large Scale Integrated (VLSI) circuits, have been fabricated ([4-6] for outlines). These neuromorphic chips, however, encounter a serious problem, namely, the trade-off between the resolution and the computational complexity of the chip. To solve the problem, multi-chip vision systems have been fabricated previously [1][5]. In these multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. On the other hand, a 3-Dimensional Custom-Stack System (3DCSS) has been proposed by our 21st Century COE program. In the 3DCSS, multiple chips fabricated by various technologies and arranged hierarchically are connected by two types of wireless connections, which are a local connection and a global connection. Due to the wireless connections, the 3DCSS overcomes a wiring complexity that is the demerit of the multi-chip system generally. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system. In the present study, In my study, I am aiming at a fabrication of the brain-type vision system incorporating the 3DCSS.

2. Research Results

2-1. Visual processing system using the 3DCSS configuration

We propose a visual processing system using the 3DCSS configuration. Fig.1(A) shows a design of the visual processing system. The system consists of an image sensing chip, a visual processing chip and an adaptive control chip. Fig.1(B) illustrates the block diagram of the image sensing chip. In the image sensing chip, an image obtained by photo sensors is processed by massively parallel arrays of processing circuits. The outputs of the image sensing chip are transferred to the visual processing chip using a local connection. The local connection are formed by a line parallel inductive coupling on spiral inductor pairs between a transmitter of the image sensing chip and a receiver of the visual processing chip [8]. Due to the line parallel method, the 2-dimensional huge visual information is transmitted very quickly. Fig.1(C) illustrates the block diagram of the visual processing chip. The input to a pixel of the visual processing chip from a corresponding pixel of the image sensing chip is memorized in an analog memory. The memorized data is processed by massively parallel arrays of processing circuits, too. The outputs of the visual processing chip are transferred to another visual processing chip using a local connection. As shown in Fig.1(A), on a surface of a system base, A power supply line, a control signal bus and output signal bus are arranged. A direct contact between these processing chips and the system base makes a power supply, an input of basic control signals and

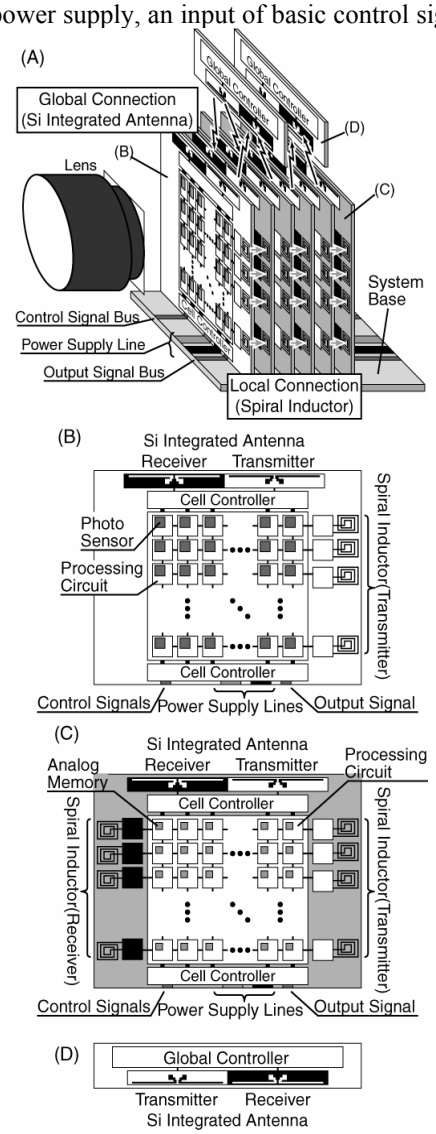

Fig.1 Visual processing system using the 3DCSS configuration. (A)System design, (B)block diagram of the image sensing chip, (C)the visual processing chip and (D)the adaptive control chip

a readout output by wired connection possible. Fig.1(D) illustrates the block diagram of the adaptive control chip. The adaptive control chip receives processing data from the image sensing chip and the visual processing chip, and controls these chips using a global connection. The global connection between the adaptive control chip and the processing chip are realized by a microwave communication utilizing integrated dipole antennas, which are integrated on

these chips for a transmitter and receiver circuits [7]. The adaptive control chip can control multiple chips at once. If these chips are arranged as shown in Fig.1(A), the image sensing chip and different varieties of the visual processing chips realize hierarchical and massively parallel image processing, and the adaptive control chips adapt to the visual environment and control the whole system immediately as found in the vertebrate visual system.

2-2. Prototype visual processing chip with a PWM-based line parallel interconnection

A prototype visual processing chip has been fabricated as a preliminary step toward fabrication of the visual processing system using the 3DCSS configuration. In our first attempt, the line parallel spiral inductor module was separated from the prototype visual processing chip. Namely, combining the prototype visual processing chip and independently-developed spiral inductor module chip makes possible an experiment of data transfer using the local connection. In the prototype chip, a pulse width modulation (PWM)-based data transfer method was adopted in order to fit a transmitter/receiver using the spiral inductor. In the transmitter/receiver, because a data format must be digital due to a constraint of the spiral inductor, an analog processed data must be converted into a digital data. In the PWM method, an analog voltage data is converted into a width of digital pulse in time domain [2]. The PWM method is suitable for the 3DCSS because the PWM and PWD (pulse width demodulation) circuits are realized simpler structure than a standard A/D and D/A converters. Fig.2(A) shows a block diagram of the prototype chip. The prototype chip consists of a cell array and a line parallel input and output units. In the cell array, processing circuits included an analog memory are arranged in a 44 x 40 matrix. The input and output units are arranged every 4 column of the cell array in a line (1 x 10) respectively. Fig.2(B) shows a circuit design of the input unit. The input unit is the PWD circuit consisted of a sample/hold circuit (Nbuf) [3]. In the input unit, if the sample/hold circuit is input into a ramp voltage and held by the PWM input, the analog voltage is proportional to the pulse width of the input. Fig.2(C) shows a circuit design depicting a single pixel. The input from its corresponding input unit is stored in an analog memory. The stored data in the analog memory is smoothed by the resistive network [3]. Fig.2(D) shows a circuit design of the output unit. The output unit is the PWM circuit consisted of a clocked CMOS comparator [2]. In the output unit, if a pulse has been generated until a ramp voltage is equal to the output voltage, the pulse width is proportional to the output voltage. Two prototype chips can be also linked by wired-connection. Therefore, it is possible to check the operation as multi-chip configuration without the spiral inductor module chip. The chip was implemented with a 0.35 um, double-poly, three metals, standard CMOS technology and the die size was 4.5 x 4.5 mm^2.

3. Conclusion and future

The visual processing system using the 3DCSS configuration is proposed. And as a preliminary step toward fabrication of the visual processing system, we have fabricated a prototype visual processing chip with a PWM-based line parallel interconnection. In the next step, I will have to verify the operation of the multi-chip system with wireless interconnection and consider visual processing algorithms.

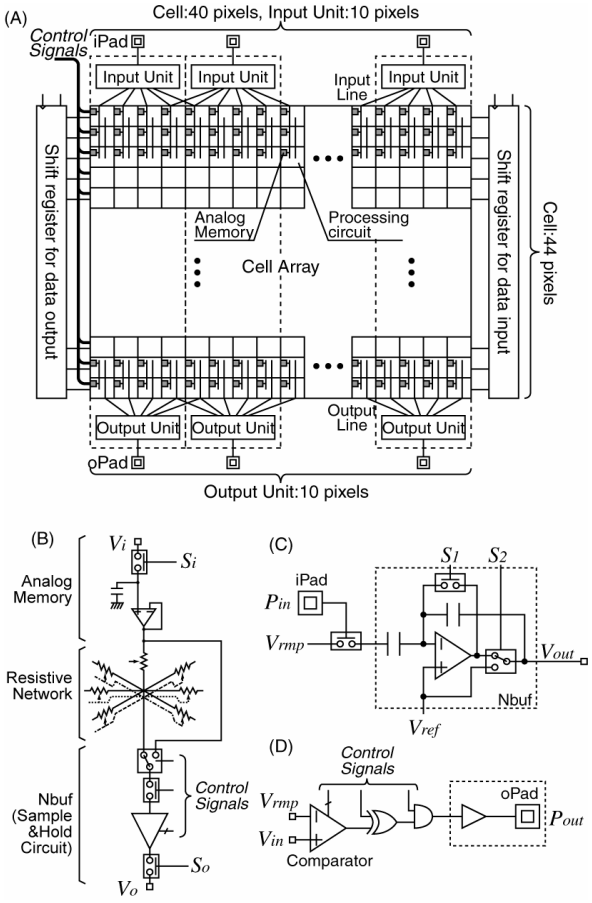

Fig.2 The prototype visual processing chip. (A)Block diagram of the chip, (B)circuit design of the single pixel, (C)the input unit and (D)the output unit.

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4. Patents

1. Japanese Patent 2004-022317(application), 2004.01.28

Development of Real-time Multi-object Recognition System

Hiroshi Ando (COE Researcher),
Atsushi Iwata (Prof. , Graduate School of Advanced Sciences of Matter)

1. Research Target

Image recognition is a very difficult task for a computer because of complexity of a natural scene. In order to recognize various kinds of object from a natural scene, robust image processing techniques are required under variation in size, orientation, lighting condition and so on. Moreover, it is also necessary to combine several image processing. The high-level information processing technologies realizing natural scene recognition is not developed at present.

On the other hand, a human brain can easily recognize complex images unconsciously. It seems that highly complex processing can be achieved by massively parallel behavior of a large number of neurons and hierarchical information processing architecture that integrates low-level image features extracted from an input into meaningful high-level image features over several stages.

The objective of our research is realization of highly intelligent information processing system that can recognize the variety and the various objects in a natural scene in an instant.

2. Research Results

2.1 A Concept of Multi-object Recognition System

For the purpose of developing a real-time/high-level recognition technology, we have been introduced a concept of multi-object recognition system composed of 3D custom stack of multi-functional chips [1]. The hierarchical and massively-parallel processing of human brain are achieved using multi-functional chips and local/global wireless interconnects among LSIs based on pixel-parallel circuit architecture. Furthermore, we apply the eigenfaces method which is one of the major pattern recognition methods using principal component analysis (PCA) [2] to the algorithm of our proposed system. The multi-object recognition system can composed of image sensor, image normalizer, objects detector, objects recognizer and multi-object database (DB) chips.

2.2 Eigenfaces Method with Principal Component Analysis

The eigenfaces method is based on the principal component analysis [3]. First, the face images in a dataset is decomposed into a small set of characteristic feature images, called eigenfaces, which are the orthogonal eigenvectors calculated from the face images. The eigenfaces are considered as the principal components of the original images. Next, a weight vector to represent face images as a linear combination of eigenvectors is calculated. Finally, by comparing the weight vectors of an unknown new face to those of dataset's images, an unknown face can be identified as a person.

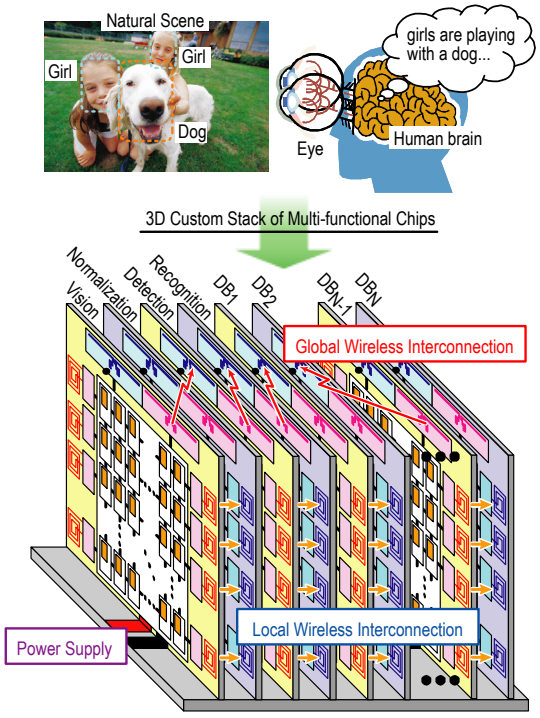

Figure 1: A concept of multi-object recognition system.

One can reconstruct an input image by using its weight vector and the eigenvectors of a dataset. If the Euclidian distance between input and reconstructed images is lower than a threshold, an input image should be identified with same class as a dataset.

2.3 Numerical Simulation of Human Face Recognition

We performed a numerical simulation of human face recognition by using the eigenfaces method. The face dataset composed of 10 persons is shown in Fig. 2(a). First, we calculated 9 eigenfaces and 10 weight vectors from these faces, and then searched each minimum distance between weight vectors for 4 input images as shown in Fig. 2(b). As a result, input images were recognized as output images, respectively, as shown in Fig. 2(c), even though there were some variations in face orientation.

Human face detection from a natural scene is shown in Fig. 3, where the eigenfaces of Fig. 2(a) were used for creating reconstructed face images. As a result of finding the image regions whose distances were lower than a threshold, only three human faces were detected exactly as shown in Fig. 3(a) and (b).

In above simulations, we treated only gray-scale images, but a real world is different. Therefore, we modified the algorithm to recognize a color image and executed numerical simulations again. As shown in Fig. 4(b), a candi-

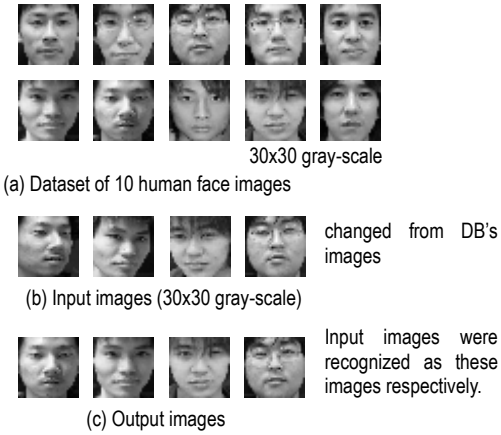

Figure 2: Numerical simulation results of human face recognition.

Figure 3: Numerical simulation results of human face detection.

date for human face was extracted using skin color information (HQ color space), and face detection and recognition were achieved successfully.

Moreover, we developed a prototype real-time human face recognition system composed of personal USB camera and software based on Win32API as shown in Fig. 5. This system can operate about 10 frame/s and recognize one or more human faces between each frame.

3. Conclusion

We proposed a concept of the multi-object recognition system composed of 3D custom stack. We also confirmed human face detection in a natural scene and recognition under some variations using the eigenfaces method by numerical simulation. Moreover, we developed a prototype real-time human face recognition software system.

We are scheduled to extend the eigenfaces method to multi-object recognition and realize their VLSI implementation.

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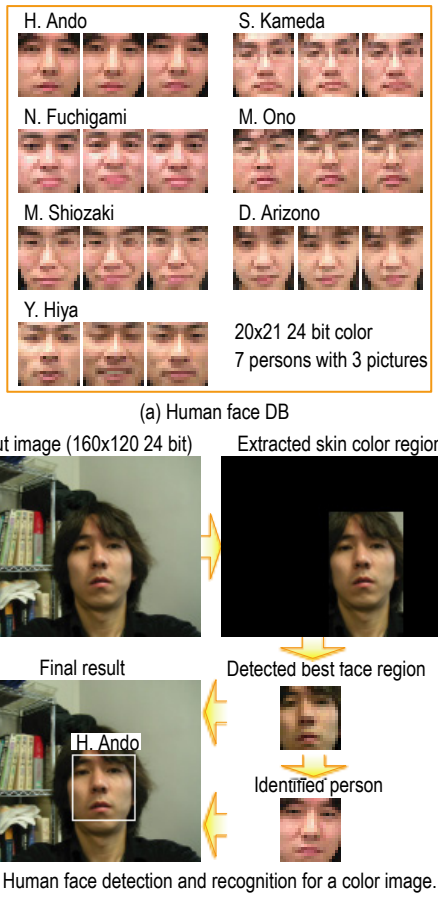

Figure 4: Numerical simulation results using color information for natural scene recognition.

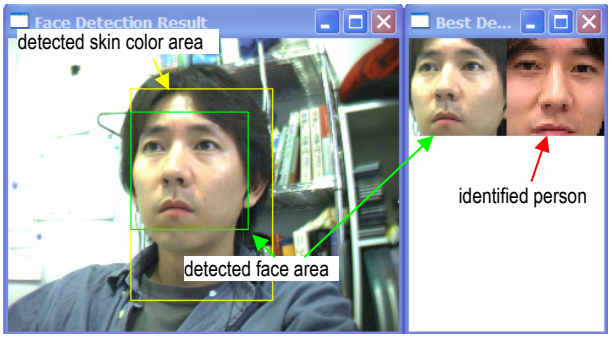

Figure 5: A prototype of real-time multi-object recognition system (now only human face).

Published Papers and Patents

① Published Papers

1. H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata "Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques", IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, 2002.

② Proceedings

1. H. Ando, T. Morie, M. Nagata and A. Iwata, "An Image Region Extraction LSI Based on a Merged/Mixed-Signal Nonlinear Oscillator Network Circuit", 28th European Solid-State Circuits Conference (ESSCIRC 2002), September 2002, Florence, Italy

A Study on Neural Sensing System

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1. Research Target

For advanced clinical and biometrics applications, various implantable neural sensors are fabricated by CMOS-LSI technologies [1, 2]. However the CMOS device has a large flicker noise and deviation of threshold voltage, CMOS Operational-amplifier (Opamp) hardly amplifies a weak neural signal. Thus the system has to implement a low-noise amplifier which can reduce these noises. Moreover, the implantable systems need a reception of system control-commands and a transmission of sensor data using a wireless communication.

In this paper, we propose the architecture of a neural sensing system, which includes low-noise amplifier and wireless transceiver implemented with a conventional CMOS technology. This study is related to RF analog circuits technology of 21st century COE program Hiroshima University.

2. Research Results

2.1 Neural Sensing System Architecture

The block diagram of the proposed neural sensing system is shown in Fig. 1. The system consists of the MUX/AMP block, 10-bit ADC, wireless TX/RX block and system control block. The multi-channel probe and wireless antenna are implemented by discrete devices.

The MUX/AMP block needs about 80-dB voltage-gain and a reduction of a flicker noise and a voltage offset, because the neural signals are typically a few ten-μV and a few kHz. In addition, the MUX/AMP block chooses any 5-channels from the multi-ch probe and the selected channels are multiplexed at a pulse width of 20-μs in order to observe the neural signals simultaneously. The ADC converts the multiplexed signal to digital data at 10-bit resolution and 10-k-sampling-per-sec (ksps) sampling rate per channel. Therefore, the system can analyze a propagation of neural signals in the large neural network.

The TX/RX block needs to transmit a measurement data to the external receiver; and the block also receives a system control data, such as a measurement channel selection and voltage-gain control, from the external transmitter. Therefore the TX/RX block consists of transmitter (TX), receiver (RX) and voltage-controlled oscillator (VCO). The data transmission rate of neural sensing system is 500-kbps, because the ADC is operated at 10-bit resolution and 10-ksps sampling rate. In order to achieve the high-transmission rate, the VCO supplies a carrier signal of 100-MHz to the TX/RX block.

2.2 Design and Test-Chip Evaluation Results

A test-chip of the proposed neural sensing system was designed and fabricated with a 0.35-μm 2-poly 3-metal CMOS technology.

The block diagram of MUX/AMP block is shown in Fig. 2. The MUX/AMP block, which is implemented using a direct chopper input scheme, is possible to detect a neural signal through a polarized charge of probe interface. Moreover, the chopper technique reduces the flicker noise and dc-offset voltage of Opamps. The MUX/AMP block amplifies a difference between a detected voltage nearby focused neuron and a reference voltage (Vref) defines a voltage of cell liquid far from the observation neuron cell. From the SPICE simulation, the chopper amplifier achieved an equivalent input noise of 23 nV/root-Hz at a 400-kHz chopper frequency. A total in-band noise (~100 kHz) was 7.2 μV.

The TX/RX block diagram is shown in Fig. 3. The TX block transmits the ADC output data to the external receiver using the binary phase-shift-keying (BPSK) modulation. And this block equipped with the modified frequency-modulation (MFM) encoder, because the MFM achieves about 50-% mark ratio of transmission data.

Figure 4 shows the microphotograph of the test chip. The test chip includes a MUX/AMP block, an ADC block and a TX block, and the chip area is 25-mm^2. Measured Output spectra of TX block with BPSK modulation is shown in Fig. 5. The VCO operated at a frequency of 110.6-MHz, and the TX block achieved the data transmission rate of 1 Mbps. The power dissipation of VCO is 0.6-mW at a supply voltage of 3 V.

We evaluated the proposed MUX/AMP block to measure a nerve fascicle of cricket foot. Figure 6 shows the measured waveforms of (a) an amplifier implemented by commercially discrete Opamps and (b) the proposed MUX/AMP. The amplifier has a 66-dB DC-gain and band-pass-filter with 20-Hz to 5-kHz bandwidth. The external curve of pulse signal shows a measured neural signal. The proposed neural sensing system achieved a detection of the neural signal. The MUX/AMP accomplished a 66-dB voltage-gain, 3.2-μV in-band noise (~100 kHz) and 6.0-mW power dissipation at a supply voltage of 3-V.

3. Relation between COE Program and Results

The Planned image recognition system implemented by 3-dimensional custom stack of multi-chip that needs the technology of biometrics and RF interface. Therefore, these research results are adapted to the circuit design and the architecture in the planned prototype system.

4. Conclusions and Plan for the Future

We proposed the architecture of a neural sensing system, which includes low-noise amplifier and wireless transceiver implemented with a conventional CMOS technology. The proposed system achieved the RF data transmission rate of 1-Mbps and observation of

neural signals. In the future, we study for lowering noise of sensing system, in order to realize an observation of a few-μV neural signal.

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3. Published Papers and Patents

① Published Papers

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② Proceedings

1. T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input Channels", Proc. of Workshop on SASIMI, pp. 206-210, 2003.
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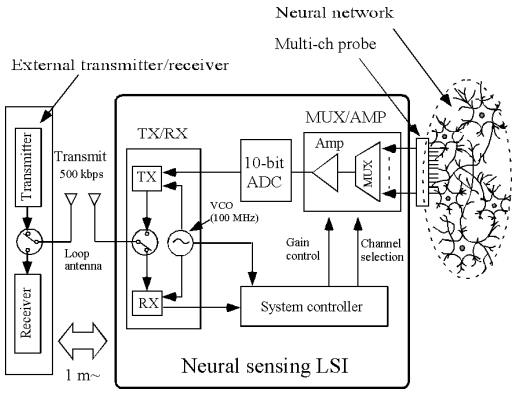

Fig.1 Proposed system architecture.

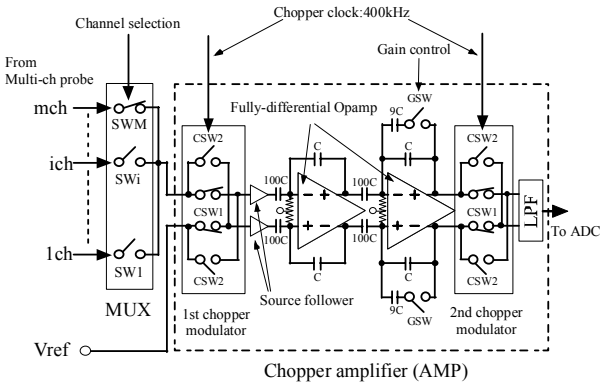

Fig.2 Schematic of the MUX/AMP block.

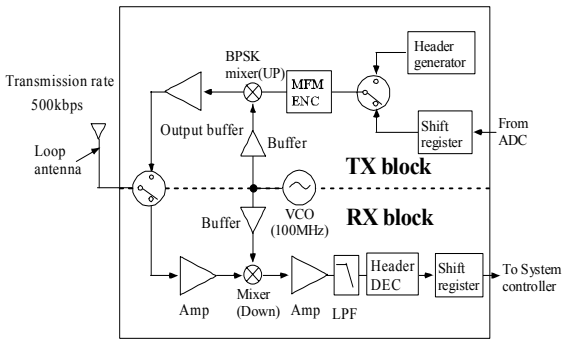

Fig.3 TX/RX block diagram.

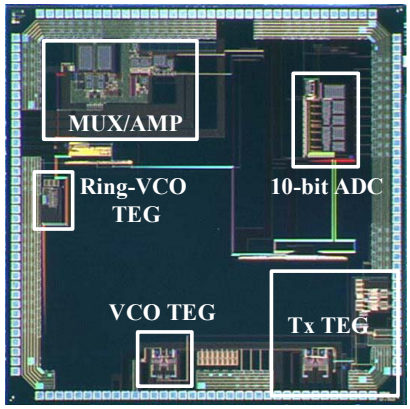

Fig.4 Microphotograph of the test chip.

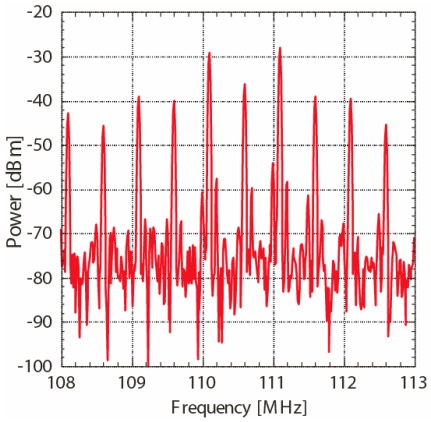

Fig.5 Measured output spectra of TX block.

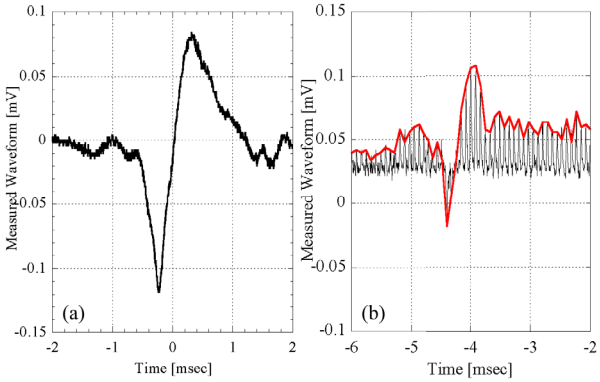

Fig.6 Measured nerve facile waveform of (a) the amplifier implemented by the discrete Opamps and (b) the proposed MUX/AMP.

CDMA Serial Communication Chips for Highly Flexible Robot Brain

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Mamoru Sasaki (Associate Prof., Graduate School of Advanced Sciences of Matter)

1. Research Target

Various serial interface standards, e.g., USB, IEEE-1394, etc have been established for multimedia applications. However, they do not have sufficient feature for robot control systems, in which various sensors, imagers, actuators and processors are connected as network. The robot control network requires real-time communication so as satisfy the restriction on the sampling time. Furthermore, it has communicated various amounts of data, e.g., commands to the actuators being little amount and huge image data from the imagers, etc. In addition, the network should be implemented with a few wiring lines, so that the actuators can smoothly move.

We propose a communication scheme suitable for the robot control system. A key idea is CDMA serial communication. The CDMA technique is used for data multiplexing and it realizes many virtual paths on the single wiring.

Several researches have been reported, in which CDMA scheme has been implemented with wired communication [1] [2]. CDMA has been implemented with bus configuration in [1]. In the case of the robot control system, if the bus configuration is adopted, the impedance matching becomes very difficult and it results in low data-transfer rate. CDMA scheme has been employed on serial link in [2] and high data transfer rate can be expected in the combination. However, if the number of multiplexing increases, the synchronization between the transmitter and the receiver becomes difficult. Although CDMA scheme has been employed, it has not achieved a lot of multiplex communication in [2]. It is very difficult that the synchronization technique developed for conventional serial link is employed for the CDMA serial link, because it seems to be PAM (pulse amplitude modulation) system with many amplitude steps. We propose a two-step synchronization technique, code synchronization and chip synchronization, which is based on the technique in the conventional CDMA system, not in the conventional serial link.

2. Research Results

The code synchronization can adjust the start timing for the decoding (despreaded) operation to the received sequence and it corresponds with the initial acquisition process in conventional CDMA system. The chip synchronization employs DLL (Delay Lock Loop) with a 2-delta delay discriminator and it can adjust the pulse timing. The receiver chip's block diagram is shown in figure 1. The number of the wave samplers is equal to the length of the spread codes. The multiple clocks control the de-interleaved timing and they are given by the ring oscillator, although the MUX and the voltage-controlled delay circuits exist between the wave samplers and the ring oscillator. The MUX and the voltage-controlled delay circuits are needed for the synchronization.

The receiver chip was fabricated in a 0.25um digital CMOS technology to demonstrate a 2Gbps, 7-multiplexing CDMA serial link. The 2.4mmX4.0mm die photo is shown in Figure 2. The amplitude of the transmitted differential signal for one code is set to 100mVp-p and the multiplexed wave has 800mVp-p swing because the number of codes is 8. Because the 2Gbps signal is de-interleaved into the 8 wave samplers, the decoders operate at the 250MHz system clock. The ring oscillator consists of 8 stages.

Figure 3 shows the measurement results of the first one of the sampler clocks. The left and right are the sampler clocks during the code synchronization and during the chip synchronization, respectively. Because the clock is always shifted by MUX during the code synchronization, the 8 phases of the clock overlap each other. On the other hand, the phase is fixed during the chip synchronization. The measurement results of the differential control voltages Cnt+ and Cnt- for the voltage-controlled delay circuits are also shown in Fig.3. They are fixed at 1.9V and 0.7V during the phase of the code synchronization. Cnt+ and Cnt- are adjusted and locked in the DLL, during the phase of the chip synchronization.

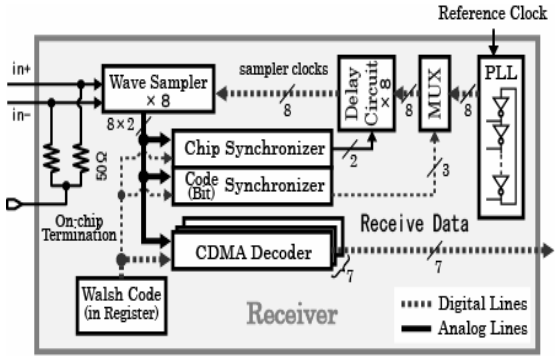

Fig.1 A block diagram of the CDMA serial receiver chip.

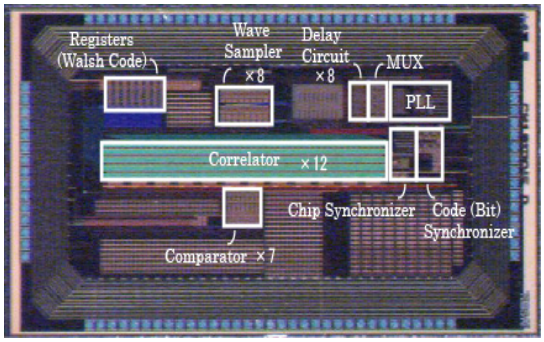

Fig.2 Chip micrograph.

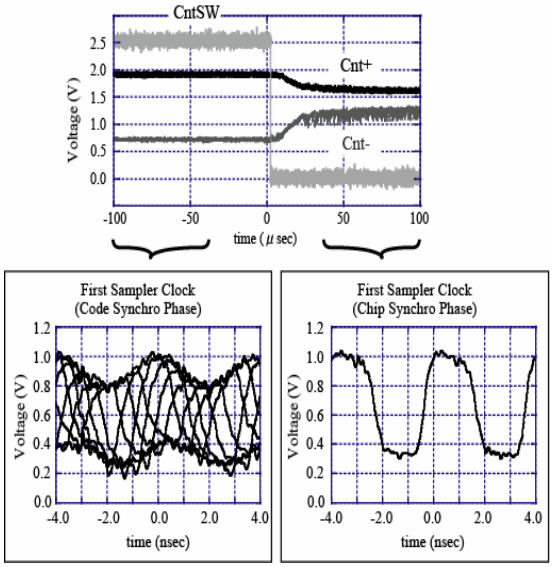

Fig.3 Measurement results.

3. Summary and future plans

A 2Gbps and 7-multi-plexing CDMA serial interface and the receiver circuit are proposed. The key techniques of the receiver chip are the two-step synchronization and its circuit implementation. The receiver chip fabricated in a 0.25um digital CMOS technology achieves a 2Gb/s data-transfer rate and synchronization of 7 multiplex communications.

Now, we are designing a transmitter chip based on the proposed serial CDMA scheme in order to demonstrate the CDMA serial link in the completed form.

4. Relation between COE program and our results

A network in the robot has few examples of use other than wired communication. These reasons are that an incorrect operation and reckless run of the robot are caused by the noise generated from other equipments. So, wired communications are excellent in an intelligence leak, a noise or cost. But it is not suitable for real-time communication with the 3D-integrated-system developed by the COE program. In addition, there is also a physical problem of wiring. In such a case, chips of this research are effective.

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2. M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, “A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System,” 2004 Symposium on VLSI Circuits. (This will be presented on Jun. 18, 2004. [Session 13-1])

Design of a Strategy Learning Model for Robot Brain and LSI Implementation of the Model

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Mamoru Sasaki (Associate Prof., Graduate School of Advanced Sciences of Matter),
Atsushi Iwata (Prof., Graduate School of Advanced Sciences of Matter),

1. Research Target

Recently, the progress of robots is remarkable. It is expected that the role which robots will bear in society from now on is expanded more, and the demand of robots will increase. The research of the robots which interact with persons such as welfare robots and communication robots, is mentioned as one of the fields from which the success is especially expected. The environments and the situations (person's characteristics) which the robots recognize tend to change very quickly because of the persons' learning. Under that condition, it is necessary for the robots to have more robust brain (We call it "Robot Brain") in order to accomplish the tasks. It can recognize person's characteristics and choose the most suitable action according to memorized experiences obtained by learning. We have two research targets. The first target is to propose a model for the Robot Brain which accomplishes the above process and to evaluate the effectiveness quantitatively using a numerical simulation. The second target is to realize the model by the custom LSI which is very compact and has low power consumptions.

2. Research Results

The proposed model is shown in Fig.1. It consists of the three sections: 1. selection of a strategy, 2. construction of a new strategy by learning, 3. addition of it or elimination of some strategies. At first, the opponent's behavior is observed in order to estimate his characteristics. Secondly, using the estimation result, the optimum strategy for the current opponent is selected from many candidates stored in the memory. This is carried out in the first section. The many strategies have been obtained by past learning. The selected strategy is copied into working memory. The robot acts based on the copied one. Thirdly, actions are decided according to the strategy in the working memory, and simultaneously the strategy is tuned in order to obtain better one. This is carried out in the second section. Finally, the tuned one is estimated with a criterion. It is added in the memory, if the estimation judges that it is needed. And, some needless strategies are eliminated to restrain memory overflow. This is carried out in the third section. We have devised only the first and second sections, and evaluated their effectiveness.

We briefly explain the algorism of the first section and the second section. We start the explanation of the second section, to easily understand the model. The algorism in this section is Reinforcement Learning (RL) [1]. We define a strategy. It consists of a set of ``situation" and ``action" pairs. By another expression, it consists of a set of if-then rules. Here, Q-function, $Q_x(\mathbf{s}_i, \mathbf{a}_j)$ has very important role. x is an index expressing each strategy. It expresses the quality of an action $\mathbf{a}_j$ in a situation $\mathbf{s}_i$ (larger Q_x means that an action is better). In the situation $\mathbf{s}_i$, an action is decided according to $Q_x(\mathbf{s}_i, \mathbf{a}_j)$. The robot is given a positive reward (or a negative reward) in the case of achieving its goal (or not), after the robot's taking the action. $Q_x(\mathbf{s}_i, \mathbf{a}_j)$ is updated by the reward. The strategy learning means updating $Q_x(\mathbf{s}_i, \mathbf{a}_j)$ by using the rule. Next, we explain the first section in Fig1. Q-function can be also employed in order to evaluate the opponent's characteristics. So, we prepare $Q_{obs}(\mathbf{s}_i, \mathbf{a}_j)$ which is Q-function, for evaluating the opponent's characteristics. As well as Q-function in the second section, Q_{obs} is also updated during a sequence. The strategy with the closest Q_x to Q_{obs} is selected.

In order to confirm the ability of the model, we applied it to "air hockey game" as the example of the task which needs persons. In this experiment, an opponent is the same program with a simple strategy. The strategy is fixed and is not tuned by learning. We had many experiments by varying the opponent's characteristics. Fig.2 shows one of the experiments. The opponent's characteristic has been varied by stick position as shown in Fig2. Fig3 shows the result of the experiment. The stick position of the opponent changes from A to E (see Fig.2) every set. It is one set in 20 points. The number of the stored strategies is four. Before the experiment, the four strategies have been obtained by learning in cases that the stick positions of opponent are fixed at A, B, C and D, respectively. The strategies are called S_A, S_B, S_C and S_D. Fig.3 shows that proper strategy except B was quickly selected. Here, we consider the case of the position B. It is the second set. Fig.4 shows that the robot overwhelmingly won even by using the Sc. So, the model has also selected the proper strategy in this case. Next, let us consider the case of the position E. Note that no strategy has been previously prepared for the position E. In order to confirm the selection of Sc for the position E is appropriate, we had another experiment. In the experiment, we applied the strategies from S_A to S_D to the position E. Fig.5 shows the result: The Sc is the best strategy because the robot overwhelmingly won as comparison with the others. From the above discussions, the model's effectiveness has been confirmed apparent.

3. Relation between COE program and this research result

A target of COE program is "Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures".

Therefore, we can provide COE program with this research result, “a strategy learning model” as the learning function of the integrated systems by integration technologies.

We will apply this model to the 3-demension integration system which is the goal of COE program. At first, we will realize Sec.1, Sec.2, and Sec.3 in Fig.1 on a custom LSI chip. Secondary, several LSI chips is used as the memory of strategies in Fig.1. The function of this model will be realized by communicating between the chips with wireless integration technology. We will be able to contribute to the accomplishment of COE program target by embedding high-level learning capabilities into 3-demension integration system.

4. Conclusion and Schedule

To realize Robot brain, which can execute tasks interacting with persons, we have proposed a model with RL. The model can select the most suitable strategy so quickly and construct a new strategy by learning. It was confirmed by the simulation experiment. In present study, we use the virtual opponent. As the next step, we’ll have the experiment using a person as the opponent, and we’ll design the circuit which has functions of this model.

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3. Published Papers and Patents

Proceedings

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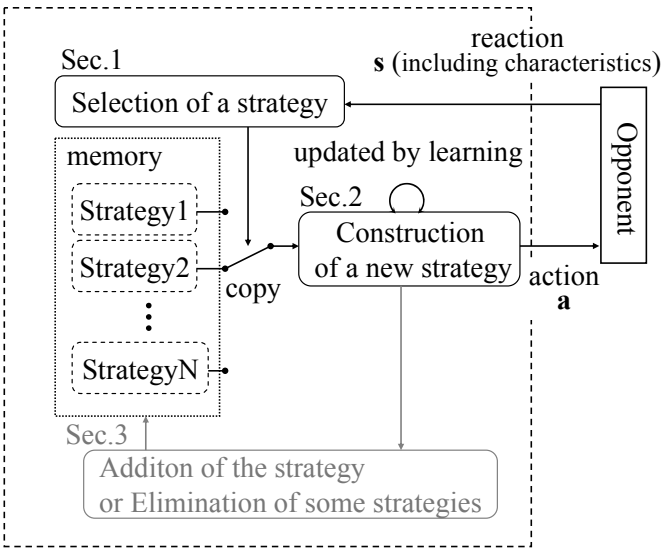


Fig. 1: A proposed model for Robot brain

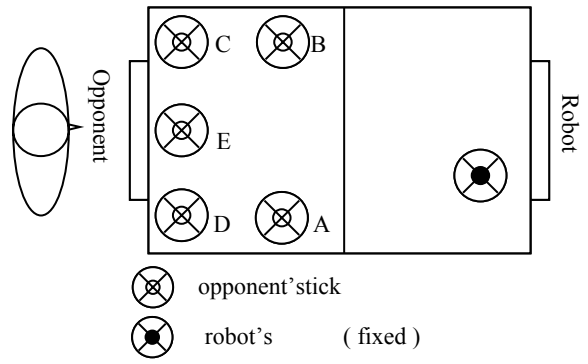


Fig. 2: An example of the opponent’s characteristics

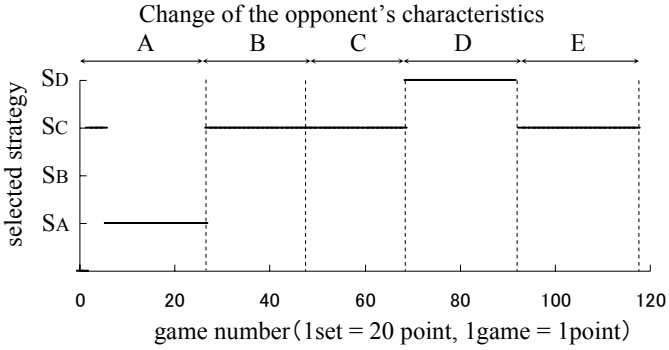


Fig. 3: The result of the experiment where the opponent’s stick position changes A from E by one set(= twenty points)

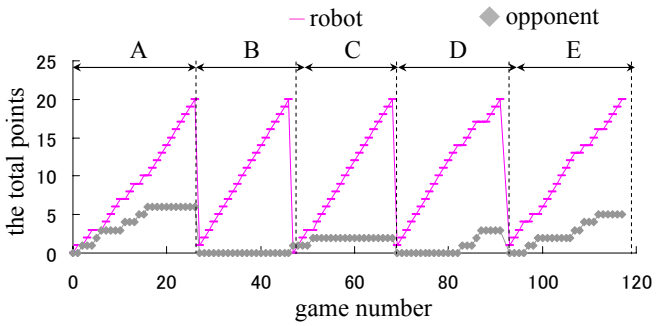


Fig. 4: The total points that the robot and the opponent got

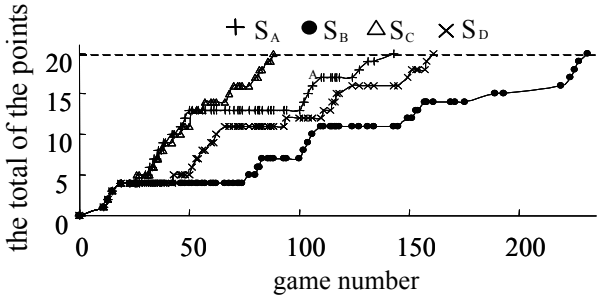


Fig. 5: The total points given to the robot by using each strategy during position E

Associative-Memory-Based Systems with Recognition and Learning Capability

- Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search in Large Reference-Pattern Space -

Representative : Hans Jürgen Mattausch (Prof., Research Center for Nanodevices and Systems, Graduate School of Advanced Sciences of Matter)
Cooperator : Tetsushi Koide (Associate Prof., Research Center for Nanodevices and Systems, Graduate School of Advanced Sciences of Matter), Yuji Yano (Graduate School of Advanced Sciences of Matter, M2), Kazuhiro Kamimura (Faculty of Engineering, B4), and Kazi Mujibur Rahman (COE Researcher)

1. Research Target

In order to realize intelligent data processing such as feature extraction, recognition, rough judgment and learning, which are usually done in the human brain, a memory-based, flexible system architecture is necessary. The intelligent-system target requires breakthrough solutions for circuits realizing two basic functions: dense, high-interconnectivity data-storage as well as fast, low-power pattern matching. Therefore, we are developing area-efficient multi-port memories and fully-parallel mixed analog-digital associative memory architectures.

The associative-memory functionality is to find the nearest-match between an input-data word of W bit length and a number R of reference-data words. Since this functionality is a basic operation for such applications as image or voice pattern recognition [1], codebook-based data compression [2, 3, 4], routing-table-lookup for network routers, and authentication parts in security system (Fig.1), it is important to find efficient solutions for its practical realization. For the example of codebook-based image compression, shown in Fig. 1(b), the pattern of a 4 x 4 macro block of pixels is approximated by the nearest-match pattern in a codebook, storing the reference patterns of blocks typically occurring in real images as templates. Only the code-number of the best matching pattern, called winner-pattern number, is transmitted. The decompression is achieved by restoring the corresponding pattern at each location of the image from the codebook [3, 4]. Since the pattern matching is a very computationally expensive process, a hardware solution is preferable for real-time applications.

The nearest-match or winner is defined by the minimum with respect to a distance measure. Practically important distance measures are the Hamming (data strings, voice patterns, black/white pictures) and the Manhattan (gray-scale or color pictures) distance. In general, the distance measures can be represented by eq. (1),

$$D_i = \sum_{j=1}^{w} | IN_i - REF_{ij} | \qquad (1)$$

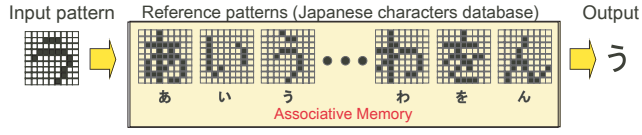
where $IN=\{IN_1, IN_2, \ldots, IN_w\}$ and $REF_i=\{REF_{i1}, REF_{i2}, \ldots, REF_{iw}\}$ are input-data and ith reference-data word, respectively. D_i is called Hamming distance, when IN and REF_i consist of 1-bit binaries, as e. g. for pixel groups from black-and-white pictures. $|IN_i - REF_{ij}|$ can be implemented with a simple EXOR gate and D_i represents the number of non-matching bits. D_i is called Manhattan distance, when IN_i and REF_i consist of n-bit ($n>1$) binaries, as e. g. for pixel groups from gray-scale or color pictures. $|IN_i - REF_{ij}|$ requires subtraction plus absolute-value function and has thus substantially higher integration complexity.

Both software and hardware solutions for the associative-memory function are possible. However, a hardware solution is preferable for applications where the search time is the major issue.

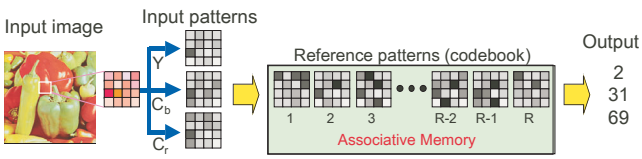
The purpose of this project is to provide a new hardware solution for the associative-memory function with the Hamming distance and the Manhattan distance measures. The solution should improve the performance of previous hardware solutions by at least 1 order of magnitude and combine short nearest-match (or winner) search times with the possibility of compact implementation in conventional CMOS circuit technology on a single chip. In particular the nearest-match circuitry should not scale with the square of number of reference words but should be only a linear function of the number of reference words.

Conventional methods for nearest distance-search have been based on: (a) analog neural networks [5], (b) SRAMs and a separate digital winner-take-all (WTA) circuit [3], (c) an analog WTA based on MOSFETs in source follower configuration [6] or a time-domain concept [7]. Problems of these solutions are: Large area-consumption [3, 5, 6] because the search circuits are of order R^2 ($O(R^2)$) or $O(R*W)$ complexity. Long search-times of about 1μs or more [3, 5]. Restricted applicability to small W [6].

To overcome these drawbacks, we have proposed a dedicated mixed analog-digital fully-parallel associative-memory architecture for nearest Hamming/Manhattan-distance search. Moreover, for the reliable handling of a large number of reference-patterns, we also have presented a bank-type associative-memory architecture as a reliable solution to the remaining issue of nearest-match search in a large reference-pattern space. Additionally, we disclose an efficient circuit for implementing the Hamming/Manhattan-distance-search function



(a) Image pattern recognition (Hamming-Distance).



(b) Codebook-based data compression (Manhattan-Distance).

Figure 1: Application examples of the associative-memory-based system. (a) pattern recognition (Hamming-distance-measure) (b) vector quantization for image compression (Mannhattan-distance measure).

within the memory field. Designed minimum Hamming/Manhattan-distance-search associative memories have high-performance at low-power dissipation.

2. Research Results

2.1 Associative-Memory Architecture for minimim Hamming/Manhattan-Distance Search

Figure 2 shows the block diagram of our proposed compact associative memory with fast fully-parallel match capability according to the Hamming/Manhattan distance. The memory part on the left side consists of conventional read/write periphery for storing the reference-data words and for reading out the nearest-match data. The search word is supplied from above, preferably on the bit-lines of the memory field, when the associative-memory function is carried out. A row of the memory field contains W storage units (SC), each which k bits plus the circuitry for unit (UC) - and word (WC) -comparison. The word-comparison results C_i are transferred to the winner-search circuit on the right side consisting of the winner-line-up amplifier (WLA) and a winner-take-all circuit (WTA). Important is the closely coupled interaction of WLA and WCs, by which the desired maximum amplification of winner-loser distances for all search cases is achieved. The output signals LA_i of the WLA are finally evaluated by the WTA to decide on the row, which contains the winner data.

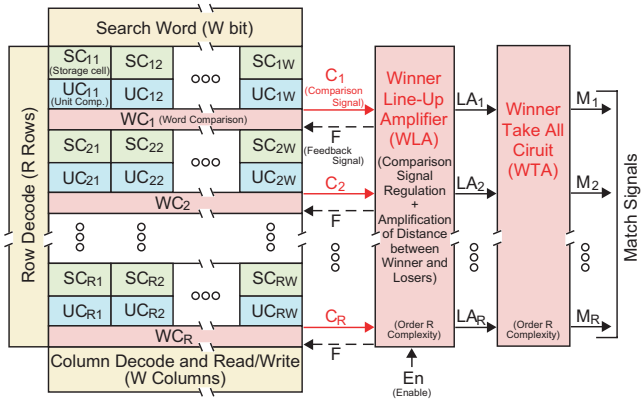


Figure 2: Block diagram of the compact-associative-memory architecture with fast fully-parallel match capability according to the Manhattan distance.

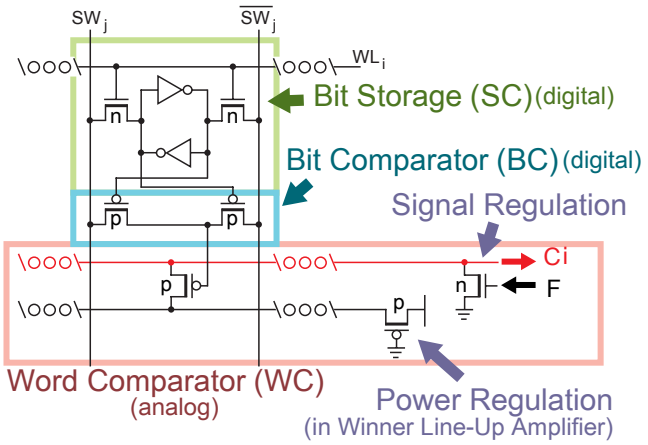


Figure 3: Architecture of the memory-field of a mixed digital/analog associative-memory for Hamming-distance search.

The concept for the memory-field for Hamming/Manhattan-distance search is illustrated in Figs. 3 and 4, respectively. For Manhattna-distance search, digital k-bit subtraction and absolute-value calculation units (UC) compare the W binaries, each with k-bit, in all rows of the memory field in parallel with the reference data. The k-bit subtraction circuit can be realized on the basis of a ripple carry adder circuit. In the test chip design, we use a newly devised compact circuit to minimize its design area. Fig. 5 shows the circuit diagram for our k-bit subtraction and absolute-value calculation unit. The transistor number of the this optimized circuit is only 20k-2. On the other hand, that of the conventional implementation needs 50k-18 transistors. So nearly 60% reduction of the transistor number can be achieved by using our newly developed circuit.

The word comparator (WC) circuit for Manhattan distance is implemented as shown in Fig. 4. To realize the WC function for Manhattan distance, the gates of the WC-transistors are connected to the corresponding k-bit output-signal lines of the unit comparator (subtractor and absolute value circuits), while their drains are connected to the corresponding output-signal line C_i. The gate width of each WC-transistor, $2^{k-1} * W_0$, varies depending on the bit position of the k-bit binary so as to distinguish each bit-weight. Since UC outputs are 0 for matching bits, WC-transistors are "off" for matching and "on" for non-matching bits. Thus small current-sink capability corre-

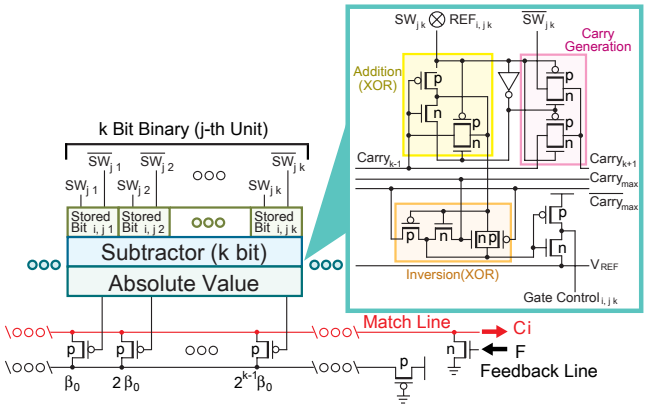


Figure 4: Architecture of the memory-field of a mixed digital/analog associative-memory for Manhattan-distance search.

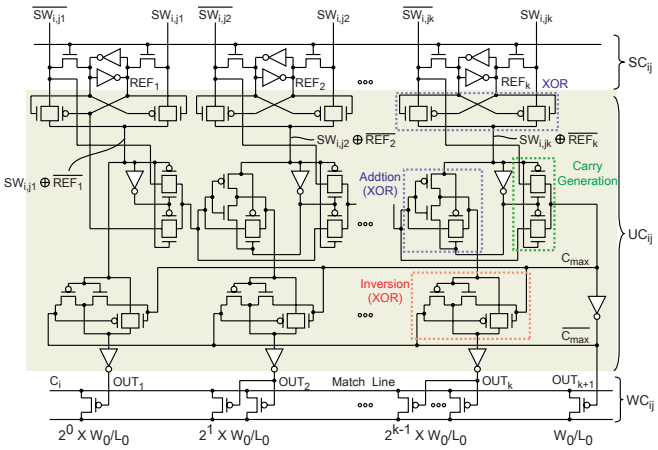


Figure 5: Newly developed circuitry for k-bit subtraction and absolute-value-calculation.

sponds to “good” matches, while large current-sink capability corresponds to “bad” matches.

Figure 6 explains the principle of self-adapting winner line-up amplification, which was implemented in an improved winner-line-up amplifier. In a previous design, the maximum gain region of the WLA was fixed and the WC output of the winner-row had to be aligned to this narrow region. This constraint limited the design freedom for the WLA quite significantly and included the danger of over- or under-regulation. In the current design, we eliminated this problem with an adaptable maximum-gain region of the WLA, which follows automatically the input voltage C_i of the winner-row. Exploiting this new design freedom leads to a drastically improved performance of the WLA. We will explain the implementation of this important new principle of a self-optimizing WLA circuit

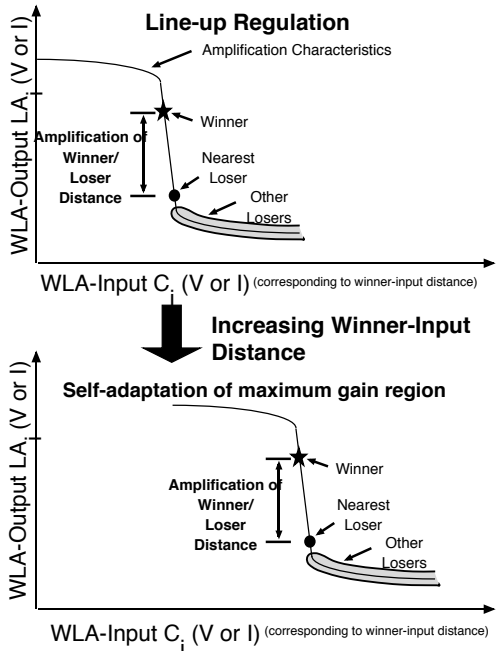


Figure 6: Selef-adapting winner line-up amplification principle. Regulation of WC outputs so that the winner-loser distance is amplified by the maximum gain follows automatically the input voltage C_i of the winner-row, that is the increasing of winner-input distance, for all possible search cases.

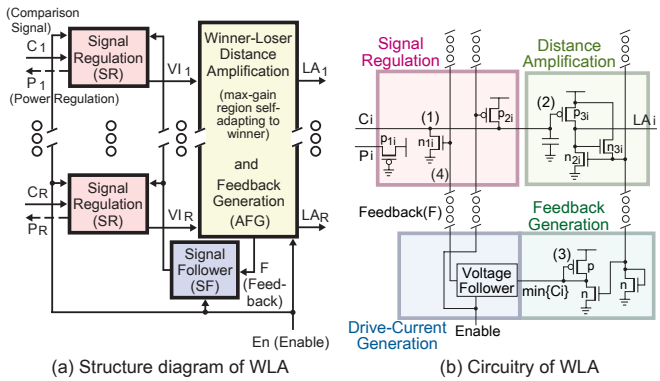


Figure 7: Winner line-up amplifier (WLA) (a) Structure diagram, (b) Circuitry of WLA with self-adapting maximum-gain region, following automatically the winner-row output C_{win} and thus eliminating the inefficient possibilities of under- or over-regulation.

in detail with Fig. 7.

First, the structure diagram of the winner-line-up amplifier (WLA) is shown in Fig. 7 (a). The WLA consists consequently of signal-regulation (SR) units for each row and a common distance-amplification/feedback-generation (AFG) unit. The feedback (F) controls the SR-units in such a way, that the generated, intermediate signal VI_{WIN} of the winner row is just within the narrow maximum-gain region of the distance amplifier in the AFG-unit. The signal follower provides the necessary high driving current for scaling to a large number of reference patterns R. We improved the WLA circuit proposed previously in [8] so as to obtain a large regulation range for feedback stabilization and relatively low power dissipation. The new WLA achieves this larger regulation range for feedback stabilization and eliminates the inefficient possibilities of under- or over-regulation by a maximum-gain region which self-adapts to the winner input C_{win}. Low power dissipation is achieved by an individual power regulation from the signal-regulation units for each input-signal source.

Fig. 7 (b) shows a circuit, which implements the new WLA according to Fig. 7 (a) in CMOS technology. The transistor-count is only 6 transistors per row, that is, O(R) complexity. A modified version of the fast minimum circuit proposed by Opris et al [9] is applied for combined feedback generation and distance amplification. The minimum function is used in the feedback loop and an intermediate node in each row circuitry is used for the distance-amplified WLA-output LA_i.

Distance amplification and self-adaptation of the maximum-gain region work as follows: Since the winner-row's WC-output C_{win} is lowest, transistor p_{3win} has the largest current-source capability, which must be balanced by the current-sink capability of transistor n_{2win}. Thus the gate voltage F_a of n_{2win}, common to all rows, has to rise appropriately and is controlled by the winner row. This in turn is only possible, if the gate voltage of the source follower n_{3win}, being also the output voltage LA_{win}, rises highest. The mechanism works independent of the absolute value of C_{win} and provides the self-adaptability of the maximum-gain region. A gain of about 20-50 over a wide range of absolute C_{win} input voltages is thus achieved. The voltage follower in Fig. 7 (b) is equivalent to the signal followers in Fig. 7 (a) and provides a sufficient driving current for scalability to large row numbers, which are necessary especially for codebook-based data-compression systems.

The WTA-circuit implemented in the test chip is depicted in Fig. 8. It is of O(R) complexity and needs just 17 transistors

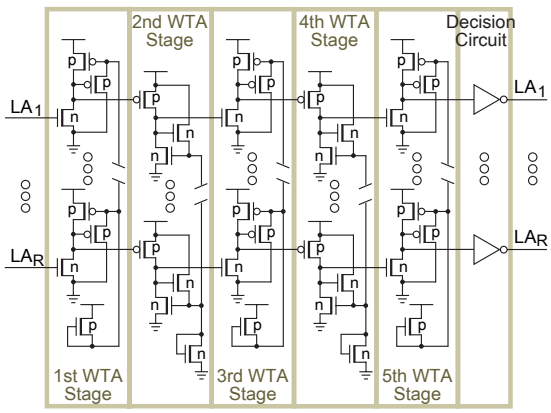


Figure 8: Winner-take-all (WTA) circuit with 17 transistors per row of the associative memory as used for the test chip.

per row. In the first design, we used 3 stages of the common-source WTA-configuration proposed by Lazzaro et al. [10], which amplify winner-loser distances by voltage-current-voltage transformations. In order to reduce the negative effects form fabrication induced miss-match of corresponding transistors in different rows and to improve the reliability for large winner-input distances, we adopt 5 stages of the common-source WTA-configuration. In the 1st stage, the current for the winner row is highest, because it has the largest WLA-output voltage. This highest current is then transformed into the lowest output-voltage of the 1st stage, while the output voltages of all other rows are substantially suppressed. The intermediate stages perform a similar voltage-current-voltage transformation and a further amplification of the winner-loser differences. The winner voltage is again lowest after the 5th stage. The final decision circuit consists of inverters with an adjusted switching threshold. It generates a "1" for the winner row and a "0" for each loser row. In this WTA-circuit, a gain of about 5 - 20 over per 1 stage is achievable.

2.2. Bank-Type Associative Memory Architecture in Large Reference-Pattern Space

The proposed bank-type associative memory architecture is shown for the case of 4 banks in Fig. 9. This system has 4 local winner-search units, implemented as banks which apply the above described fully-parallel architecture, and a global digital minimum-distance-winner selection circuit. Each local-winner is decided by fully-parallel minimum distance search in the banks in parallel. In addition to the associative memory core, each bank has a priority encoder (PE) and a circuit for digital-distance calculation of the local winner. The minimum-distance-winner selection circuit determines the global winner among the local-winners by digital calculation in a tournament-selection way and outputs the global winner's bank number as well as bank-internal address. With this bank-type approach our fully-parallel associative memory architecture can be applied to search problems in an in principle infinite space of reference patterns. For example, in the application case of code-book based vector quantization for video compression a typical code-book size is 1024 reference patterns. This could be realized with an 8-bank structure and 128 reference patterns per bank. Local winner search in each bank and global winner selection circuit could be pipelined, so that the search throughput would be determined only by the local search time of a single bank.

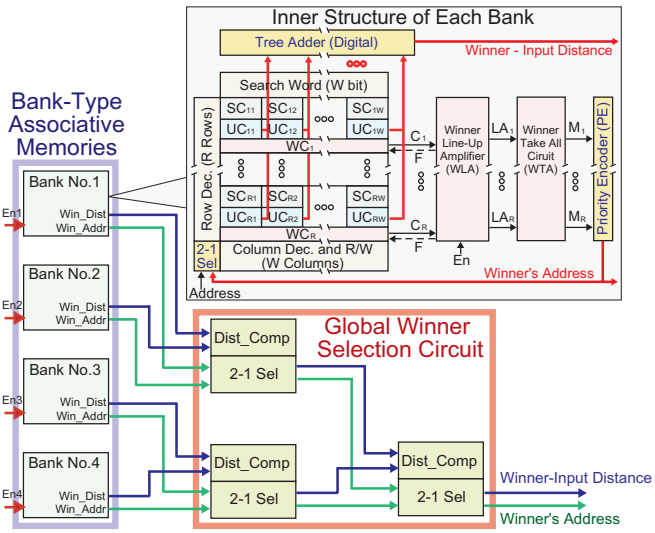


Figure 9: Bank-type associative memory architecture with fully parallel search in each bank and global winner determination by tournament search.

2.3. Chip-fabrication and Measurement Results

The Hamming-distance test chip is designed in 0.6μm CMOS with 3-metals and contains 32 reference words with 768 bit binaries (Fig. 5). Design area is 9.75mm^2 and a high performance of < 70nsec minimum distance search at low-power dissipation of 43mW are achieved. The Manhattan-distance test chip was designed in 0.35μm CMOS with 3-metal layers and contains 128 reference words with 16 binaries each 5-bit long. Fig. 6 (a) shows the photomicrograph of the fabricated Manhattan-distance test chip. Fig. 6 (b) depicts the measured average nearest-match times of this chip as a function of the distance between winner and input-data word. The data for winner to nearest-loser distances of 1 and 10 bit are plotted. Some of the chosen row combinations of winner and nearest

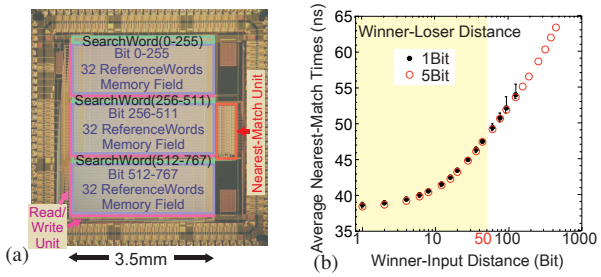


Figure 10: Minimum Hamming-distance-search associative memory. (a) chip photo (b) measured average search times

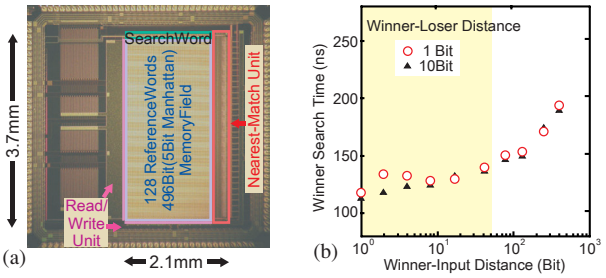


Figure 11: Minimum Manhattan-distance-search associative memory. (a) chip photo (b) measured average search times

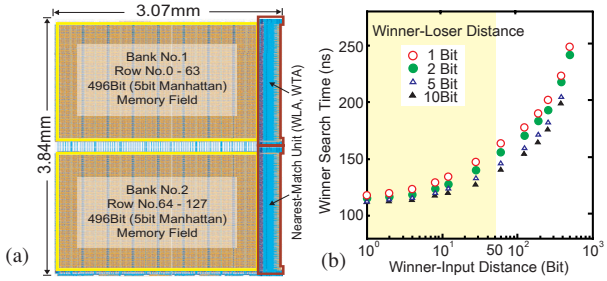


Figure12 : 2-Bank minimun Manhattan-distance search associative memory. (a) chip layout (b) simulated average search times

Table 1: Performance data of designed associative memory test chips.

Distance Measure	Hamming	Manhattan (5 bit)
Memory Field	32 x 768	128 x 80
Technology	0.6µm CMOS	0.35µm CMOS
Area	9.11 mm^2	8.6 mm^2
Search Range	0 - 400 bit	0 - 480 bit
Winner-Search Time (Measured)	< 70 nsec	< 190 nsec
Performance	1.34 TOPS	160 GOPS
Power Dissipation	43 mW	91 mW
Supply Voltage	3.3V	3.3V

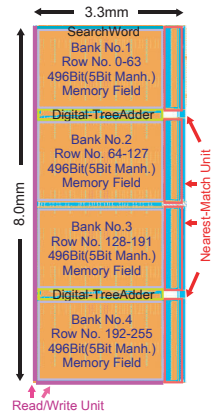


Figure 13: Layout image of the 4-bank, 256 reference-pattern Manhattan-distance- search memory.

Table 2: Characteristics of the bank-type Manhattan-distance associative memories.

Distance Measure	Manhattan (5 bit)	
	2-Bank	4-Bank
Reference Number	128 (64 x 2)	256 (64 x 4)
Design Area	11.8mm^2	26.5mm^2
Search Unit Area	0.99mm^2	1.97mm^2
Search Range	0 - 496bit	0 - 496bit
Winner-Search Time (Simulation)	< 260nsec	< 280nsec
Power Dissipation (Simulation)	< 330mW	< 640mW
Performance	128 GOPS	229 GOPS
Technology	0.35µm 3-metal CMOS	0.35µm 3-metal CMOS
Supply Voltage	3.3V	3.3V

loser delivered unreliable match results for large winner-input distance. However, this causes no practical problem because vector-quantization (VQ) simulations of real images confirmed that almost all winner-input distances are less than 50bit. In the practical case with optimized codebook winner patterns with larger winner-input distance are in general expected to be very seldom. Therefore, the measured performance of the designed test-chip is already sufficient for VQ application with a nearest match time < 140nsec. Taking into account that the area for the input-pattern circuit remains the same, we extrapolate an area of about 17.2mm^2 and a power-dissipation of about 180mW for a nearest Manhattan-distance-search memory with 256 reference patterns in 0.35µm CMOS technology. If we furthermore extrapolate the test-chip data to a state-of-the-art 0.13µm CMOS technology with 1.2V power-supply, we expect an integration area of about 6.4 mm^2 and a power dissipation of about 71.7mW. Table 1 shows the data of fabricated test chips for minimum Hamming/Manhattan distance search.

Multi-bank associative memories have been also designed in 0.35µm CMOS technology. Fig. 7 (a) shows the layout of a 2-bank associative memory for minimum Manhattan-distance search with 128 reference pattern number. Fig. 7 (b) depicts the simulated average nearest-match times of this layout, indicating that high-speed search time can be expected. The layout of a 4-bank associative memory with 256 reference patterns is shown in Fig. 8 and the photomicrograph of the fabricated chip is shown in Fig. 9. Table 2 summarizes performance data of designed 2 and 4 bank associative memories. In addition to the scalability of the bank number N, the introduction of a bank-selective activation methodology can reduce the power dissipation of the whole chip. This is in particular useful if the reference-pattern space can be categorized, so that the bank (or banks) which must contain the winner can be identified in a preprocessing step. Consequently, only 1 bank has to be activated for local winner search in the best case, reducing the power dissipation by approximately a factor 1/N.

3. Conclusion

Associative memory architecture for fully-parallel minimum distance search is proposed and test chips are designed in 0.6µm (Hamming) and in 0.35µm (Manhattan) CMOS technologies. The 9.75mm^2 Hamming test-chip with 32 reference patterns and 768 equivalent bit per pattern, has a performance of < 70nsec nearest-match time, equivalent to a 32bit computer with 150GOPS/mm^2, at a power dissipation of 43mW. The 8.6mm^2 Manhattan test-chip with 128 reference patterns and 496 equivalent bit per pattern, has a performance of < 190nsec nearest-match time, equivalent to a 32bit computer with 20GOPS/mm^2, at a power dissipation of 91mW. These data are sufficient for application in high-performance mobile real-time systems such as systems for image compression by vector-quantization.

Moreover, a bank-type associative memory architecture for fully-parallel minimum distance search is presented and verified by test chips in 0.35µm CMOS technology. The proposed architecture extends the possibility of fully-parallel nearest-match search to an in principle infinite space of reference patterns. Designed 1-, 2- and 4-bank test chips in 0.35µm CMOS verify nearest-match times below 280nsec, a performance between 120GOPS and 230GOPS, and a power dissipation between 90mW and 150mW per bank. For search problems with categorizable reference-data space the power dissipation can be reduced to the value for one bank in the best case. These data are sufficient for application in high-performance mobile real-time systems such as image-compression systems by vector-quantization.

4. Future Plan

Although search time and power dissipation are already very competitive in comparison to other associative-memory solutions, we are planning to further improve the performance of the WLA circuit with a current-comparator-based structure. Search times below 100ns per bank and at the same time a power dissipation below 100mW are expected to be possible. Since a further very important distance measure, the Euclid distance, is very popular in many high-level architectures for realizing artificial intelligent systems, we plan also to extend our Manhattan-distance-search architecture to enable nearest Euclid-distance search.

Acknowledgment
The test-chips have been fabricated in the chip fabrication program of VDEC, the Univ. of Tokyo with the collaboration by Rohm Co. and Toppan Printing Co.

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Associative-Memory-Based Systems with Recognition and Learning Capability

～Automatic Reference-Pattern Learning and Optimization～

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and Yoshinori Shirakawa(Graduate School of Advanced Sciences of Matter, M1)

1. Research Target

Pattern recognition and learning are basic functions, which are needed to build artificial systems with capabilities similar to the human brain. Their effective implementation in integrated circuits is therefore of great technical importance. Among the methods for achieving the pattern recognition and the learning functions, having been proposed so far, the neural-network approach is most widely used. However, the performance progress of hardware that uses neural-networks is much slower than expected initially. Because of this difficult situation a new method that includes the memory element, missing up to now, in a power-efficient LSI hardware is urgently needed.

Presently, we are developing a new associative-memory architecture which achieves small area and high nearest-match speed [1-3]. The proposed architecture can search the reference pattern of minimum distance to the input pattern at high speed for different distance measures. Therefore, it is expected that this small-area and high-speed associative memory becomes the basis for a new method to construct systems with recognition and the learning capability. Moreover, there is the advantage that it can be easily integrated by the use of present CMOS technology.

Here we report 2 new associative-memory-based automatic-learning architectures for artificial intelligence systems that have recognition and learning capability. The developed associative memory that we have developed is used to imitate the long-term and the short-term memory of the human brain(Fig. 1) and only a simple adder and subtractor for learning the optimized reference patterns.

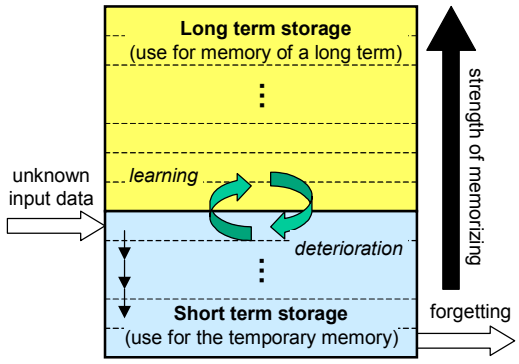

Fig. 1: Learning concept based on a short/long term memory.

2. Learning Concepts

2.1. Short/Long Term Storage Concept

A memory-based learning system can achieve higher learning efficiency than a neural-network, for which a complicated training is necessary at the beginning to enable the recognition of new data. For a memory-based method, the training which we call “supervised learning” corresponds only to writing of the new data into the memory. The proposed learning algorithm, explained in the following, can furthermore automatically learn input data according to the frequency of their appearance, a learning mode, which we call “unsupervised learning”.

The basic underlying concept of our proposal tries to model the short/long term storage of the human brain. Therefore, the reference patterns of the associative memory are classified into two areas. One is a short-term storage area where new information is temporarily memorized. The other is a long-term storage area where a reference pattern can be memorized for a longer time without receiving the influence of the constantly changing input patterns.

Fig.2 shows the flow chart of the associative-memory-based recognition and the learning algorithm. The proposed algorithm uses a “rank” for each reference pattern of the associative memory as an index. The refer-

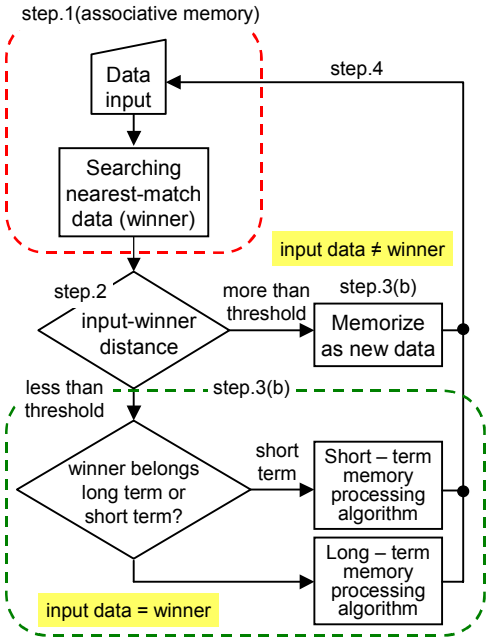

Fig. 2: Flow chart of the pattern-learning algorithm based on short/long-term memory.

ence patterns are classified into the long-term and the short-term memory according to their rank. Important specifying features of the algorithm are the process for changing the rank of a pattern and the method for pattern transition between short and long-term memory.

Details of the proposed algorithm are as follows.

Step1. The associative memory searches for the pattern, which is the nearest-match (winner) to the input pattern among the reference patterns.

Step2. The distance "D" between input pattern and winner-pattern is calculated.

Step3(a). Input pattern and winner-pattern are considered to be the same in case of "D<threshold". In this case, the rank of the reference pattern that became the winner is raised. The rank advancement is decided based on the previous rank of the winner. When the winner belongs to the long-term memory, the advancement becomes J_L. And, if the winner is in the short-term memory, the advancement becomes J_S (J_L<J_S). Each of the patterns of rank between the old and the new winner rank are reduced in rank by one. The transition between short and long-term memory occurs by these changes in rank.

Step3(b). In the case of "D≥threshold", the system considers input and winner patterns to be different, and inserts the winner pattern at the top rank of the short-term memory. The rank of each of the other reference patterns that exist in the short-term memory is moved down by one, and the reference pattern with the lowest rank is erased and forgotten.

Step4. Return to waiting status for new input data. Whenever input data is given to the system, processing from step 1 to step 3 is repeated.

The user of the proposed algorithm has to properly decide the number of pattern entries in the short-term and long-term memory (N_S and N_L) according to the application.

2.2. Learning the Optimized Reference Patterns Concept

The algorithm proposed here needs only a simple adder and subtractor for learning the optimized reference patterns. Furthermore, an optimum threshold value for highly reliable recognition is learned in addition. Fig.3 shows the processing flow of the proposed algorithm, which is explained in the following sections in detail.

(1)Reference pattern learning

The optimal reference pattern for the recognition process is located in the center of the input-pattern distribution which represents a certain object. However it is difficult to identify this optimal reference pattern in online recognition, where input patterns are inputted continuously. We proposed to use the center of a fixed number N of recently recognized input patterns, and to continuously optimize each of the reference patterns after it has been recognized N times. For this purpose the following processing steps are carried out. When an input pattern is inputted, the Manhattan distance D between input and every reference pattern is calculated according to (Eqn.(1)).

$$D_i = \sum_{j=1}^{C} | \mathbf{Y}_j - \mathbf{X}_{ij} | \quad (1)$$

The nearest reference pattern to the input pattern, i.e. the winner which has the smallest D is determined during the winner-searching step (Fig.3(b)). It is assumed here, that the winner-reference pattern became the winner for the k^{th} time. If the Manhattan distance $D_{w,k}$ between winner $\mathbf{X}_w$ and input pattern $\mathbf{Y}_{w,k}$ is smaller than or equall to the threshold value Dth_w, the difference vector $\mathbf{G}_{w,k}$ between input pat tern $\mathbf{Y}_{w,k}$ and winner $\mathbf{X}_w$ is derived from Eqn.(2).

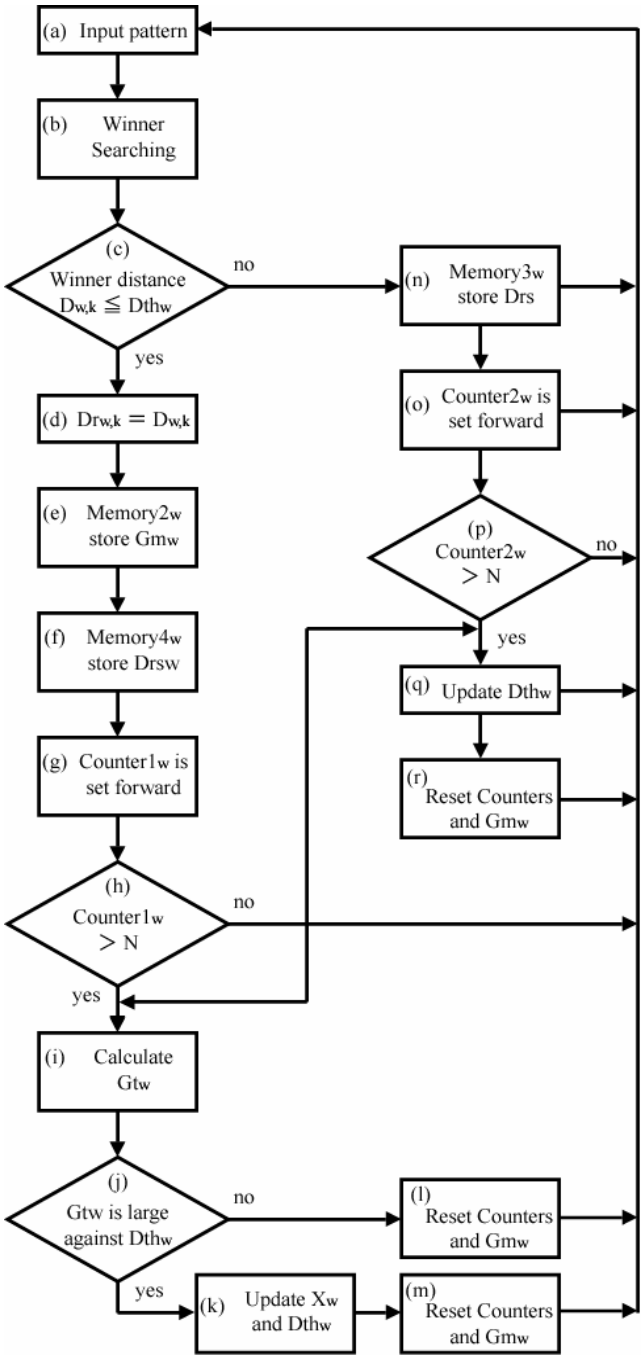

Fig. 3: Flow chart of the algorithm for reference-pattern and recognition-threshold optimization.

$$\mathbf{G}_{w,k} = \mathbf{Y}_{w,k} - \mathbf{X}_w \quad (2)$$

$\mathbf{G}_{w,k}$ is then added as shown in Eqn.(3) to the variable $\mathbf{G}_m$, memorized in Memory1$_w$ (Fig.3(e)).Step (f) addresses the threshold update, which is described in the next section 2.2.(2). *Counter1*$_w$ of the winner pattern is their forward (Fig.3(g)) by 1 to the next value k+1.

$$\mathbf{Gm}_{w,k} = \mathbf{Gm}_w + \mathbf{G}_{w,k} \quad (3)$$

In case that k>N is true, the winner pattern $\mathbf{X}_w$ is optimized (Fig.3(k)), according to Eqn.(4), if additionally a control condition (Fig.3(j)) is fulfilled, which we describe in section 2.2.(3).

$$\mathbf{X}_w = \mathbf{X}_w + \mathbf{Gm}_w / N \quad (4)$$

(2)Threshold value learning

A threshold value is used to recognize input patterns. Namely, if the winner distance $D_{w,k}$ is larger than the threshold Dth_w, the winner pattern is considered to be different from the reference pattern, that means it is considered as not recognized. Besides its function for a recognition condition the threshold value is also used for selecting the input patterns which are included in the reference-pattern update, in order to prevent local solutions. Therefore threshold value learning, that is learning of the size of the recognition region, is also important.

For threshold value learning it is necessary to distinguish whether the input pattern is inside or outside of the threshold region. If all input patterns for which a given reference pattern is determined as the winner are inside the region determined by the threshold value, this threshold value is effective for the recognition purpose. On the other hand, if winner input patterns are outside of the region determined by the threshold, it is required to extend the recognition region, or in other words to use a larger threshold value. Threshold value learning is carried out by 2 factors. The 1st factor is the rate of the number of input patterns which are inside or outside threshold value Dth_w. This factor determines whether a threshold value Dth_w will be made smaller or larger. The 2nd factor is the gap between the winner distance Dth_w and the corresponding threshold value Dth_w. This 2nd factor decides how much to reduce or increase the threshold when updating occurs. For our threshold learning algorithm, we prepare the additional counter *Counter2*$_i$, which counts for each reference pattern i the number of presented winner-input patterns outside (>Dth_w) of the threshold-value region (Fig.3(o)). The winner-input pattern number inside the threshold-value region is already determined for reference pattern learning (Fig.3(h)) by *Counter1*$_w$.

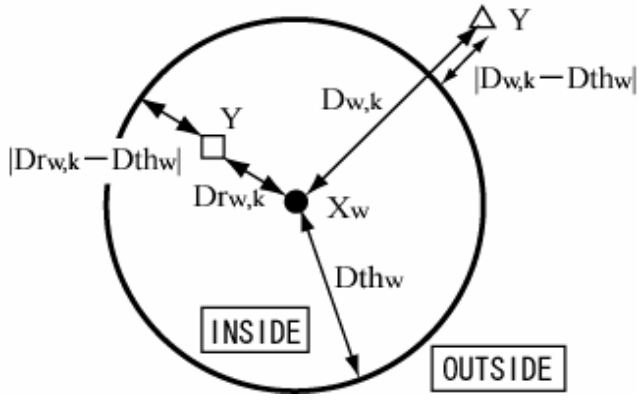

Fig. 4: The location of winner, input pattern and threshold value.

Especially, we define a winner which lies inside the threshold-value region as a recognition winner and its winner distance $D_{w,k}$ as a recognition-winner distance $Dr_{w,k}$ (Fig.4).

When *Counter1*$_w$ is set forward, we calculate the gap between the recognition-winner distance $Dr_{w,k}$ and the threshold value Dth_w, and add it to the sum of recognition-winner gaps memorize in Drs_w as Eqn.(5). On the other hand, when a winner distance $D_{w,k}$ is larger than the threshold value Dth_w, *Counter2*$_w$ is set forward. The sum of the gaps between the non-recognization winner distances $D_{w,k}$ and the threshold value Dth_w is memorized in Ds_w as Eqn.(6).

$$Drs_w = Drs_w + | Dr_{w,k} - Dth_w | \quad (5)$$

$$Ds_w = Ds_w + | D_{w,k} - Dth_w | \quad (6)$$

When the value of either *Counter1*$_w$ or *Counter2*$_w$ becomes larger than the fixed number N, the threshold learning starts (Fig.3(h),(p)). In the case of *Counter1*$_w$ =N and *Counter2*$_w$ =0, the threshold value Dth_w is decreased, because all input patterns were inside the recognition region of threshold Dth_w. For this purpose we calculate the average recognition-winner gap Drg_w(=Drs_w/N).

On the basis of Drg_w the updating-magnitude of the threshold value Dth_w is decided. For reflecting the fact that our algorithm includes only a small fraction of the complete input-pattern space, the magnitude of the decrease Dc_w is randomized by a triangle distribution Eqn.(7) also shown in the plot of Fig.5.

$$p_T(Dc_w) = -2Dc_w / (Drg_w + 1)^2 + 2/(Drg_w + 1) \quad (7)$$

On the other hand, the threshold value Dth_w is increased, when the number of winner-input patterns inside and outside the recognition region are large i.e. when (*Counter1*$_w$+*Counter2*$_w$) as well as *Counter2*$_w$ are large. For this purpose we calculate the average non-recognition-winner gap Dg_w(=Ds_w/N). The magnitude of the increase Dc_w is again randomized by Eqn.(7), but now Drg_w is replaced by Dg_w. After completion of each learning step a reset operation is carried out for *Counter1*$_w$,

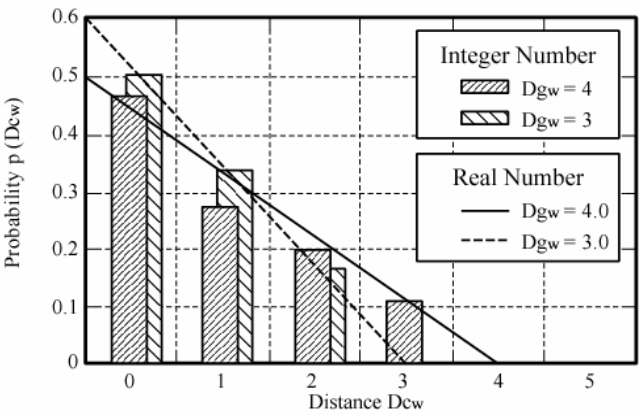

Fig. 5: The triangle distribution for updating threshold value.

Counter2$_w$, Drs$_w$, Ds$_w$,Drg$_w$ and Dg$_w$.

(3)Learning control

Both reference pattern and threshold learning are not performed, when the normalized Manhattan distance Gt$_w$ between **Gm**$_w$=(Gm$_{w,1}$, Gm$_{w,2}$, ... , Gm$_{w,j}$, ... , Gm$_{w,C}$) and the zero vector, calculated according to Eqn.(8)small against the threshold.

Because of the smallness of Gt$_w$ it can be concluded that used reference pattern and threshold values are already sufficiently good, so that an update is not necessary.

$$Gt_w = \frac{1}{N}\sum_{j=1}^{C} | \mathbf{Gm}_{w,j} | \qquad (8)$$

2. 3. Simulation and Result

2. 3. 1. Short/Long Term Storage Simulation

A simulator was written in C programming language to verify the effectiveness of the proposed learning algorithm. The size of the associative memory for the verification experiments was chosen to allow holding of 30 patterns with 256bit each. The Hamming Distance was selected as the distance measure. The relative sizes of long-term and short-term memory were set at 2:1, which means N_L=20 and N_S=10. The remaining parameters of the learning algorithm were chosen as threshold=10, J_L=6 and J_S=3.

The automatic learning of 20 new character-bit patterns (each 256 bit) was investigated as test problem. These 20 new patterns were presented to the system as inputs randomly. The learning task was additionally complicated by also presenting noise patterns as inputs, where each of the 256 bits was set at random to 1 or 0. These noise patterns were arbitrarily intermixed with the 20 new character-bit patterns at the same rate (50% noise patterns, 50% new character-bit patterns).

Fig.6 depicts the simulation result for the number of learned patterns among the 20 new character-bit patterns as a function of the total number of presented input patterns. The blue line shows the result without short/long-term storage concept, where an input pattern, which is identified as new, is stored at the topmost rank of the associative memory. Due to the intermixed noise patterns, the new character-bit patterns cannot be learned efficiently. The number of learned patterns oscillates around 10 due to the noise intermixture rate of 50%. The red line shows the result with the short/long term storage concept, which completes the learning of all 20 new character-bit patterns after about 1800 input cycles, even under the presence of noise-input patterns. The short/long-term memory concept and the transition mechanism from short-term to long-term memory have the effect that noise patterns are unable to advance from the short-term to the long-term memory. These concepts are thus the key to efficient memory-based hardware for automatic learning.

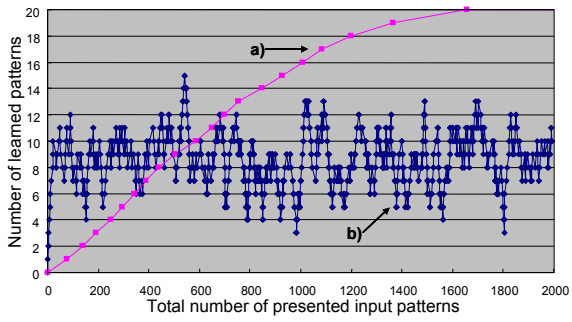

Fig . 6: Simulation result.
a) Learning algorithm based on short/long term storage concept.
b) Without short/long term storage (unknown data is inserted at the top rank).

Fig.7 shows the architecture of the test chip, which is divided roughly into the associative memory block, the rank-processing circuit and the automatic learning control circuit. A test chip of the described architecture was designed in 0.35um CMOS technology. (Fig.8 The automatic learning circuit within the test chip receives the result of the nearest-match search from the associative memory, including the input-winner distance (D), and generates the signals for the rank-processing circuit and the learning signals for the associative memory within one clock cycle. Table.1 shows the parameter table of the designed test chip. The associative memory finishes the nearest-match search in 250nsec or less, and the automatic learning circuit operates at a maximum operation frequency of 166MHz (gate level simulation).

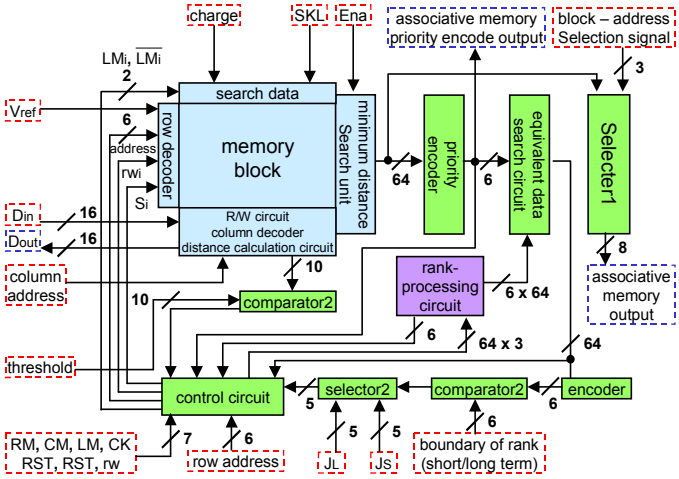

Fig. 7: Associative-memory-based automatic pattern learning architecture, with 64 patterns. Long/short-term-memory size, parameters J_L, J_S and the threshold in the algorithm can be set externally.

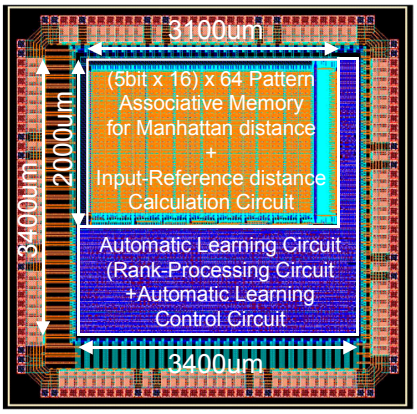

Fig. 8: Layout of test chip.

2. 3. 2. Learning the Optimized Reference Patterns Simulation

As the performance measure for the proposed reference pattern-learning algorithm, we chose the error rate α_w [4]. When this parameter is near to "0", reference pattern is optimized. Figures 9 and 10 show the simulated reference-pattern learning of the proposed algorithm in comparison to the k-means algorithm for Gaussian and Homogeneous input-pattern distributions, respectively. From Fig.9 it can be seen, that both algorithms achieve the same learning performance in case of a Gaussian input-pattern distribution for a given parameter set(N=8 for the proposed algorithm, ε=0.5 for k-means). This is remarkable, because the proposed algorithm applies the less complex Manhattan distance and not the Euclid distance as the k-means algorithm. In addition, if the input-pattern distribution is homogeneous, the k-means algorithm with the same ε converges less good than the proposed algorithm as shown in Fig.5. To achieve good convergence the ε-value has to be change (to ε=0.1) for the k-means algorithm, while α parameter change is not necessary for the proposed algorithm. In consequence, the proposed algorithm can be expected to perform better than k-means for a general unknown input-pattern distribution.

Table. 1: Characteristics of the designed test chip.

Distance Measure	Manhattan Distance (5bit x 16)
Reference Patterns Short Term Storage Long Term Storage	64 24 (Default, Variable) 40 (Default, Variable)
Nearest-Match Range	0 to 496
Technology	0.35um, 2-poly 3-metal, CMOS
Supply Voltage	3.3V
Number of Transistors	402,768
Design Area Associative Memory Automatic Learning Circuit	11.04mm^2 6.2mm^2 4.84mm^2
Automatic Learning Algorithm Processing Time	< 290nsec (search time 250nsec)
Automatic Learning Circuit Max Operation Frequency	166MHz (gate level simulation)

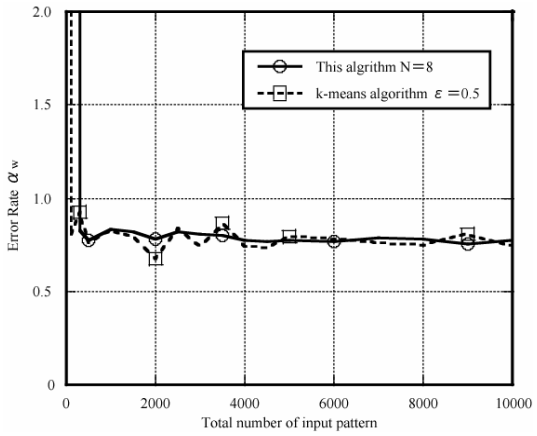

Fig. 9: Performance of the proposed algorithm in comparison to the k-means algorithm for a Gaussian input-pattern distribution.

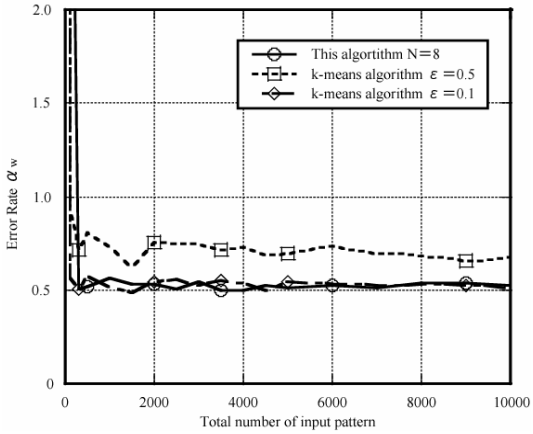

Fig. 10: Performance of the proposed algorithm in comparison to the k-means algorithm for a Homogeneous input-pattern distribution.

The largest advantage of the proposed algorithm is its relatively easy VLSI implementation with a fully-parallel associative memory for Manhattan-distance search. Due to the Euclid distance, the k-means algorithm requires a much complex hardware, which is also much slower. Fig.11 shows the block diagram of the complete VLSI architecture for the case of reference patterns with integer components. A more detailed diagram of the learning-circuit architecture is depicted in Fig.12.

Besides the associative memory, the functional units of comparator, memory, counter, subtractor, adder, divider, random-number generator, probability-distribution memory, REG (register) and switch are required.

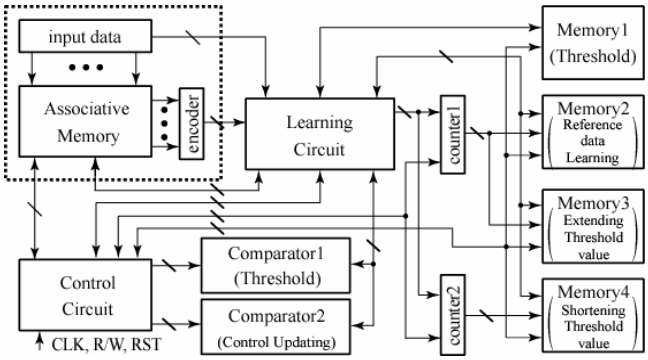

Fig. 11: The associative memory with learning function architecture

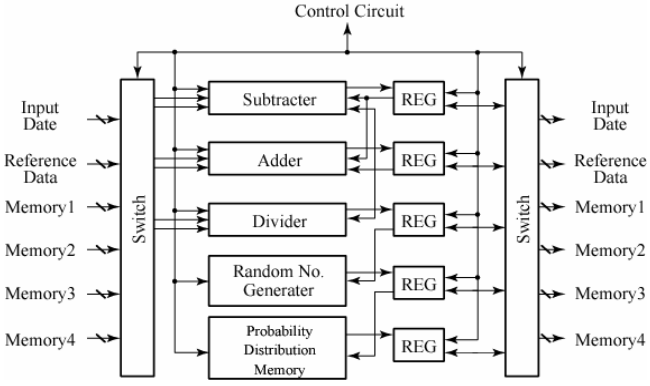

Fig. 12: The learning circuit architecture.

The specific construction and function of random number generator and probability-distribution memory, used for threshold value learning, are briefly explained. The threshold-updating value is selected with this random number from a codebook memory (see Fig.13) which stores the designed probability distribution.

For example, if the number “50” is selected by the random-number generator from the specified range "0" to "100", the threshold-updating value Dc_w=1 is selected from the probability distribution memory
(see Fig.13}). In this way, it is easy to implement the threshold-learning part of the proposed algorithm in hardware.

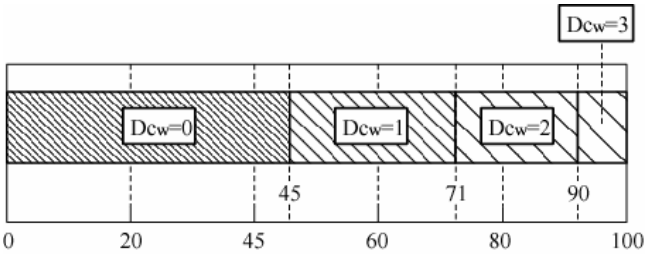

Fig. 13: Contents for random number generation in the range “0” to “100”.

3. Conclusion

We have proposed algorithms and VLSI architectures for automatic learning and optimization of reference patterns. These architectures are intended for application in associative-memory-based pattern-recognition systems. The VLSI architecture for part of the algorithms has also been verified by design and fabrication of a test chip in 0.35μm CMOS technology. According to the test-chip simulation, the basic learning cycle can be completed very fast in about 300ns, which is sufficient for probably all conceivable application. Although the proposed algorithms use only the Manhattan distance, the pattern-learning performance could be shown to be as good as the conventional k-means algorithms, based on the more complicated Euclid distance, for which a good fully-parallel hardware implementation is not known.

4. Future Plan

The next verification step of our architecture for automatic reference-pattern learning and optimization will a test-chip design for the complete proposed architecture including the pattern-optimization part. The test chip will then be fabricated and its performance will be evaluated to experimentally verify the feasibility of our architectures.

We are also developing the full-scale real application of moving-object detection and recognition, where we plan to evaluate the system-level suitability and performance of our automatic reference-pattern-learning architecture.

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[2] H. J. Mattausch et al. , “Fully-parallel pattern-matching engine with dynamic adaptability to Hamming or Manhattan distance”, 2002 Symposium on VLSI Circuit Dig. of Tech. Papers, pp.252-255, 2002.

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5. Published Papers and Patents

① Proceedings

1.Y. Shirakawa, H.J. Mattausch and T. Koide, “Reference-Pattern Learning and Optimization from an Input-Pattern Stream for Associative-Memory-Based Pattern-Recognition Systems”, 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS’04), in press, 2004.

2.Y. Shirakawa, M. Mizokami, H. J. Mattausch and T. Koide, “Automatic Pattern-Learning Architecture Based on Associative Memory and Short/Long Term Storage Concept”, 2004 Solid State Devices and Materials International Conference (SSDM’04), submitted, 2004.

②Patents

1. H.J. Mattausch, T. Koide, M. Mizokami, "Recognition and Learning Method of Reference Data and Pattern-Recognition System", Japanese Patent Application 2003-434596 (2003.12.26)
2. H.J. Mattausch, T. Koide, Y. Shirakawa, "Method for Reference-Data Optimization and Pattern-Recognition System", Japanese Patent Application 2004-053433 (2004.2.27)
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2. M. Mizokami, Y. Yano, M. Honda, H. J. Mattausch and T. Koide, “Performance Evaluation of A Digital-analog Associative Memory Capable of Parallel Processing of Reference Data with Large Pattern Length,” Proceedings of the 2003 IEICE Regional Conference in Central Japan, 101309, pp.283-284, 2002.

Image Processing Front End for Associative Memory-Based Systems

- Hardware-Efficient Low-Power Motion-Picture Segmentation by Pipeline Processing of Tiled Images with Cell-Network -

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Cooperator : Hans Juergen Mattausch (Prof., Research Center for Nanodeivices and Systems, Graduate School of Advanced Sciences of Matter), Takashi Morimoto (Graduate School of Advanced Sciences of Matter, D1), Yohmei Harada (Graduate School of Advanced Sciences of Matter, M2), Hidekazu Adachi (Faculty of Engineering), and Osamu Kiriyama (RCNS Researcher)

1. Research Target

The vision-based intelligent processing for associative memory-based systems with recognition and learning capability, as illustrated in Fig. 1, requires segmentation of objects and feature extraction/modeling for associative memory-based systems. Image segmentation is the extraction process of all objects from natural input images and is the necessary first step of object-oriented image processing such as object recognition or object tracking. For these front-end technologies of image segmentation and future extraction, we are investigating and implimenting new feature extraction and modeling methodologies suitable for associative memory-based systems. Fig. 2 shows a conceptual example of the aimed-at image segmentation and feature extraction systems.

Technologies for image recognition and object tracking are essential in research fields like robot vision and intelligent transport systems. If humanlike recognition of objects in natural complex images becomes possible, a wide range of applications in the industrial, public and private sector will profit. One important application field are hand-held mobile application systems. To realize such systems, 3 requirements have to be attained simultaneously, namely *real-time processing, compact implementation, and low-power dissipation*. Since visual information is generally complex and contains a multitude of informations, it's difficult to achieves these requirements with general purpose hardware like FPGAs, microprocessors or digital signal processors (DSP). A common strategy for reducing the complexity of the task is the extraction of important information (objects) from the natural complex image. To realize this strategy an image-processing function called *image segmentation* is required.

Many image segmentation algorithms have already been proposed [1, 2]. But, nearly all of these algorithms are strongly software-oriented, so they cannot satisfy above 3 requirements simultaneously. In particular, hardware implementation is basically restricted to microprocessor or DSP because of algorithm complexity. Recently, some proposals for special purpose image-segmentation hardware have been made [3, 4]. However, they still have problems, namely with respect to power dissipation and chip size but also segmentation quality, when applied to real-time processing of standard size (e.g. VGA) motion pictures.

The aim of our project in the COE research is to develop a high-speed and high-density image segmentation algorithm and architecture, and the associative memory-based future extraction architecture, using the proposed image segmentation framework for real-time moving pictures, to enable vision-based intelligent processing.

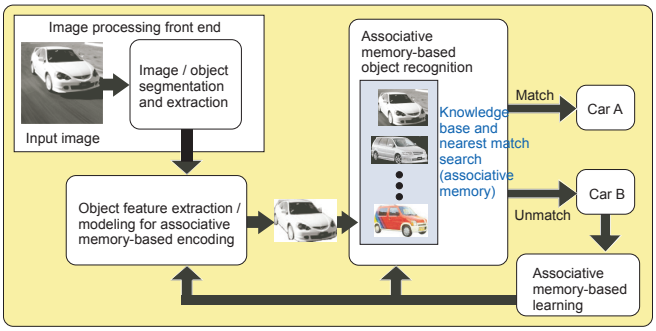

Figure 1: Structure of envisaged associative memory-based systems.

2. Research Results

In this report, we explain the current status of the proposed cell-network-based segmentation architecture, applying a tiled subdivided-image approach (SIA) and a boundary-active-only (BAO) region-growing scheme for low-power mobile applications. A test-chip design of the cell-network core in 0.35um CMOS verifies that real-time VGA-size motion-picture segmentation becomes possible in standard digital CMOS at below 30mW power dissipation.

2.1 Cell-Network-Based Segmentation Architecture

The proposed architecture of a cell-network-based segmentation algorithm [5, 6] has following features: (1) region-growing approach, (2) pixel-based fully-parallel processing,

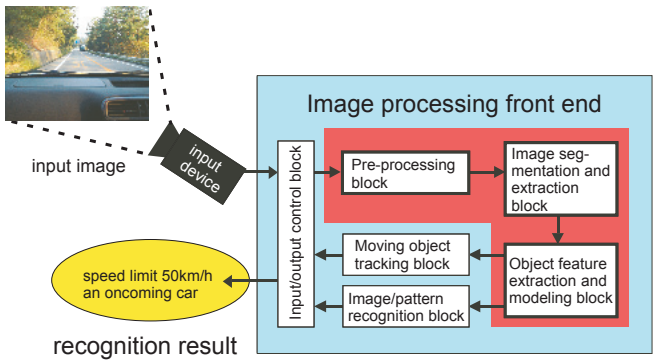

Figure 2: A block diagram of image segmentation and feature extraction for real-time applications.

and (3) gray-scale or color-image segmentation by only changing an initialization step for weight calculation.

Figure 3 shows the outline of the flowchart of the proposed segmentation algorithm. In an initialization phase (a), connection-weights are calculated from luminance (RGB-data for color images) differences between neighboring pixels. Then leader cells, which are the seeds of the subsequent region-growing processes, are determined from calculated connection-weights. In the main phase, self-excitation (b, c) and segment-growing (d, e) are executed for determining the individual segments. During the search phase of self-excitable cells (b), one of the leader cells is selected with a token-passing search. Then the selected leader cell is self-excited (c). In the subsequent region-growing process, excitable cells are determined with a threshold condition for the sum of connection-weights with excited neighbors (d). These excitable cells are then automatically excited (e) in parallel, which leads to a growth of this region. The growing operation is repeated as long as excitable cells exist in the loop (d)-(e). If there are no excitable-cell left, the region of excited cell is labeled as one segment and inhibited (f). The above self-excitation and region-growing phases are repeated until all leader cells are inhibited. Segmentation examples with the described algorithm are shown in Fig. 4.

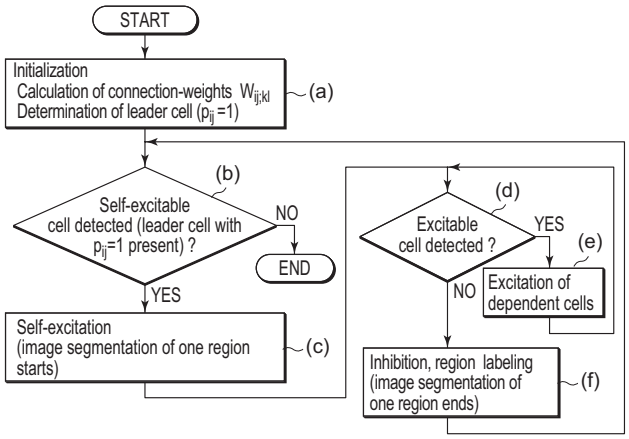

Figure 3: Examples of real image segmentation results for gray-scale (a)-(c) and color (d) images.

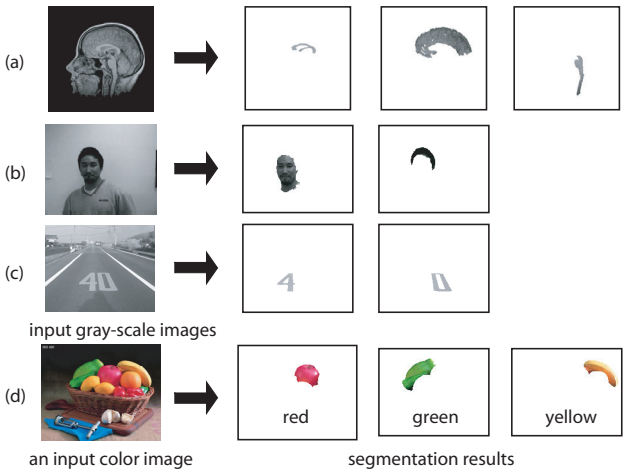

Figure 4: Block diagram of the cell-network-based image segmentation architecture with subdivided-image approach (SIA). The blocks with bold-line are added for SIA implementation.

The proposed cell-network-based VLSI implementation consists of 4 functional blocks (shown in non-bold form in Fig. 5), namely the connection-weight calculation (A), the leader cell selection (B), the image-segmentation cell-network (C) and the segmentation-restore circuit (D). The connection-weight calculation circuit (A) and leader cell selection circuit (B) execute the initialization phase (a). Calculated connection-weights and leader cells are transmitted to the cell-network (C) in column pipeline mode. In the cell-network (see Fig. 6), which consists of cells P_{ij} and connection-weight-register blocks WR_{ij}, the steps (b)-(f) of the algorithm are carried out with pixel-parallel processing. Each active cell P_{ij}, corresponds to a pixel and is a processing element, which determines its current status in each clock cycle from the connection-weights to its excited nearest neighbors. The connection-weights are stored in connection-weight-register blocks WR_{ij}, which are placed between the cells. Finally, segmentation-results are restored by segmentation restore circuit (D).

The active cell P_{ij} consists of decoder, adder/ subtractor, control unit and four 1-bit registers. We have 2-types of P_{ij}

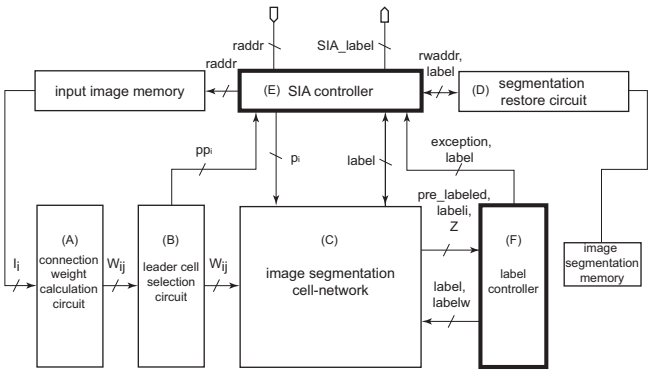

Figure 5: Block diagram of the cell-network-based image segmentation architecture with subdivided-image approach (SIA). The blocks with bold-line are added for SIA implementation.

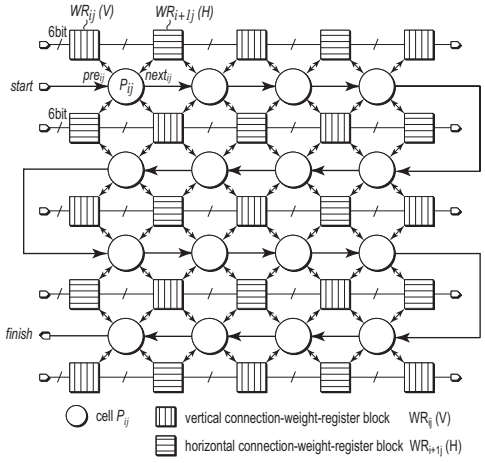

Figure 6: Construction of the cell-network for 4×4 pixels. Vertical and horizontal registers are used for resource-sharing of the connection-weights.

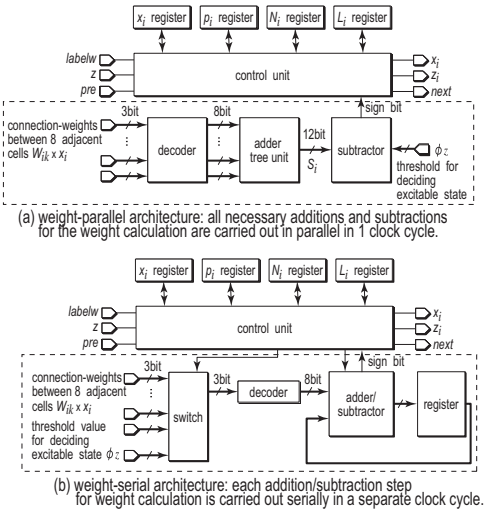

Figure 7: Weight-parallel (a) and weight-serial (b) structure of active cells.

implementations, weight-parallel (WP, Fig. 7a, single clock-cycle solution) and weight-serial (WS, Fig. 7b, multiple clock-cycle solution) for high speed and high density, respectively. The main difference of these two implementations is the processing block for weight calculation surrounded by the dashed lines in Fig.7a, b.

The test-chip reported in [5] has a pixel integration density, PID, of 19.6pixel/mm^2. Based on this test-chip design, we have estimated the possible PID for full-custom weight-parallel and weight-serial cell-network architectures in scaled-down CMOS technologies with 5 metal routing layers. Fig. 8 shows the estimation result at 90nm with a PID of 665pixel/mm^2 and a required chip-size of 116mm^2 (11mm x 11mm) for the QVGA image-size. If more than 5 metal layers are available, even higher pixel densities are possible by introducing dedicated routing layers for VDD and VSS. Since the typical chip-size for the cost-performance market in 2004 is expected at 195mm^2 (14mm x 14mm) from the International Technology Roadmap for Semiconductors (ITRS2002 Update), single-chip implementation of our weight-parallel architecture for QVGA-size image segmentation is predicted possible at the 90nm

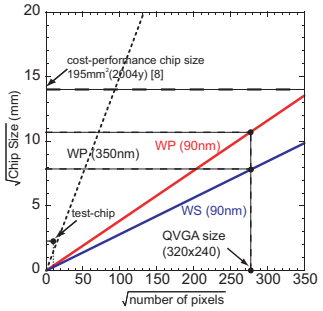

Figure 8: Chip-size estimation for weight-parallel (WP) and weight-serial (WS) architectures at the 90nm technology node with 5 metal layers as a function of the image size.

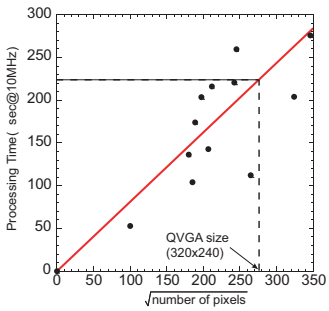

Figure 9: Image segmentation time estimation of WP architecture for larger image sizes at 10MHz clock frequency.

technology node. We have also estimated the processing time by a software simulator for the weight-parallel architecture and tested several natural image samples. The simulated average processing time of the weight-parallel architecture, implemented in the fabricated test-chip, is shown in Fig. 9. Consequently, a real-time, full-color, QVGA-size image segmentation chip in a 90nm CMOS technology with 5 metal layers, should complete the frame segmentation within <250usec, even at a low clock frequency of 10MHz.

2.2 Subdivided-Image Approach (SIA)

The fast segmentation speed of the original architecture, explained in Section 2.1, can be exploited for reduced hardware cost by pipeline-processing of tiled images. The basic concept of this method, which we call *subdivided-image approach (SIA)*, is explained in Fig. 10. Input images are divided into tiles with an overlapped region of 1 row and 1 column. Then, each image tile is processed in sequential order in a correspondingly smaller cell-network. The segment label numbers of the pixels in the overlap region, are reused as *prelabels* for the segmentation of subsequent tiles. As illustrated in Fig. 11, segments extending over several tiles are thus identified without problems. In consequence, SIA avoids the necessity of a large-scale cell-network, which increases with the input image size, and enables compact integration.

The SIA architecture is realized as an extension of our original cell-network-based image segmentation architecture. Additional elements, shown as bold blocks in Fig. 6, are the SIA controller (E) and the label controller (F). Slight modifications of image segmentation cell-network and segmentation restore circuit are also required. The function of this proposed SIA architecture is shortly explained as follows. When the segmentation of a previous tile has finished, the SIA controller assigns the next image tile address *raddr* to input memory. Pixel data are streamed in column-wise and

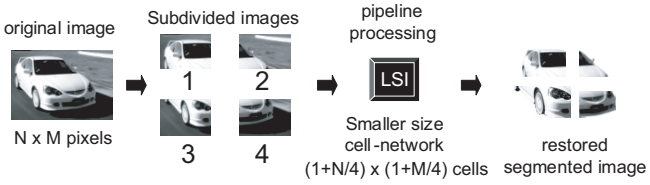

Figure 10: Conceptual diagram of the subdivided-image approach (SIA). Pipelined segmentation of image tiles with a corresponding smaller-size cell-network is applied.

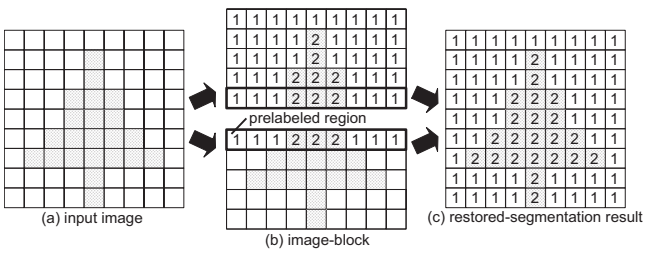

Figure 11: Processing example of the SIA approach. Prelabeled regions at the boundary of the tile enable correct segmentation of regions extending over several tiles.

connection-weights W_{ij} as well as leader cells pp_i are calculated from the luminance (or R, G, B) data I_i and are written into the cell-network in column-parallel pipeline mode. The prelabeled cells in the overlap region (left column and upper row) are forced to become leader cells by the SIA controller. Then tile segmentation is carried out in the cell-network. After completion of the segmentation process the label numbers of overlap row and column with subsequent tiles are stored in the label controller and are transferred to the cell-network for segmentation of the respective tiles. Tile segmentation finishes by storing the segmentation results in the image-segmentation memory with the segmentation restore circuit.

2.3 Low-Power Techniques

The guideline for low-power consumption is to keep all network cells, which are not involved in the growing process of the current segment, in a low-power stand-by mode.

2.3.1 Boundary-Active-Only (BAO) Concept

Since the architecture, described up to now, relies on pixel-based fully-parallel processing, power dissipation increases in proportion to the number of pixels. Without the SIA architecture, the power dissipation of a VGA-size cell-network would be about 1W. For battery-based mobile applications, substantial reduction of the power dissipation is therefore indispensable.

For this purpose, we propose a boundary-active-only (BAO) scheme as a low-power technique which doesn't sacrifice real-time processing. Instead, it effectively exploits the region-growing characteristics of the algorithm, namely that only the boundary cells of the currently grown region have to be in active mode. All other cells may be set to a low-power stand-by mode as conceptually illustrated in Fig. 12. More precisely formulated, a network cell is kept in stand-by mode, if it satisfies one of the 3 following conditions: (1) It is already excited (x_{ij}=1). (2) It has already a segment number (l_{ij}=1). (3) It is not excited and has no segment number, but there are no neighboring cells excited during the previous clock cycle t.

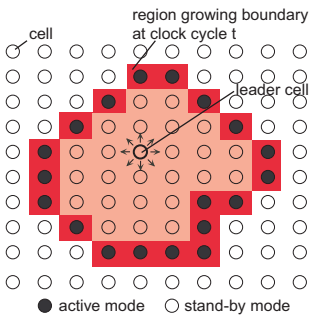

Figure 12: Conceptual diagram of the proposed boundary-active-only (BAO) scheme.

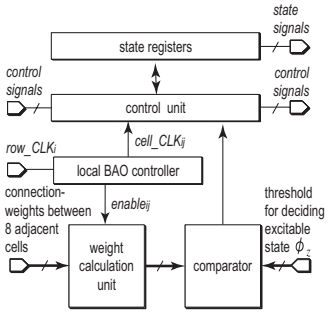

Figure 13: Block diagram of the cell with BAO controller.

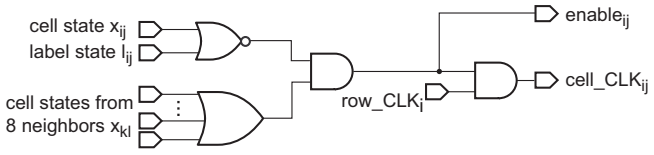

Figure 14: Circuit diagram of BAO controller in each cell for cell-internal power reduction.

2.3.2 Implementation of the BAO Concept

The BAO architecture is implemented with both local and global approaches for power minimization. The local approach is to implement a BAO controller in each cell (see Figs. 13, 14), which examines the 3 stand-by-mode conditions and keeps the cell in stand-by mode, if at least one of these conditions is true. The cells, which satisfy none of the 3 conditions, can be activated by a gated-clock signal (cell_CLK_{ij}). Since the cell-network has long global clock-lines with large capacitances, global clock control is applied as a global approach for efficient power reduction. Figure 15 explains the global BAO implementation, which restricts clock distribution to potentially active network cells in the next clock cycle by boundary detection of the grown region. Detection of the region-growing boundary is no overhead because it is required anyhow for recognizing the region-growing end. The detection is carried out with an OR-function of the state signals of all network cells, indicating whether the respective cells have been included in the currently grown region during the previous clock cycle. Only cell-network rows i, where cells have been included in the grown region, will output a "ZOR_i = 1" signal. The clock controller distributes the clock signal only to the neighboring rows {i-1, i, i+1} of the detected boundary cells in the next clock cycle.

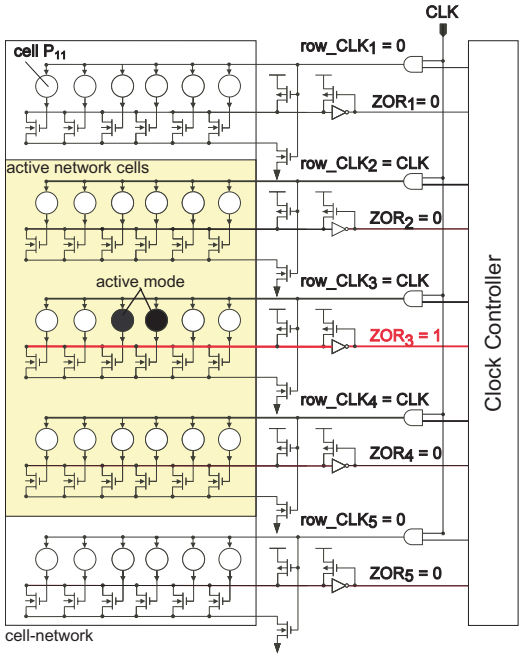

Figure 15: Block diagram of global BAO implementation for power-reduction of clock distribution. Rows i containing region-boundary cells are detected (ZOR_i=1) from the state signals of the row cells. The clock controller distributes the clock only to rows containing boundary cell and their nearest neighbor rows {i-1, i, i+1}.

We have estimated the power-saving potential of the proposed low-power BAO architecture by worst case analog circuit simulation with the HSPICE. Even for the small cell-network size of 10×10 cells more than 75% power-reduction was achieved.

2.4. Designed CMOS Test-Chip Design

Segmentation speed and power dissipation of the pipelined SIA segmentation architecture depend on the number of image tiles. Therefore, we estimated the most suitable tile size for VGA images before starting the test-chip design. Figure 16 shows the estimated power dissipation and image-segmentation time of the SIA architecture for 0.35um CMOS technology at 10MHz clock frequency as a function of the tile number. Obviously the image-segmentation time has a trade off with the number of image tiles and the power-dissipation, so that an optimum cell-network size can be chosen for each target application. For mobile applications with VGA-size video pictures (640×480 pixels), we have chosen following boundary conditions: processing time <8msec (giving some margin with respect to real-time processing) and power dissipation <50mW. The tile size satisfying these conditions is 40×32 pixels. Including the overlap regions a segmentation network with 41×33 cells becomes necessary. The detailed parameter choice for VGA-size image segmentation with the SIA architecture is summarized in Fig. 17.

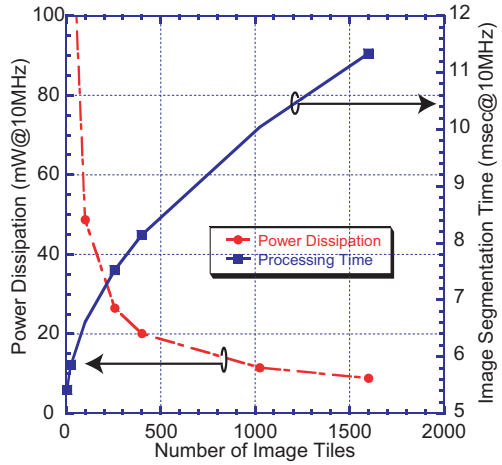

Figure 16: Estimated SIA performance data for VGA size images as a function of tile size (0.35um CMOS with 3-metal layer, 10MHz clock frequency).

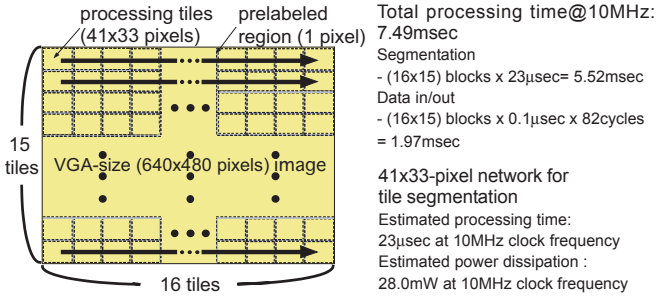

Figure 17: Segmentation of a VGA-size image with subdivided-image pipeline processing. 41×33-pixel sized tiles are processed sequentially by the cell-network with BAO scheme.

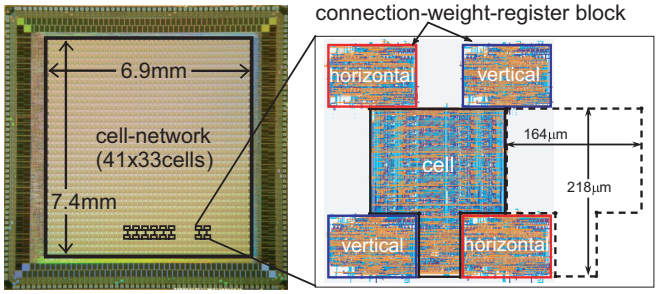

Figure 18: Die photo of the network with BAO including 41×33 cells. It is designed in a 0.35um 3-metal CMOS technology.

Table I: Characteristic data of the designed test-chip.

Technology	0.35µm, 2-Poly 3-Metal CMOS
Cell Architecture	Weight-Parallel (high-speed)[5]
Design Area	6.9mm×7.4mm (41×33 cells)
Supply Voltage	3.3V
Max Clock Frequency	20MHz
Segmentation Time (41×33 pixels)	23µsec@10MHz (Worst Case)
Power Dissipation (Simulated, 41×33 pixels)	21.8mW@10MHz (Segmentation) 60.72mW@10MHz (Initialize)
Pixel Density	26.5pixel/mm^2

For the verification purposes, particularly of the proposed low-power BAO concept, we have designed a test-chip of the main functional unit of the SIA architecture, the image segmentation cell-network with 41×33 cells in 0.35um CMOS technology with 3 metal layers. The die photo of the fabricated test-chip is shown in Fig. 18. Cells and connection-weight-register blocks, enlarged on the right side of Fig. 18, are full-custom designed, resulting in over 50% area reduction as compared to a standard cell based implementation. Simulated power dissipation with the HSIM circuit simulator [7] of the designed test-chip with implemented BAO concept amounts to 21.8mW and 60.7mW in segmentation and initialization phase, respectively. This is even less than the power dissipation of a previously designed 12 times smaller cell-network with 10×10 cells [5], which doesn't include the BAO concept and consumes 24.4mW at 10MHz clock frequency. The characteristic data of the designed image segmentation test-chip are summarized in Table I.

3. Conclusions

In this report, we have proposed a cell-network-based digital image segmentation architecture with pixel parallel processing for gray-scale/color images in real-time applications. A CMOS test-chip for the cell-network, which is the main functional stage, has been fabricated, in a 0.35um CMOS technology and verifies the effectiveness of our proposal. In the performance verification of the test-chip, high speed segmentation in <9.5usec and low power dissipation of <36.4mW@10MHz are measured. The extrapolation results to larger image sizes suggest, that QVGA-size image segmentation will be possible within 300usec@10MHz at the 90nm CMOS

technology node. Furturemore, we have proposed a low-power and hardware- efficient pipelined segmentation architecture for VGA-size motion pictures, which applies a subdivided-image approach (SIA) for compact implementation and a boundary-active-only (BAO) scheme for low-power dissipation. We have verified the effectiveness of the proposed architecture with 51mm^2 test-circuit in 0.35um CMOS technology for the segmentation-network core consisting of 41×33 cells. The segmentation performance for a VGA-size input image is 21.8mW power dissipation and 7.49msec segmentation time at 10MHz clock frequency.

4. Future Plan

The future work includes the test-chip design of a large size cell-network, implementing also peripheral circuits such as the circuits for connection-weight calculation and leader cell selection. The improvement of the architecture for low power dissipation and the development of a complete image segmentation system are further important topics. Currently , we are planning the moving object tracking architecture based on the proposed cell-network based image segmentation architecture and a fully-parallel area-efficient minimum-Manhattan-distance search associative memory. The development of the prototype architecture of the moving object tracking system is an immediate research topic. Moreover, architecture/circuit development for the feature-extraction unit, which requires also selection of concrete application examples is the next step in our research effort towards the complete associative memory-based information processing system.

Acknowledgments

The test-chips in this study have been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in the collaboration with Rohm Corporation and Toppan Printing Corporation. HSIM is licensed within the academic collaboration program of Nassda Corporation.

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[7] Nasda Corporation, "HSIM, Ver.3.0", http://www.nasda.com/, 2004.

5. Published Papers and Patents

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(3) Patents

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Optimized Mixed Digital-Analog Nearest-Match Circuit for Fully-Parallel Associative Memories

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Kazuhiro Kamimura (Faculty of Engineering, B4),
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1. Research Target

A basic operation of pattern recognition is to find the nearest match between an input-data word of W bit length and a number R of reference-data words [1]. For fast and efficient integration of the nearest-match function a fully-parallel associative-memory has been proposed recently [2]. In this fully-parallel associative memory, the search time is primarily determined by the performance of a circuit called winner-line-up amplifier (WLA). The prime goal of the WLA circuitry is to amplify the distance between the winner and the nearest-loser sufficiently so that the following winner-take-all (WTA) circuit can decide the winner at binary logic level. Because of the internal capacitances and resistances in the MOS transistors, there is an inherent delay and the WLA needs considerable time to set at the stable operating point. Moreover, due to use of feedback loop, the WLA is prune to instability and oscillations at higher amplification.

In order to keep the average power of the whole network reasonably low, the current for the mismatched bits should be as low as possible (fraction of μA only). The WLA primarily intends to magnify the distance in the narrow range of the winner and the nearest-loser. For this purpose, the WLA has to operate relatively at higher gain for the winner and nearest-loser. A feedback loop is added in the WLA network that regulates the ml and sets the desired operating point. The feedback regulation has to be done properly, as both under-regulation and over-regulation deteriorates the network performance [2].

The task of this research project is a further improvement of the mixed digital-analog nearest-match circuitry of the fully-parallel associative memory, in particular the WLA, with respect to reduced search time and power dissipation, while maintaining sufficient stability during the search operation.

2. Research Results

2.1 WLA Network with Parallel Capacitances in Match Lines

The presently used WLA is shown in Fig. 1 [3]. A pre-charge transistor MP_{ia} is added in each match line (ml), otherwise, the network will not be able to make a fast decision because of the possibility of different initial voltages on the ml. The transistors MP_{ia} charge ml to

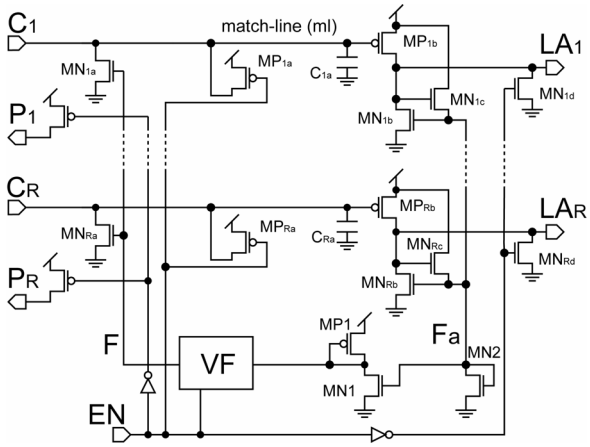

Fig. 1 WLA circuit (WLA-A) with capacitors in the match lines.

V_{DD} as the enable signal (**EN**) goes low. In the evaluation period with **EN** = HIGH, the transistors MP_{ia} turn off and the capacitances discharge through the transistors MN_{ia} controlled by the feedback loop.

2.2 Improved WLA Circuitry for Search Speed Enhancement

From Fig. 1, it is evident that the distance amplification part of the WLA-A network cannot start immediately at the positive edge of **EN**, rather, it has to wait until the capacitance voltage falls to the threshold voltage V_{th} of the transistors MP_{ib}. The search speed of the WLA-A is expected to improve by adding separate

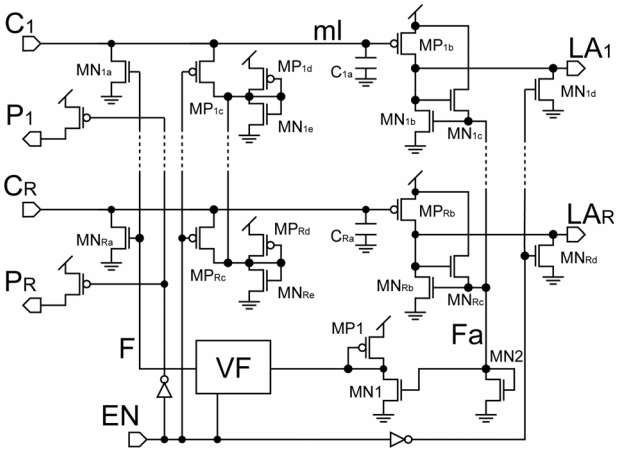

Fig. 2 WLA circuit (WLA-B) with match line pre-charged to V_{DD}-V_{th}.

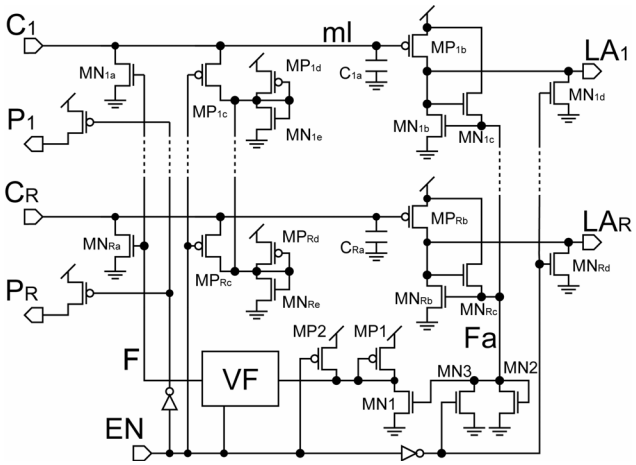

Fig. 3 Reset transistors added in the feedback path in WLA-C network to ensure same initial conditions for all searches.

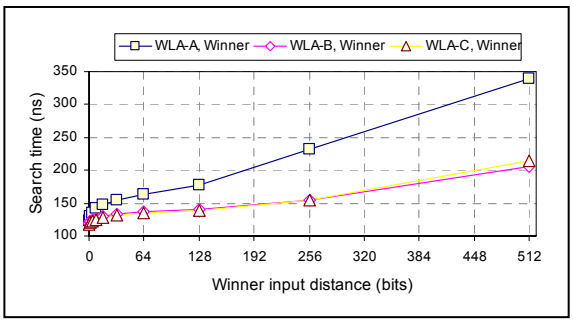

Fig. 4 Winner search times for the nearest-loser set at 1-bit apart while other-losers set at 21-bit distance.

charging sources in each ml as shown in Fig. 2. Each charging source has a pull-up diode MP_{id} connected to a pull-down diode MN_{ie}. It supplies a voltage of V_{DD}-V_{th} to the charging transistors MP_{ic} of the ml. The charging circuit parameters are adjusted to have a current drain of 3.1 µA for each ml.

For both WLA-A and WLA-B circuits, the feedback line voltage (gate voltage of MN_1) may have some residual charges whose magnitude differs at different pre-search conditions. Although it does not have significant impact on the search result, it improves search reliability to have same initial conditions in all parts of the WLA network before a search starts. A reset transistor MN_3 added in the feedback path as shown in Fig. 3, discharges residual charges thus forcing the feedback line to start from the same initial condition for all new searches. The three WLA versions (WLA-A, WLA-B and WLA-C) are compared in an 350 nm CMOS technology for an associative memory with Hamming

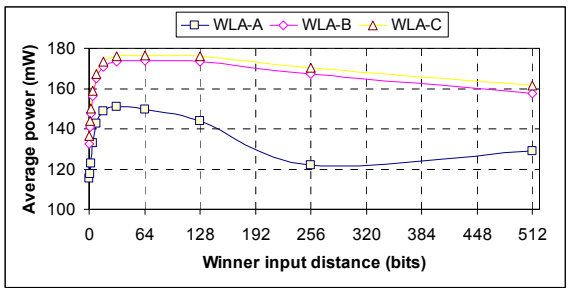

Fig. 5 Power consumption for the nearest-loser set at 1-bit apart while other-losers set at 21-bit distance.

distance search strategy having standard WTA circuits [4] in the output stage and 128 reference patterns with 512 bit length each.

Search results for the associative memory with the nearest-loser set at the most difficult 1-bit distance and all other-losers at 21-bit apart are shown in Fig. 4. The search-time reduction with WLA-B is about 37% to less then 180ns. The additional reduction with WLA-C is less than 1%. The cost of the shorter search times in terms of increased power dissipation is depicted in Fig. 5. Circuit WLA-B increases maximum average power dissipation by about 14% while circuit WLA-C adds about another 1%.

3. Conclusion

The most effective improvement of the WLA circuit in the fully-parallel associative memory was a changed pre-charging of the match-lines from V_{DD} to $V_{DD} - V_{th}$. The resulting reduction of the maximum search time was about 37% at the cost of only 17% increased power dissipation. Pre-charging of the internal nodes of the feedback loop was less effective, leading only to an additional improvement of 1%.

4. Future Plan

Kaji Mujibur Rahman finished his work as a COE researcher in April 2004 and returned Bangladesh University of Engineering and Technology. He is planning to continue cooperation with the COE and his research work on improved nearest-match circuits for the fully-parallel associative memories in Bangladesh. One important idea for a further reduced search time at even lower power dissipation is the application of a WLA circuit based on match-line-current comparators.

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3. Published Papers and Patents

① Proceedings

1. K. M. Rahman, K. Kamimura, T. Koide and H. J. Mattausch, "Improved Mixed Digital-Analog-Match Circuit for Fully-Parallel Associative Memories," Second Hiroshima International Workshop on Namoelectronics for Terra-Bit Information Processing, pp. 40-41, 2004.

2. K. Kamimura, K. M. Rahman, T. Koide and H. J. Mattausch, "Optimized Multi-stage Minimum-Distance-Search Circuit with Feedback Stabilization for Fully-Parallel Associative Memories" Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2004), in press, 2004.

Development of Digital-CMOS-Based Real-Time Color-Motion Picture Segmentation Architecture and its LSI Chip Verification

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Graduate School of Advanced Sciences of Matter),
Hans Jürgen Mattausch (Prof., Research Center for Nanodeivices and Systems,
Graduate School of Advanced Sciences of Matter)

1. Research Target

Image segmentation is the extraction process of all objects from natural input images and is the necessary first step of object-oriented image processing such as object recognition or object tracking. However, conventional gray-scale and color image segmentation algorithm are implemented in software with general purpose or digital-signal processors resulting in relatively large size, large power dissipation, and high cost for application hardware.

Objective of this research is the proposals of a hardware-oriented segmentation algorithm and it's digital CMOS implementation.

2. Research Results

We propose a highly-parallel digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network based implementation architecture in state-of-the-art CMOS technology. The segmentation algorithm uses a region-growing approach, which can be viewed as a simplified digital version of a locally-excitatory globally-inhibitory oscillator network (LEGION). Color and gray-scale picture segmentation differ only in the expressions for the connection-weight calculation between the network cells. Fig. 1 shows an explanation of our segmentation algorithm with 3×3 gray-scale example image. The proposed VLSI implementation architecture (Fig. 2) based on a digital-algorithm consists of 4 functional stages for connection-weight calculation, leader-cell determination, image segmentation and segmentation-result restoring, respectively. The image-segmentation network, which is the core of the proposed architecture, consists of cells (Fig. 3) and connection-weight registers (Fig. 4). Each cell represents a pixel of the original picture. In this network, the self-excitation and excitation steps of the algorithm of Fig. 1 are carried out for all pixels of the picture in parallel. As shown in Fig. 5, the complete cell network can be implemented by alternately laying a cell, corresponding to a pixel, and a horizontal or vertical connection-weight register block. Thus the connection weights can be efficiently shared among neighboring cells, and the wiring length and circuit area can be minimized. Since the cell structure becomes simple and compact, high speed and high density implementation is achieved.

The test-chip of Fig. 6 for the cell-network core was designed in 0.35μm, 3 metal CMOS technology. Decoder and adder/subtractor of the network cells, which consume the largest area portion, were designed in full-custom. An integration density of 19.6 pixels/mm^2 was thus achieved. We have also estimated the possible pixel density for full-custom high-speed (Fig. 3a) and high-density (Fig. 3b) designs in scaled-down CMOS technologies, assuming just 3-metal layers. From this data we expect a one-chip integration of the proposed architecture for 300×300 pixel pictures at the 100nm technology node and for 800×600 pixel pictures at the 50nm technology node.

3. Relationship with COE Program

The research on this subject is indispensable for a "Real-Time Image Recognition System", which is one of the important COE research tasks.

4. Summary and Future Work

A real-time image segmentation for gray-scale and color images is developed. From our present results, VGA size video segmentation is expected to become possible in 50nm CMOS technology.

The future research work is concerned with the development and verification of new algorithm, which will enable low-power real-time image segmentation hardware for VGA-size (640×480) video data.

5. Published Papers and Patents

① Published Papers

1. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Efficient video-picture segmentation algorithm for cell-network-based digital CMOS implementation," IEICE Trans. on Info. & Sys., Vol.E87-D (2) (2004) pp. 500-503.

② Proceedings

1. T. Koide, T. Morimoto, Y. Harada, and H. J. Mattausch, "Digital gray-scale/color image-segmentation architecture for cell-network-based real-time applications," Proc. of The 2002 Int'l Tech. Conf. on Cir. & Sys., Computers. and Communications (ITC-CSCC2002) (2002) pp. 670 -673.
2. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Real-time segmentation architecture of gray-scale/color motion pictures and digital test-chip implementation," Proc. of The 2002 IEEE Asia-Pacific Conf. on ASICs (AP-ASIC2002) (2002) pp. 237-240.
3. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Low-complexity, highly-parallel color motion-picture segmentation architecture for compact digital CMOS implementation," Ext. Abs. of the 2002 Int'l Conf. on Solid State Devices and Materials (SSDM2002) (2002) pp. 242-243.
4. Y. Harada, T. Morimoto, T. Koide, and H. J. Mattausch, "CMOS test chip for a high-speed digital image-segmentation architecture with pixel-parallel processing," Proc. of The 2003 Int'l Tech. Conf. on Cir. & Sys., Computers. and Communications (ITC-CSCC 2003) (2003) pp. 284-287.
5. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Low-power real-time region-growing image- segmenta-

tion in 0.35μm CMOS due to subdivided-image and boundary-active-only architectures," Ext. Abs. of the 2003 Int'l Conf. on Solid State Devices and Materials (SSDM2003) (2003) pp. 146-147.
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③ Patents

1. "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus", JPN Patent Application No. 2002-152491, (2002.05.27).
2. "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus", USA Patent Application No.10/445,247 (2003.05.26), EPC Patent Application No.03011840.0 (2003.05.26),KOR Patent Application No.2003-33324 (2003.05.26), TWN Patent Application No.92114142 (2003.05.26).

④ Awards

1. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "A real-time picture-segmentation archictecture for intelligent information processing, " 4th LSI IP Design Award, Development Encouragement Award, LSI IP Design Award Committee, 2002.5. URL http://ne.nikkeibp.co.jp/award/
2. T. Morimoto, "Research for Real-Time Image Segmentation Architecture and its Digital-CMOS Implementation," Hiroshima University Student Award, President of Hiroshima University, Taizou Muta, No. 1-0061, 2003.3.

⑤ Others

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2. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "A cell-network-based image segmentation LSI for rel-time applications," The 5th IEEE Hiroshima Student Symposium (HISS) (2002) pp. 221-224, in Japanese.

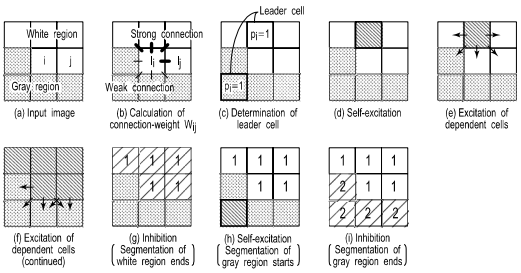


Fig.1 Explanation of our segmentation algorithm with 3×3 gray-scale example image.

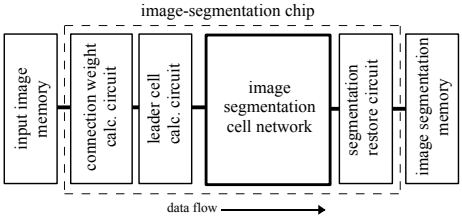


Fig.2 Block diagram of the proposed architecture.

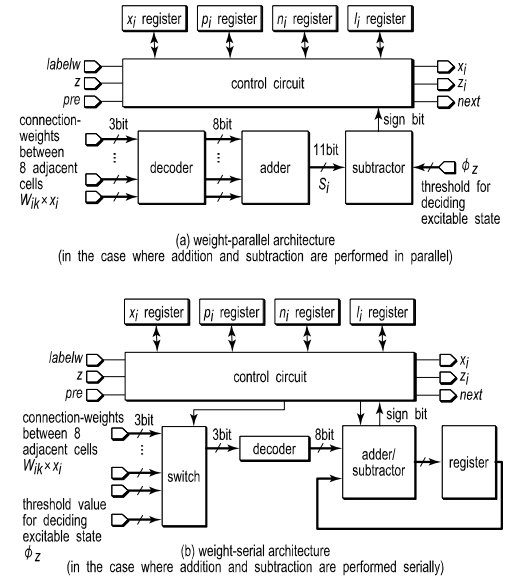


Fig.3 Structure diagram of the network cell.

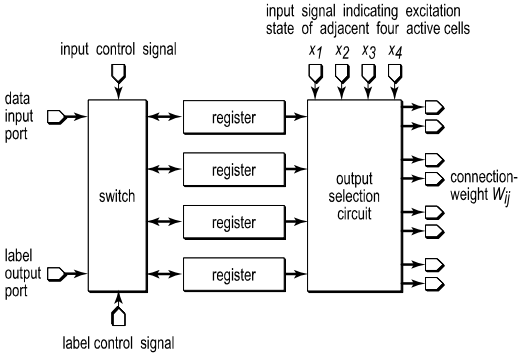


Fig.4 Structure diagram of a connection-weight-register block.

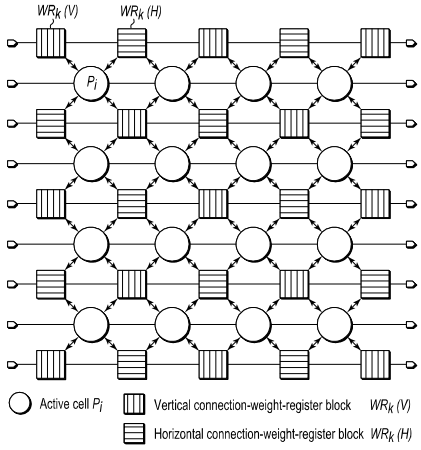


Fig.5 Block diagram of the cell-network construction for 4×4 pixels.

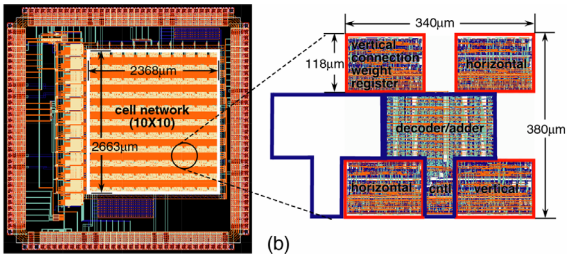


Fig.6 The layout of the test-chip with 0.35μm 3-metal layer CMOS technology.

4-II. Device Modeling

TEG Design for HiSIM Model-Parameter Extraction and Parameter Extraction with Single Structures

Mitiko Miura-Mattausch (Prof., Graduate School of Advanced Sciences of Matter),
Takeshi Mizoguchi (Graduate School of Advanced Sciences of Matter, M2),
Yasuhito Uetsuji (Graduate School of Advanced Sciences of Matter, M1)

1. Research Target

Our COE project aims at fusion of silicon-based nanodevice, circuit and chip-architecture research. For realizing the fusion, we develop HiSIM-Microwave, a transistor model valid for RF applications including possibility to simulate optical responses as well as electromagnetic response . As a first step for the realization, we have designed TEGs (Test Element Groups) with the 0.18μm TSMC technology for extracting HiSIM model parameters to be used both for circuit design and device design. The designed TEG was fabricated by TSMC, and measurements and their analysis were performed.

For accurate RF-circuit simulation, HiSIM has to be accurate, and the model parameter values have to be reliable. With TEG measurements, we will check the quality of HiSIM for advanced devices such as for RF devices, as well as the reliability of model parameter extracted from measurements.

2. Research Results

Fig. 1 shows designed TEG blocks in 3x3mm^2 area. A large area, about 1/3 of the total area, is used for single MOSFET structures. These blocks consist of different single-MOSFET sizes, different gate lengths and widths. These measurements are used to extract general device features valid for any sizes. Since HiSIM description is scalable for any MOSFET sizes, the number of the transistors required in TEGs is not so many as usually prepared.

We have also designed couple of TEG blocks for high-frequency measurements. For the accurate measurements, to exclude external contribution is the key. TEGs have been designed to fulfill the requirements.

Additionally a block was designed by a designer group, where real RF-circuit-performance tests are available.

Fig. 2 shows statistics of measured threshold voltage from 16 chips of p-MOSFET with gate length of 0.18μm. Extremely large variations are observed. This means the technology is not yet mature for the shortest design rule.

3. Summary

Figs. 3-7 show comparison of measured current-voltage characteristics with HiSIM calculation results for five different gate lengths, from long to short . For the calculation only one model parameter set is applied for any device sizes. It is seen that the extracted HiSIM parameters reproduce measurements within variations among chips.

4. Future Plan

As the second step, high-frequency measurements will be performed and the HiSIM validity for the measurements will tested.

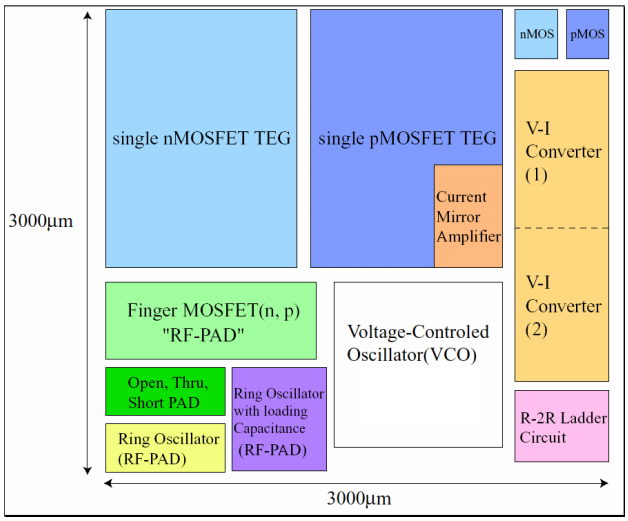


Fig. 1. Designed chip layout

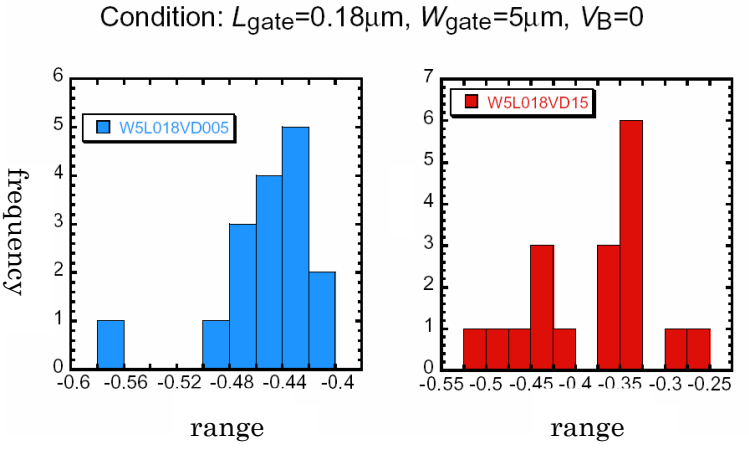


Fig. 2. Measured statistics from 16 chips.

Figs. 3-7. Comparison of measured I-V characteristics with HiSIM calculation results.

Fig3.

$L_{channel}$=2.0μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

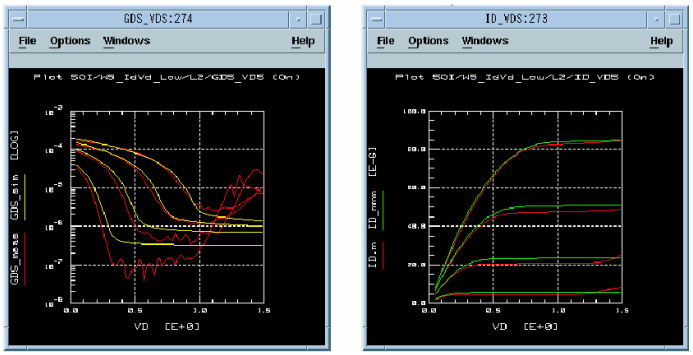


Fig4.

$L_{channel}$=0.70μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

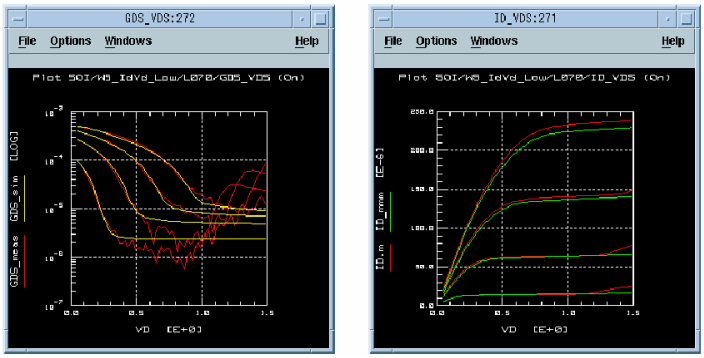


Fig5.

$L_{channel}$=0.50μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

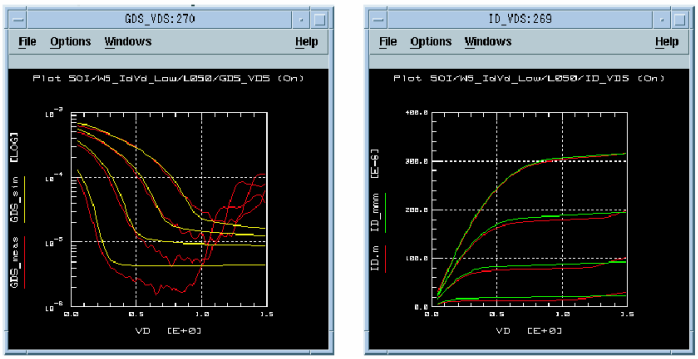


Fig6.

$L_{channel}$=0.30μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step

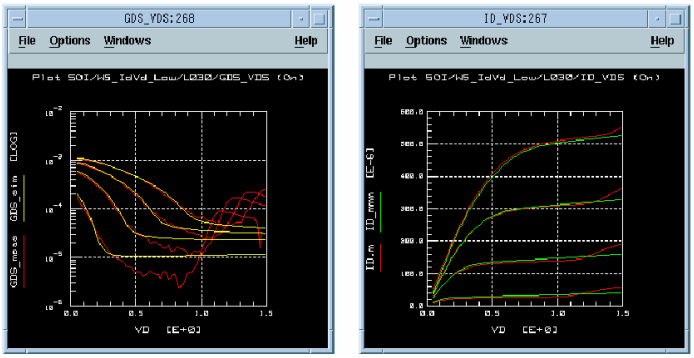
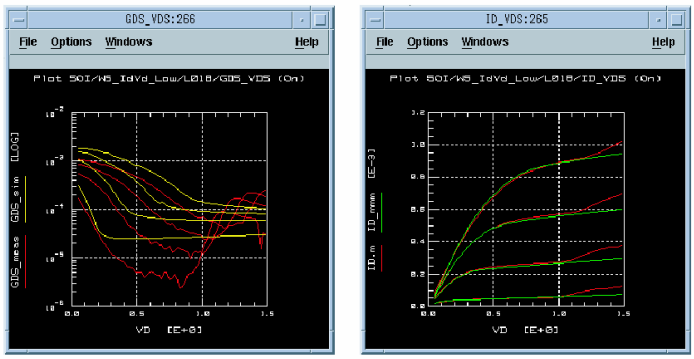


Fig7.

$L_{channel}$=0.18μm, W=5.0μm I_{DS}-V_{DS} and G_{DS}-V_{DS} characteristics

Conditions: V_{DS}=-1.49V ~ 50mV; 0.02V step, V_{BS}=0
V_{GS}=-1.5 ~ -0.6V; 0.3V step



Measurement of Thermal Noise for 100nm-MOSFET And Its Modeling

Mitiko Miura-Mattausch (Prof., Graduate School of Advanced Sciences of Matter),
Satoshi Hosokawa (Graduate School of Advanced Sciences of Matter, M2)

1. Research Target

The thermal noise (TN) is becoming important as RF application of MOSFETs is becoming realistic. However, to achieve accurate measurement is still a serious task, and thus to realize its accurate modeling is also an urgent task for accurate simulation of RF-circuits. Our aim is to investigate the origin of observed TN enhancement, and to develop its model based on the origin, which can be even used for testing and supplementing measurements.

The thermal noise is independent of applied frequency. Thus the Nyquist theorem describes the spectral intensity of the TN current (S_{id}) of a MOSFET at temperature T [1, 2]

$$S_{id} = \frac{4kT}{L_{eff}^{\ 2} I_{ds}} \int_{\phi_{S0}}^{\phi_{SL}} g_{ds}^{\ 2}(\phi_S) d\phi_S = 4kTg_{ds0}\gamma \qquad (2)$$

where k, R, g_{ds}, g_{ds} , g_{ds0} , γ are Boltzmann's constant, channel resistance, transconductance, that at V_{ds} =0, and noise cofficient, respectively. Origin of TN is attributed to the carrier fluctuation in a time interval. The Nyquist theorem predicts that γ varies from 1 to 2/3 as a function of V_{ds} for long-channel transistors as shown in Fig. 1 schematically, and has been prove experimentally. For short-channel transistors, Knoblinger et al. measured much larger γ than 2/3, even more than 3 in the saturation region [3]. The reason was explained by hot electrons [4]. Jamal et al. have measured smaller values, and they modeled S_{id} only with the effective channel length L_{eff} considering the channel length modulation as shown in Fig. 2 [5]. Their result shows a monotonically increasing γ characteristics as a function of V_{ds} for the gate length L_g of 0.18μm,similar to the Knoblinger result. Recently, Scholten et al. measured that γ for L_g=0.18μm is about 1 in the saturation region [6]. They explained the enhanced γ by the velocity saturation. However, detailed description of the model is not given.

2. Research Results

We followed the Nyquist theory given in Eq. (1). For the g_{ds} description we applied HiSIM, a circuit simulation model based on the drift-diffusion approximation [7]. The approximation allows the description to be valid for any bias conditions. The final TN description is verified with γ , which gives universal relationship without varying from technology to technology. Fig. 3 shows the calculation result including both the velocity saturation and the channel-length modulation by symbols. Calculated γ characteristics are nearly the same for all gate lengths, and expected γ increase is not obtained. From this fact a conclusion is derived that an important feature of the enhanced TN origin is missing in the modeling.

We have derived the TN description including position dependence of all physical quantities along the channel such as the mobility and the carrier concentration. The final equation is a function of surface potentials at source & drain sides and derivalives. Calculated γ with the model is also depicted in Fig. 3. Thus the reason of the γ increase for short-channel MOSFETs is attributed to the position dependence of physical device quantities. Here origin of the dependence is reduced to the surface potential distribution along the channel. The basis of the Nyquist theorem is the carrier fluctuation by scattering, and this is enhanced by the potential increase along the channel. HiSIM distinguishes potential values at source & drain sides, which allows us to include the potential gradient in a consistent way.

Calculated TN characteristics are compared with the Scholten measurements in Fig.4. Required model parameters for the calculation were extracted from measured current-voltage characteristics with a normal parameter extraction. Without any fitting parameter good agreement can be achieved for any channel length and any bias conditions. This concludes that the TN characteristics are determined only by the carrier transport in the channel, and the origin of the carrier transport is the potential difference along the channel. The difference of TN with other device characteristics such as the drain current is that the gradient itself, namely g_{ds}, determines the characteristics. Fig. 5 shows the γ characteristics as a function of V_{ds}. By reducing L_g, γ increases, but not so drastic as reported previously. It is also seen that γ for short L_g length reduces in the liner region, and starts to increase as V_{ds} entering the saturation condition, causing steep potential increase in the channel. The minimum of γ becomes larger than 2/3 as reduction of L_g is further continued.

3. Summary

We found that the enhancement of TN for short-channel MOSFETs is caused by potential gradient in the channel. A model developed on the basis of the concept reproduces measured noise characteristics without fitting parameter.

4. Future Plan

The noise induced by drain current has been investigated. For RF-circuit applications the gate induced noise becomes serious as well. This will be focused.

5. Papers and Presentation

Presentation

S. Hosokawa, Y. Shiraga, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, H. Masuda, and S. Miyamoto, *Ext. Abs. Int. Conf. SSDM*, 20 (2003).

Patent

2003-420845: Drain-current-thermal-noise analysis and simulation method, 18th December, 2003.

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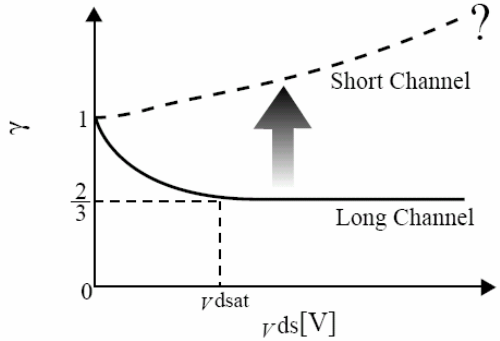

Figure 1: Schematic of γ as a function of $V_{\rm ds}$ for a long channel MOSFET. The dashed line showes that given in [4].

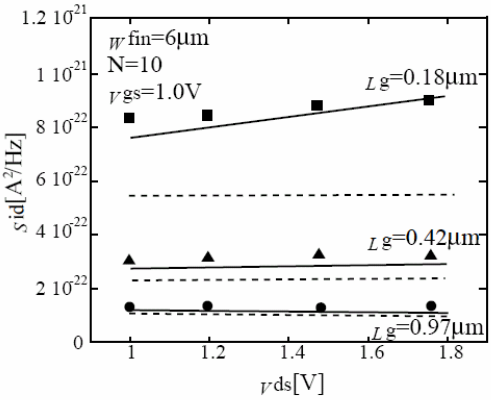

Figure 2: Comparison of measured thermal noise current (symbols) with calculated results as a function of $V_{\rm ds}$ given in [5] : with the channel length modulation (solid lines) and without the channel length modulation (dashed lines).

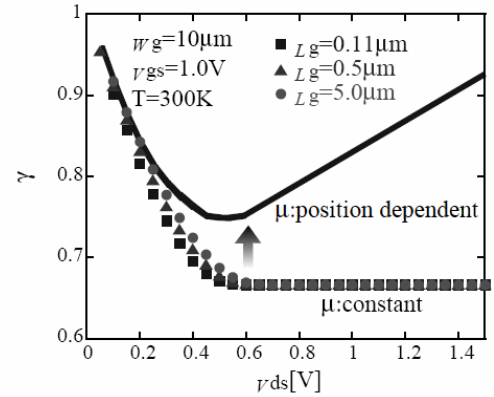

Figure 3: Calculated γ with a constant mobility (symbols) and that considering the position dependence (solid line) for a short channel.

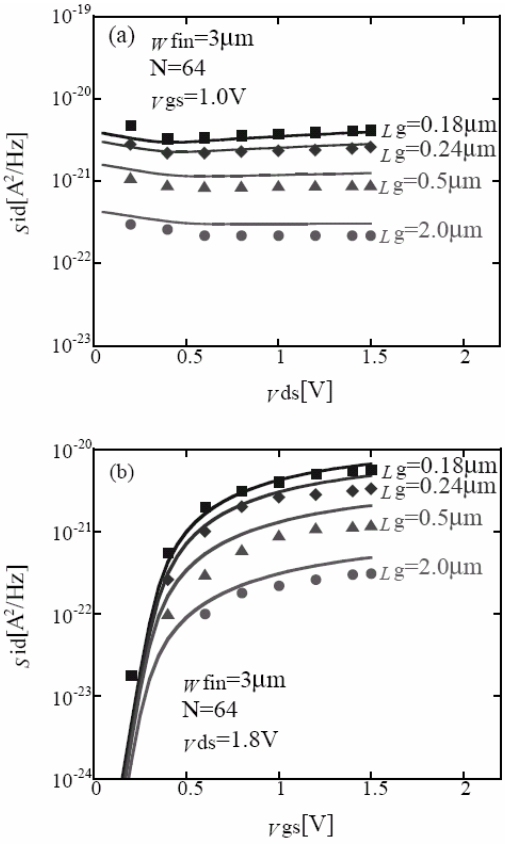

Figure 4: Calculated thermal noise cuurent characteristics with the developed model (solid lines) compared with measurements (symbols) given in [6], (a) as a function of $V_{\rm ds}$ and (b) as a function $V_{\rm gs}$.

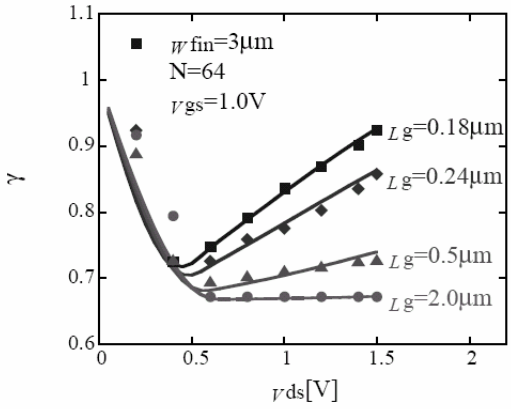

Figure 5: Calculated γ with the developed model as a function of $V_{\rm ds}$ (solid lines) compared with the transformed Scholten measurements into γ, where the $g_{\rm ds0}$ values are selected so that γ unity at $V_{\rm ds}$=0.

Inversion Charge Model of SOI-MOSFET for Circuit Simulation and 1/*f* Noise Analysis

Mitiko Miura-Mattausch (Prof., Graduate School of Advanced Sciences of Matter),
Norio Sadachika(Faculty of Engineering, B4)

1. Research Target

The MOSFET is the most widely applied device, and possible future variations such as double-gate MOSFET as well as FinFET have been intensively investigated [1]. Their models for circuit applications are now under development with different applications[2]. Our objective is to develop a circuit simulation model for the fully-depleted SOI-MOSFET as the first step for describing phenomena caused by the channel confinement between two oxide layers. Advantage of pursuing the fully-depleted SOI-MOSFET is that the modeling accuracy is easily verified by measured characteristics of production-level SOI-MOSFET technologies.

Existing SOI-MOSFET models are suffering convergence problems in circuit simulation. The main reason is a violation of the charge conservation. The SOI-MOSFET has three important Si-SiO_2surfaces as can be seen in Fig. 1 . Charges are induced at all surfaces. Thus surface-potential-based modeling is the only solution for the SOI-MOSFET to secure the charge conservation in a consistent way. We have developed the SOI-MOSFET model HiSIM-SOI based on this charge conservation guideline. Our investigation here focuses on carrier density changes in the SOI channel in comparison to the bulk-MOSFET. For this purpose the 1/*f* characteristics are studied, since the 1/*f* noise is sensitive to the carrier concentration as well as its density distribution in the channel[3].

2. Research Results

To include all device features of the SOI-MOSFET accurately, HiSIM-SOI determines not only the surface-potential at the channel surface, but also at the back side, as well as at the bulk back-gate self-consistently as schematically depicted in Fig. 1 [4]. The total iterative potential calculation requires only about twice as much calculation time as for the bulk-MOSFET case, solving just at the channel-surface. Fig. 2 demonstrates the accuracy of the three calculated

Surface potentials in comparison to the results with the 2D-device simulator MEDICI. Fig. 3 compares HiSIM-SOI simulation results of the channel-inversion charge with MEDICI for two silicon-layer thicknesses T_{SOI}. The bulk-MOSFET result is also depicted for comparison. Enhancement of the carrier concentration is obvious. The model reproduces measured *I-V* characteristics within numerical accuracy as shown in Fig. 4, and is verified to show stable convergence in circuit simulation.

Fig. 5 compares simulation result of the 1/*f* noise with measurements. For the HiSIM-SOI simulation two model parameters are fitted: *NFTRP* determining the magnitude of the 1/*f* noise; and *NFALP* determining the contribution of the mobility fluctuation due to carrier trap/detrap. The fitted *NFTRP* value is the nearly the same as that of the bulk-MOSFET, and *NFALP* is very small in comparison with *NFTRP* but about 10 times larger than for the bulk-MOSFET. Good agreement of the measured and simulated noise-voltage characteristics is the proof of accurate calculation of the carrier concentration and its distribution along the channel. Deviation of three measurement points (open triangles) from simulation results is attributed to impact ionization, which is not yet included in HiSIM-SOI.

Comparison with the bulk-MOSFET is shown in Fig. 6. Increased noise density is obvious and explained by the higher carrier concentration in the channel, as evident from Fig 3. Fig. 7 shows the expected noise increase for reduced T_{SOI}, which will cause serious problems in circuit applications.

3. Summary

Reduction of T_{SOI} enhances the driving capability of the SOI-MOSFET. However, we have found the necessity of considering a trade-off between the driving capability and the 1/*f* noise. The enhanced noise due to the increased carrier concentration, caused by the inversion-layer confinement, will also cause serious problems in future devices such as the double-gate MOSFET and the FinFET.

4. Future Plan

Accuracy and stable convergence of the developed HiSIM-SOI will be checked with real circuits.

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5. Papers and Presentation

Presentation

N. Sadachika, Y. Uetsuji, D. Kitamaru, L. Weiss, U. Feldmann, S. Baba, H. J. Mattausch, M. Miura-Mattausch, “Fully-Depleted SOI-MOSFET Model for Circuit Simulation and Its Applications to 1/f Noise Analysis,” Proc. Simulation on Semiconductor Processes and Devices, 2004.

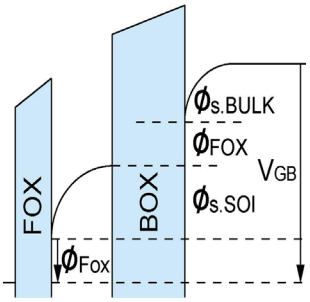

Fig. 1. Schematics of the fully-depleted SOI-MOSFET. The three surface potentials are solved iteratively with the Poisson equation.

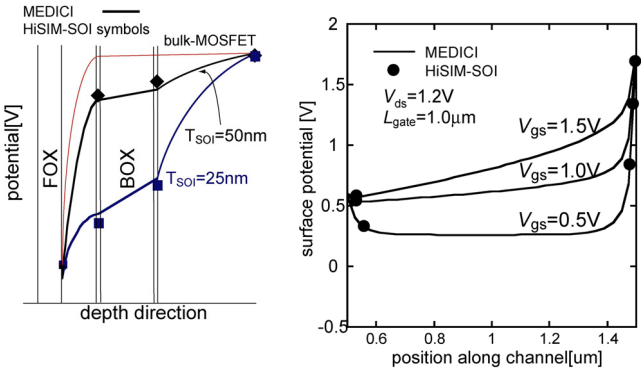

Fig. 2. Comparison of HiSIM-SOI calculated surface potentials with the results of the 2D-device simulator MEDICI.

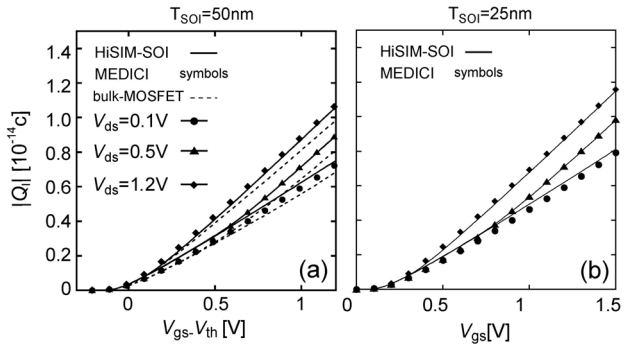

Fig. 3. Comparison of calculated inversion charge Q_I with MEDICI results, for a silicon-layer thickness of (a) 50nm and (b) 25nm. The bulk-MOSFET result is plotted in addition in (a).

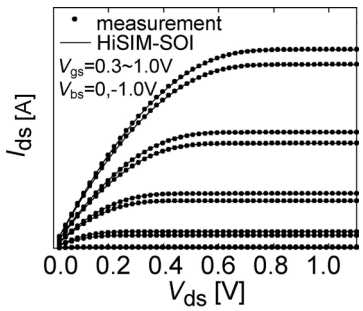

Fig. 4. Calculated drain current I_{ds} as a function of drain voltage V_{ds}. Symbols are measurements.

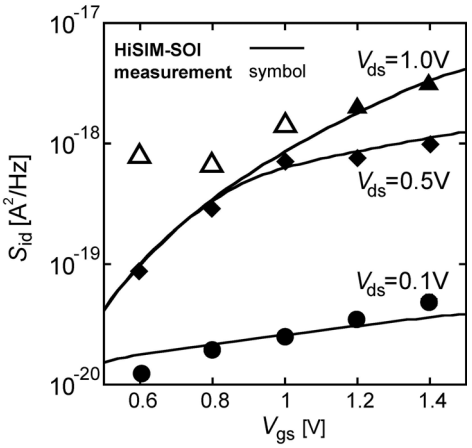

Fig. 5. Calculated 1/*f* noise density as a function of gate voltage V_{gs}. Symbols are measurements. Deviation of the three open triangles from the HiSIM-SOI result is attributed to impact ionization, which is not yet included in HiSIM-SOI.

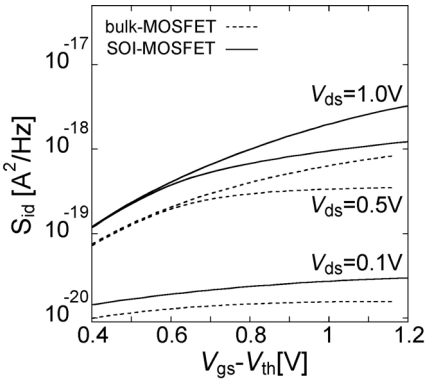

Fig. 6. Comparison of calculated 1/*f* noise for the fully-depleted SOI-MOSFET with that of the bulk MOSFET.

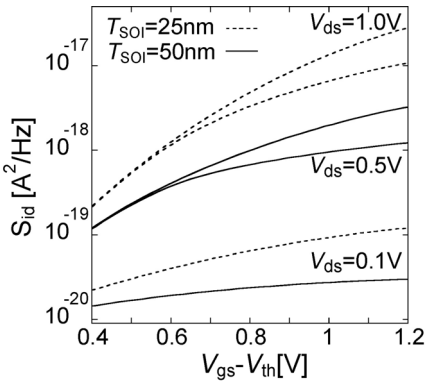

Fig. 7. Comparison of calculated 1/*f* noise for the different SOI-layer thicknesses.

Modeling of Optoelectronic Devices

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1. Research Target

Signal propagation delay via metal interconnects is becoming a serious problem in realizing high-frequency operation of circuits. The immediate solution is to adopt a large cross-section of metal interconnects, but this hinders high integration of devices in a single chip. Under such a situation, optical interconnects attract much attention [1], which involves light emitting devices, optical waveguides and photodetectors. In order to fully realize optical interconnects, models describing the physical properties of optoelectronic devices become a requirement.

At present, our research group is investigating the response of photodiodes integrated on a Si chip [2,3], which are employed as photodetectors in optical interconnects. We are developing a physics-based model describing the carrier transport characteristics in a photodiode. The model will be useful in predicting photodiode characteristics and performing circuit simulation of optoelectronic integrated circuits (OEICs) [4].

2. Research Results

2.1 Photoresponse of *p-n* Photodiode at High Illumination

We fabricated *p-n* photodiodes using conventional CMOS technology as shown in Fig. 1a. To generate carriers in the depletion region at the *p-n* junction, laser pulses are injected to the n^+ region via the metal layer opening. In our measurement, we used a 532nm-pulsed laser with pulse duration of ~1ns FWHM, an absorption coefficient of ~10^4cm^{-1} and absorption depth of ~1μm into bulk Si. Generated electrons and holes drift to opposite electrodes due to the applied reverse bias and flow out the external circuit as photocurrent. The measurement setup is shown in Fig. 1b. The photocurrent is measured using an oscilloscope. The measured photocurrents are shown in Fig. 2a for different reverse bias voltages. In the low intensity of radiation or the high reverse bias cases, the measured photocurrent keeps the same shape as the irradiated laser pulse, and no time delay is observed. However, by increasing the laser intensity, transport delay becomes clear for low bias conditions. To analyze the measured photocurrent characteristics, 2D device simulations with MEDICI [5], which involve solving the four basic device equations, were performed. Simulation conditions are chosen to be the same as measurement conditions. Simulation results shown in Fig. 2b are similar to the measurements. The apparent transport delay observed for the high laser intensity was found to be due to the high carrier concentration suppressing the potential drop in the depletion region. The highly generated carrier concentration diminishes the field in the depletion region resulting in a reduction of carrier movement. More remarkable observation is that simulated photocurrent shapes for small bias show clear deviation from corresponding measurements. Obvious plateaus occur which are not observed in the measurements. We attribute the reason to the shortcoming of the quasi-equilibrium condition approximated in the 2-dimensional simulator. Such shortcoming originates from the breakdown of the drift-diffusion approximation used in the simulation [3]. Therefore we proposed a necessity of modifying mobility models used in the drift-diffusion approximation at high illumination and low reverse bias condition. This study serves as a foundation to develop a carrier transport model of photodiodes in any operating condition.

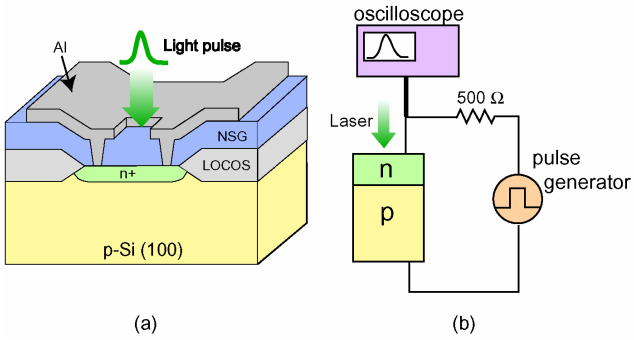

Fig. 1. (a) Cross-section of fabricated *p-n* junction. (b) Setup for measuring photocurrent.

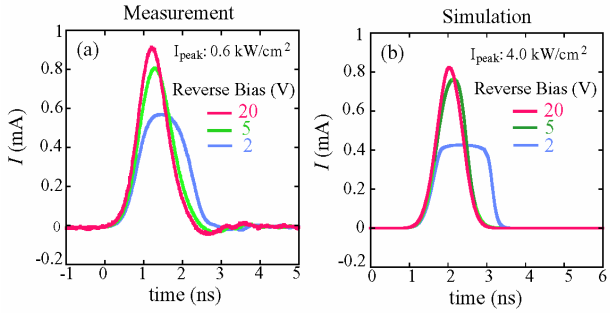

Fig. 2. (a) Measured and (b) MEDICI simulation results of photocurrent for different applied reverse biases.

2.2 Modeling of Vertical *p-i-n* Photodiodes

For the purpose of developing a model for circuit simulation of OEICs, we analytically formulate carrier transport [4] in a vertical *p-i-n* photodiode as shown in Fig. 3. The vertical *p-i-n* photodiode has been discussed by many authors [6], and analytical description has also been developed [7]. However, one important factor, *diffusion* of carriers generated in n^+ and p^+ diffusion region which is used in characterizing the cut-off frequency of the photodiode, has been neglected so far. This factor determines the cut-off frequency in the cases of small load resistance and moderate intrinsic region length. Thus, we take into account the effect of carrier diffusion. We obtained analytical solution for photocurrent in Fourier space, and therefore our formulation is very useful in harmonic balance simulation [8] for circuits. Furthermore, we developed a simulation scheme based on the spectral method [9] for reproducing current in time domain using Fast Fourier Transform (FFT). By using the derived solution in the frequency domain and the scheme, we successfully reproduced the output current (see Fig. 4), which has a comparable accuracy with MEDICI [5] in spite of significant reduction of computational time.

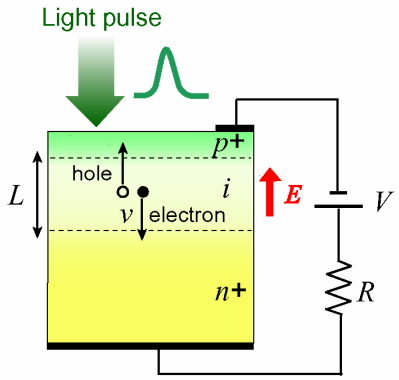

Fig. 3. Structure of a vertical *p-i-n* photodiode.

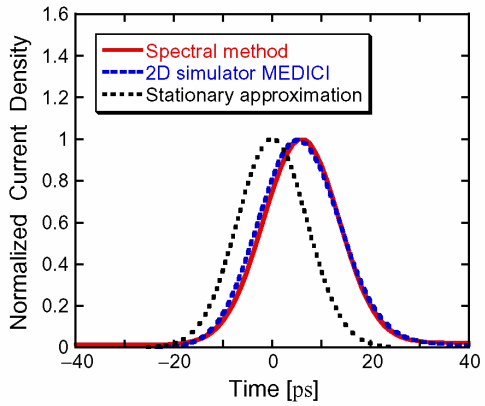

Fig. 4. Photocurrent calculated by our model in comparison with MEDICI and stationary approximation. The model is in excellent agreement with MEDICI.

2.3 Cut-Off Frequency of Lateral *p-i-n* Photodiodes

We also investigated lateral *p-i-n* photodiode. This type of photodiode is free from light absorption depth limitation inherent with the vertical type, and thus high responsivity is possible. Moreover, the technology is compatible to VLSI processes. For our purpose, we fabricated a Si lateral *p-i-n* photodiode as shown in Fig. 5.

Figure 6a shows measured output photocurrent, from which reverse bias dependence can be found. Figure 6b shows results transformed to frequency domain of the photoresponse. The input is a Gaussian laser pulse of ~60ps FWHM. We confirmed ~1GHz cut-off frequency of the fabricated device in Fig. 6b.

To clarify the cause of the tail part (in Fig. 6a) which determines the cut-off frequency, we performed numerical simulation using MEDICI [5]. Changing the $n+$ and $p+$ diffusion depth from 0.1μm to 5μm, we confirmed the reduction of the tail part as shown in Fig. 7. Therefore short intrinsic region length, large reverse bias, and deep diffusion depth are necessary factors for achieving high cut-off frequency photodetectors [10]. This study is useful for developing a model of carrier transport in the lateral *p-i-n* photodiodes

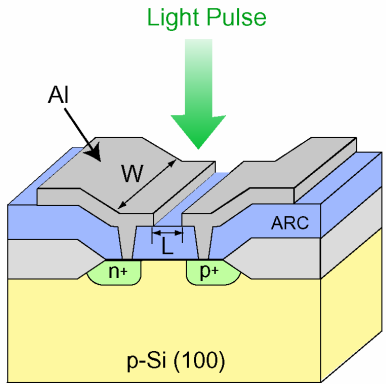

Fig. 5. Structure of a fabricated lateral *p-i-n* photodiode.

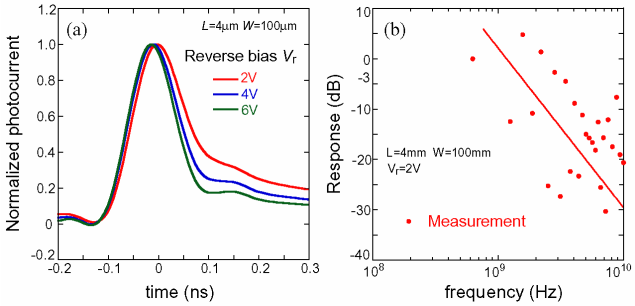

Fig. 6. (a) Measured photocurrent of the lateral *p-i-n* photodiode. (b) The cut-off frequency of the fabricated photodiode is extracted to be ~1GHz.

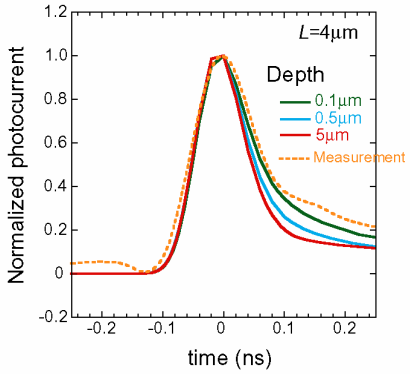

Fig. 7. MEDICI simulation of photocurrent for different diffusion depths. The tail reduces as the diffusion depth is increased.

3. Research Results

We have investigated photoresponse of photodiodes theoretically and experimentally. Through the experiment for a *p-n* photodiode at high illumination, we clarified carrier transport in which the ordinary drift-diffusion approximation is not appropriate. Furthermore, we suggested a necessity of modifying present mobility models if we use the framework of the drift-diffusion approximation. We also perform a measurement of photocurrent for lateral *p-i-n* photodiodes. From this work, the causes of the end tail in the measurements are investigated. The important features of the carrier transport are useful for modeling such devices. We also developed a model describing carrier transport in the vertical *p-i-n* photodiodes. In particular, we considered the diffusion of carriers generated in the n^+ or p^+ region, which has been neglected so far. The photocurrent calculated by our model in time domain shows excellent agreement with the result obtained by using 2-dimensional device simulator MEDICI. Our model is useful for performing circuit simulation of OEICs employing vertical type of *p-i-n* photodiodes

4. Future Work

We will develop models describing the carrier transport in the *p-n* and the lateral *p-i-n* photodiodes, based on the experimental studies we have carried out. The lateral *p-i-n* photodiodes have significant features over the vertical one since the carrier moving path is perpendicular to light absorption direction. Thus, it does not suffer from limitations due to light absorption length. With this feature, it enables both high responsivity and high speed device operation. Furthermore, it realizes fabrication of silicon monolithic photodetectors since the technology is compatible to VLSI processes. Finally we are aiming at performing circuit simulation of OEICs using the developed models in this work.

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5. Papers and Presentation

① Refereed Journals

1. O. Matsushima, K. Konno, M. Tanaka, K. Hara, M. Miura-Mattausch, "Carrier Transport in Highly Generated Carrier Concentration", Semicond. Sci. Tech. **19**, S185 (2004)
2. K. Konno, O. Matsushima, D. Navarro, M. Miura-Mattausch, "Limit of Validity of the Drift-Diffusion Approximation for Simulation of Photodiode Characteristics", Appl. Phys. Lett. **84**, 1398 (2004)
3. K. Konno, O. Matsushima, D. Navarro, M. Miura-Mattausch, "High-Frequency Response of *p-i-n* Photodiode Analyzed by an Analytical Model in Fourier Space", Submitted to J. Appl. Phys.

② Presentation

1. O. Matsushima, K. Konno, M. Tanaka, K. Hara, M. Miura-Mattausch, "Carrier Transport in Highly Generated Carrier Concentration", International Conference on "Nonequilibrium Carrier Dynamics in Semiconductors", Modena, Italy, July 28-Aug 1, 2003.
2. K. Konno, O. Matsushima, K. Hara, G. Suzuki, M. Miura-Mattausch, "Modeling of Photoresponse of *p-i-n* Photodiodes and Current Simulation based on the Spectral Method", Japan Society of Applied Physics, 2004 Spring Meeting

Modeling of $1/f$ Noise with HiSIM for 100nm CMOS Technology

Representative Hiroaki Ueno (Res. Asso. Graduate School of Advanced Sciences of Matter)
Cooperator Mitiko Miura-Mattausch (Prof., Graduate School of Advanced Sciences of Matter)

Abstract

A new $1/f$ noise model of MOSFETs for circuit simulation valid down to 100nm technology has been developed. The main feature of the model is inclusion of the carrier density distribution along the channel. The model is implemented into the circuit simulation model HiSIM based on the drift-diffusion approximation. It was proved that only one gate-length-independent model-parameter, the trap density, is sufficient to reproduce all measured $1/f$ noise characteristics.

1 Introduction

Accurate prediction of $1/f$ noise characteristics is becoming increasingly important for RF applications of MOSFETs, because the low-frequency $1/f$ noise affects for example the high frequency phase noise through upconversion [1].

The origin of the conventional $1/f$ noise in MOSFETs has been explained theoretically by a fluctuation in the number of channel carriers by trapping/detrapping processes at the oxide interface [2] and by a fluctuation in mobility [3]. However, shortcomings of existing $1/f$ noise models for circuit simulations are that they can hardly reproduce the strong gate length (L_g) dependence as well as the complicated bias dependence with a single model equation. The measured $1/f$ noise was found to exhibit the large increase of noise by reducing the gate length, which is stronger channel length dependence than predicted by the conventional $1/LW$ linear relationship [4].

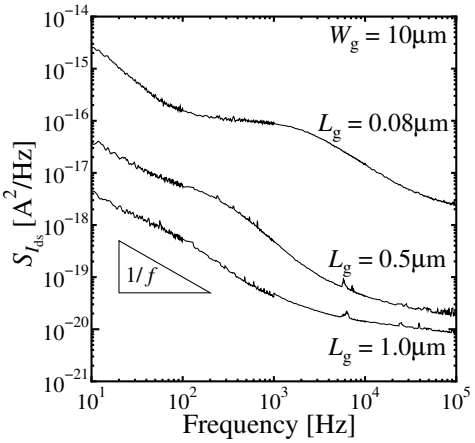

Fig. 1: Drain current noise of n-MOSFET with different gate length (0.08, 0.5 and 1.0μm) under linear condition.

Thus, our objective is to develop the $1/f$ noise model for circuit simulation valid for all gate lengths with a single parameter set. The model will be demonstrated to meet required accuracy for any bias conditions and gate lengths with a single model parameter set.

2 Analysis of Measured $1/f$ Noise Characteristics

The $1/f$ noise spectrum is obtained by assuming uniform trap density and energy distribution in the oxide layer [2]. However, as device size reduces, measured low-frequency noise strongly departs from the $1/f$ dependence as shown in Fig. 1. This means that the trap density and energy distribution is spatially non-uniform in the oxide layer [5, 6]

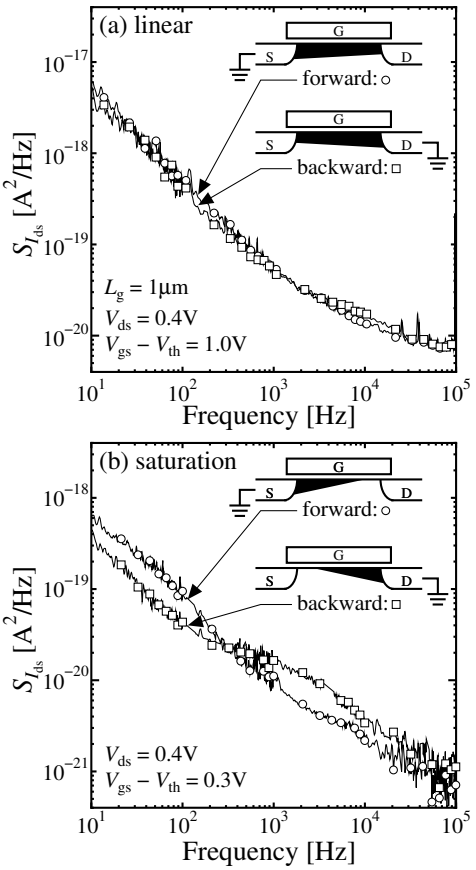

Fig. 2: Comparison of drain current noise spectrum density between forward measurement and backward measurement under (a) linear and (b) saturation condition for L_g = 1.0μm. The insets show schematics of the inversion charge distribution in the forward and backward measurement.

especially in smaller scale devices [7, 8]. Thus, the spatial distribution of the trap density determines the noise feature.

Figs. 2a and 2b show measured noise spectra under the linear and saturation conditions, respectively, for a gate length (L_g) of 1.0μm. The measurements with exchanged source (forward) and drain (backward) contacts are compared in the figures. The carrier density distribution along the channel is schematically depicted for each condition. Under the linear condition the difference in the noise spectra between the forward and backward measurement is hardly observed. On the contrary, the difference becomes clear under the saturation

condition. However, no difference in the measured drain current is observed by the exchange. This concludes that the measured characteristics in Figs. 2a and 2b are due to the position dependent trap density and energy along the channel direction, in which the drain current is insensitive.

The Lorentzian noise is described

$$S_{I_{ds}} = \frac{A\tau}{1 + (2\pi f\tau)^2} \tag{1}$$

where A is a magnitude of the Lorentzian noise determining the trap density, and τ is a time constant of the carriers in the generation-recombination process, determined by the position in the depth direction of the oxide layer [2, 9]. The calculation result with Eq. (1) is shown in Fig. 3 together with measurement [10]. Under the linear condition, the carrier concentration is rather homogeneous along the channel. Therefore, all trap sites along the channel causing the Lorentzian noise contribute on the noise characteristics for both the forward and backward cases, resulting in a nearly diminished difference in the measured noise spectra. On the contrary, the pinch-off condition occurs under the saturation condition, and the carrier distribution along the channel becomes inhomogeneous.

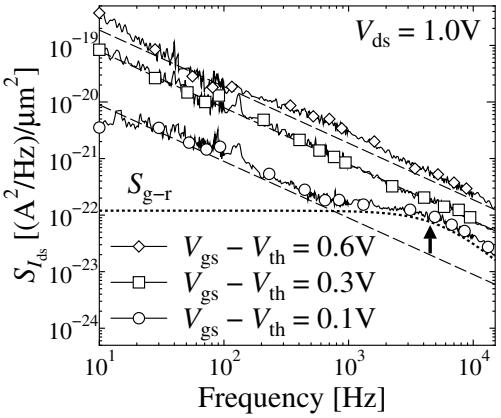

Fig. 3: Measured drain current noise power spectra $S_{I_{ds}}$ versus frequency for various $V_{gs} - V_{th}$ values. Three dashed lines represent ideal $1/f$ spectra and the dotted line is the result fitted with Eq. (1).

neous.

Figs. 4a and 4b show the same measurement as Figs. 2a and 2b but for $L_g = 0.12\mu$m case. The difference in the forward and backward noise measurements under the saturation condition is enhanced. The reason is that the contribution of each inhomogeneous trap site on the noise characteristics is enhanced due to the reduced gate length. There is again no distinguishable difference in the measured drain current identical for the forward and the backward measurement of the $L_g = 1.0\mu$m case.

The above investigation proved that the non-$1/f$ noise is due to the non-uniform trap density. Thus, by averaging the noise spectra over chips on a wafer, it is expected that the noise reduces to the $1/f$ characteristics [11]. Fig. 5 shows measured noise spectra of about 30 different chips on a wafer for $L_g = 0.46\mu$m at $f = 100$Hz. The average of all these

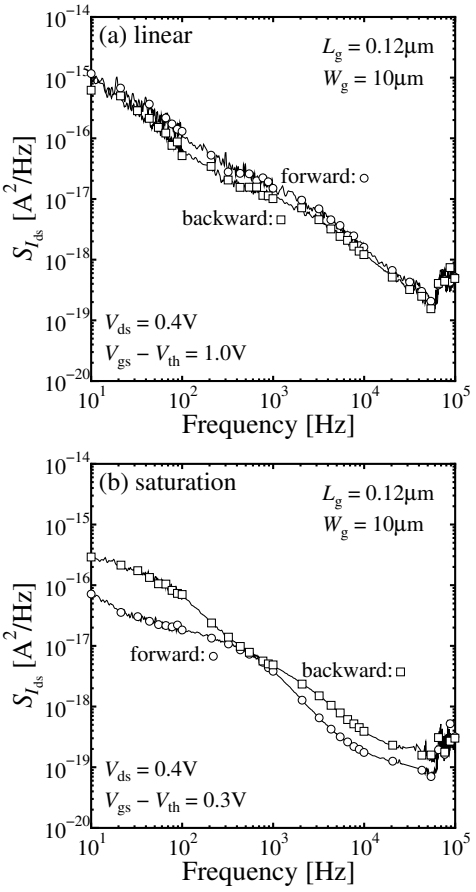

Fig. 4: Comparison of drain current noise spectrum density between forward measurement and backward measurement under (a) linear and (b) saturation condition for $L_g = 0.12\mu$m.

noise spectra exhibits really the $1/f$ noise characteristics as shown by a thick line. This concludes that trap sites causing the Lorentzian noise spectra distribute randomly on a wafer as can be seen from the Gaussian distribution of the noise spectrum density at $f = 100$Hz shown in Fig. 6. Thus as a circuit-simulation model it is a subject to describe only this averaged $1/f$ noise characteristics with boundaries as the worst and the best case.

3 Model Description

The general expression for the $1/f$ noise power spectrum density of a MOSFET ($S_{I_{ds}}$) [2, 12] has a position-integral part of the inversion-charge density ($N(x)$) along the channel direction x

$$S_{I_{ds}}(f) = \frac{I_{ds}^2 N_{trap} kT}{L^2 W q f} \int_0^L \left(\frac{1}{N(x) + N^*} \pm \alpha\mu \right)^2 \mathrm{d}x \tag{2}$$

$$N^* = \frac{kT}{q^2}(C_{ox} + C_{dep} + C_{it}) \tag{3}$$

where k is the Boltzmann constant, T is the lattice temperature, L is the channel length, W is the channel width, q is the electron charge, μ is the carrier mobility, C_{ox} is the gate oxide capacitance and C_{dep} is the depletion layer capacitance. The model parameters N_{trap} ($= N_t/\gamma$), α and C_{it} are the ratio

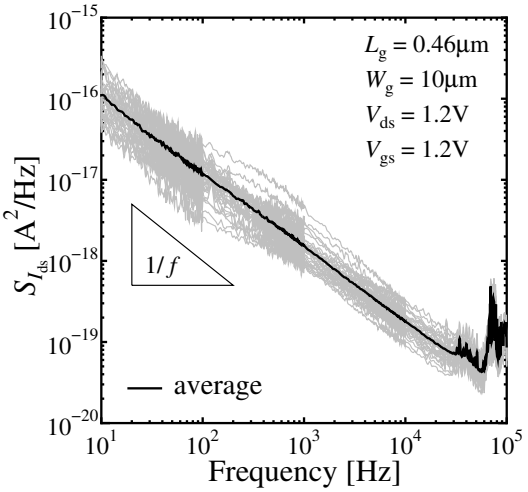

Fig. 5: Measured drain current noise spectra of about 30 devices with the same size under the same bias condition on a wafer. The fat curve represents an averaged noise spectrum.

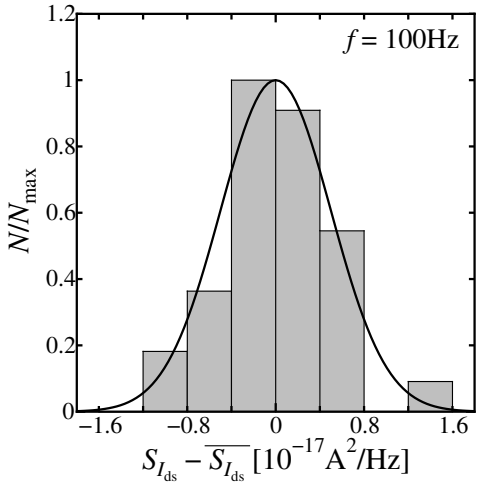

Fig. 6: Histogram of measured drain current noise spectra at 100Hz. The curve shows the normal distribution function. $\overline{S_{I_{ds}}}$ is about 1.0×10^{-17}A^2/Hz.

of trap density (N_t) to attenuation coefficient into the oxide γ, the contribution coefficient of the mobility fluctuation and the capacitance caused by the interface trapped carriers, respectively. To develop an precise $1/f$ noise model, therefore, not only the current I_{ds} itself, but also the position dependent carrier concentration along the channel $N(x)$ is necessary. Our new $1/f$ noise model is linked with the circuit simulation model HiSIM [13], based on the drift-diffusion approximation [14]. HiSIM provides the carrier concentrations at the source N_0 and drain side N_L determined by surface potentials consistently. Beyond the pinch-off point under the saturation condition the carrier concentration becomes negligibly small, thus the integration in Eq. (2) is done from ϕ_{s0} to ϕ_{sL}. Thus, our description of the $1/f$ noise spectrum density is

$$S_{I_{ds}}(f) = \frac{I_{ds}^2 N_{trap} kT}{L^2 W q f} \int_{\phi_{s0}}^{\phi_{sL}} \left(\frac{1}{N(\phi) + N^*} \pm \alpha v \right)^2 d\phi \quad (4)$$

In Eq. (4) the mobility μ is replaced by v of the second term in the parenthesis of the right-hand side of Eq. (2). The reason is that the field increase along the channel has to be considered together with the mobility distribution. In order to perform the integration analytically an assumption is applied. Namely, $N(x)$ is linearly decreasing from N_0 to N_L. This can be verified with two-dimensional simulation results with MEDICI [15] in Fig. 7. For the two-dimensional simulation the impurity profile was extracted by the inverse modeling from measured current-voltage characteristics. It is seen that the linear approximation of $N(x)$ is applicable for any bias conditions.

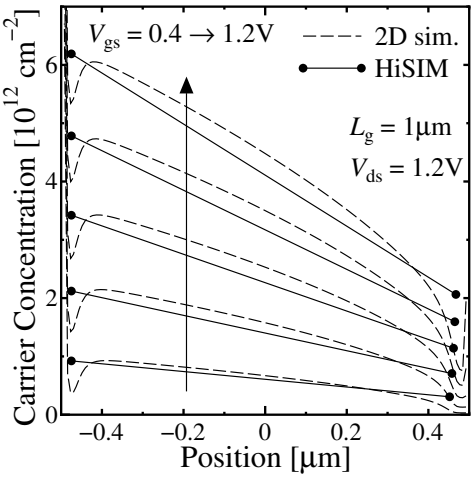

Fig. 7: The inversion-charge density at the source N_0 and drain side or pinch-off point in saturation condition N_L calculated by HiSIM. The position dependence of $N(x)$ calculated by two-dimensional device simulator is also depicted.

The validity of the exclusion of the channel region beyond the pinch-off point is proved here. In the pinch-off region carriers loose the gate voltage control and number of carriers reduces drastically. Thus, diminished trapping/detrapping process is expected due to diminished collision with the interface. Fig. 8 shows the simulated number of channel electrons colliding with the oxide interface per unit time by the Monte Carlo simulator FALCON [16] as a function of position along the channel [10]. The FALCON includes all scattering mechanisms important for MOSFETs with a full-energy-band structure. Thus, the diminished noise power arises from the pinch-off region and L in Eq. (2) can be replaced by $L - \Delta L$ where ΔL is the length of the pinch-off region [17].

The final analytical equation of the $1/f$ noise, valid for all bias conditions, is derived

$$S_{I_{ds}}(f) = \frac{I_{ds}^2 N_{trap} kT}{(L - \Delta L) W q f} \left\{ \frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\alpha v}{N_L - N_0} \log\left(\frac{N_L + N^*}{N_0 + N^*} \right) + (\alpha v)^2 \right\} \quad (5)$$

where N_{trap} is the model parameter, and N_0 and N_L are calculated by HiSIM.

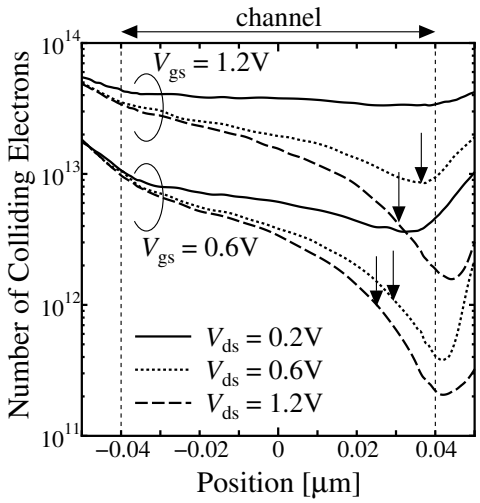

Fig. 8: Monte Carlo simulation result for number of electrons colliding with the oxide interface per unit time as a function of position along the channel for $L_g = 0.12\mu$m. The vertical arrows indicate pinch-off points.

4 Calculation Results

Fig. 9 shows the measured V_{gs} dependence of $S_{I_{ds}}$ of n-MOSFETs for different V_{ds} values with $L_g = 1.0$, 0.46 and 0.12μm at $f = 100$Hz by symbols. All measured points are average values over 30 samples on a wafer. Calculated results with our model are also shown by solid curves. It is seen that the bias dependences of the noise characteristics for all channel lengths are well reproduced with a single model-parameter set. Fig. 10 shows the measured V_{ds} dependence of $S_{I_{ds}}$ of n-MOSFETs for different V_{gs} values. Among three model parameters (N_{trap}, α, C_{it}), two parameters (α and C_{it}) were extracted to be negligibly small. And only L_g independent N_{trap} is responsible for the measured $1/f$ characteristics.

The dotted curves in Fig. 9 are calculated results with averaged $N(x)$ in the channel (N_{ave}) instead of the integration explicitly as shown below:

$$S_{I_{ds}}(f) = \frac{I_{ds}^2 N_{trap} kT}{(L-\Delta L)Wqf}\left\{\frac{1}{N_{ave}+N^*}+(\alpha v)\right\}^2 \qquad (6)$$

It is seen that the results with N_{ave} cannot reproduce the bias dependences of the $S_{I_{ds}}$ for all channel lengths with a single model-parameter set. Especially the noise enhancement for larger V_{ds} is not well reproduced. Thus, we can conclude that the position dependence of the carrier concentration plays an important role for the $1/f$ noise characteristics. For the successful prediction of the $1/f$ noise characteristics, the measured I–V characteristics have to be accurately simulated, since N_0 and N_L are important origin of the complicated bias dependent $1/f$ noise. To verify the role of our argument, we compare the V_{ds} dependence of the drain current noise (solid curves) and square of drain current (dotted curves) in Fig. 11. Roughly, the $1/f$ noise characteristics are governed by the I_{ds}^2 characteristics. However, clear deviations between two are observed. Especially, the $S_{I_{ds}}$–V_{ds} characteristics in linear condition are different from the I_{ds}–V_{ds} characteristics. In linear condition, terms of N_L cannot be negligible in Eq. (5). Thus, the bias dependence of the $1/f$ noise is due to not only the I–V characteristics but also the bias dependence of N_0 and N_L.

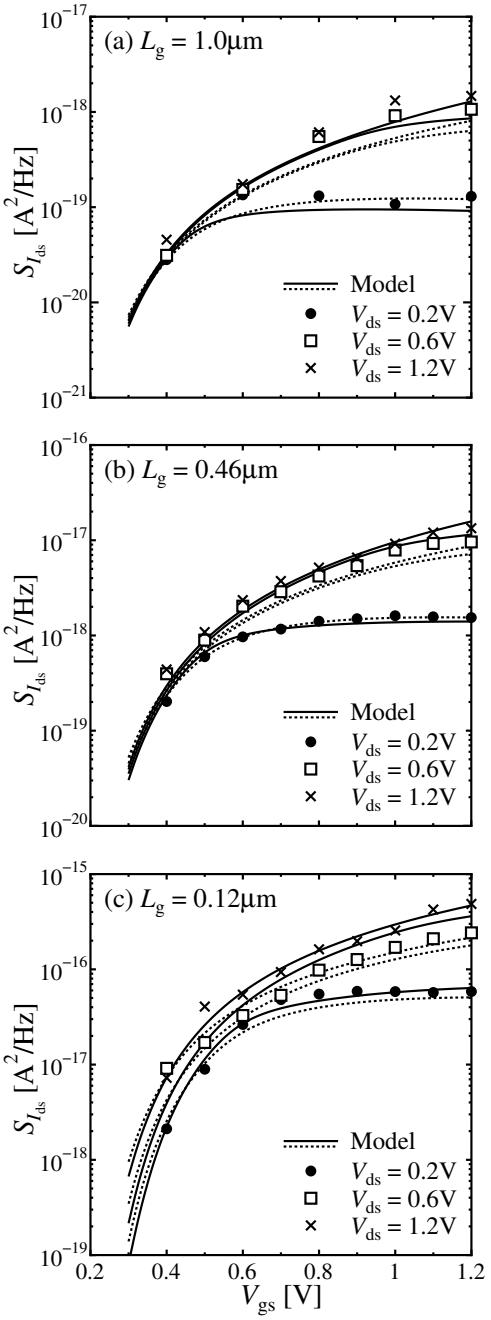

Fig. 9: Comparison of the V_{gs} dependence of the measured and simulated drain current noise by our model for (a) $L_g = 1.0\mu$m, (b) 0.46μm and (c) 0.12μm at frequency 100Hz. Model parameter values are the same for all L_g values. Dotted curves represent calculated results with N_{ave} instead of N_0 and N_L.

Fig. 12 shows the device area LW dependence of measured $S_{I_{ds}}$ normalized by I_{ds}^2 at $f = 100$Hz, where W_g is fixed to 10μm. The well-confirmed $1/LW$ dependence is still preserved for 100nm-MOSFETs. However, the deviation from the linear relationship is observed beyond $L_g = 0.14\mu$m. The

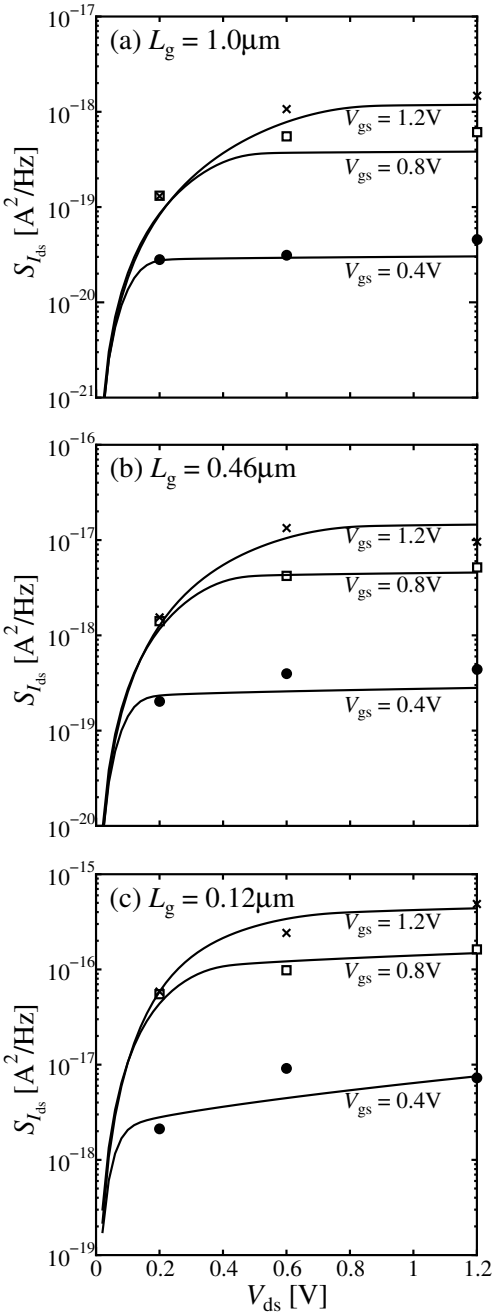

Fig. 10: Comparison of the V_{ds} dependence of the measured and simulated drain current noise by our model for (a) L_g = 1.0μm, (b) 0.46μm and (c) 0.12μm at frequency 100Hz.

enhancement is attributed to the high-field effects becoming more pronounced for smaller L_g. It is seen in Fig. 9 that the present model is valid even for such case.

5 Conclusion

We have demonstrated that the non-$1/f$ noise characteristic is caused the inhomogeneous trap density distribution along the channel. Averaged noise spectra on a wafer reduces to the $1/f$ characteristic, which is suitable for the modeling. A new $1/f$ noise model for circuit simulation based on the drift-diffusion approximation, reproduces the bias and L_g dependence of the averaged noise spectrum with only three model parameters. Practically only one model parameter is responsible for describing the measured $1/f$ characteristics.

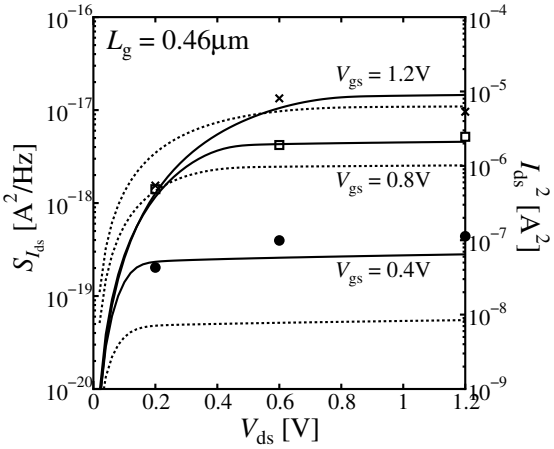

Fig. 11: Comparison of the V_{ds} dependence of the measured and simulated drain current noise (solid curves) and square of drain current (dotted curves).

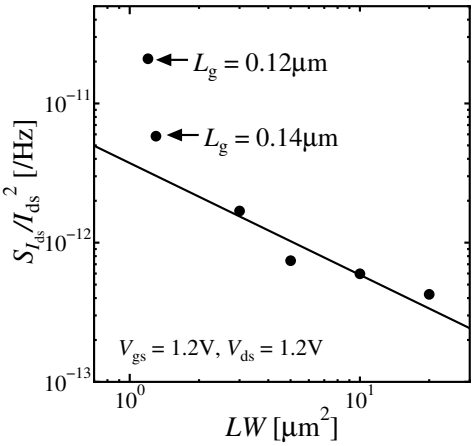

Fig. 12: Measured drain current noise power spectrum density $S_{I_{ds}}$ normalized by I_{ds}^2 vs. gate area LW. The solid line is the $1/LW$ linear relationship.

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6 Published Papers and Patents

Published Papers

1. M. Tanaka, H. Ueno, O. Matsushima, and M. Miura-Mattausch, "High-Electric-Field Electron Transport at Silicon/Silicon-Dioxide Interface Inversion Layer," Jpn. J. of Appl. Phys.," **42**, pp. L280–L282, (2003).

2. N. Nakayama, H. Ueno, T. Inoue, T. Isa, M. Tanaka, and M. Miura-Mattausch, "A Self-Consistent Non-Quasi-Static MOSFET Model for Circuit Simulation Based on Transient Carrier Response," Jpn. J. of Appl. Phys., **42**, pp. 2132–2136, (2003).

3. M. Miura-Mattausch, H. Ueno, H. J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, "100nm-MOSFET Model for Circuit Simulation: Challenges and Solutions (Invited)," IEICE Transactions on Electronics, **E86-C**, pp. 1009–1021, (2003).

4. N. Nakayama, D. Navarro, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, T. Kage, and S. Miyamoto, "A Non-Quasi-Static Model for MOSFET Based on Carrier-Transit Delay," IEE Electronics Letters, *in print*.

5. S. Hosokawa, D. Navarro, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, T. Kage, and S. Miyamoto, "Universal Thermal-Drain-Noise Prediction from Threshold Voltage," IEEE Electron Device Letters, *in print*.

Proceedings

1. T. Mizoguchi, H. J. Mattausch, H. Ueno, D. Kitamaru, K. Hisamitsu, M. Miura-Mattausch, S. Itoh, and K. Morikawa, "Extraction of Inter- and Intra-Chip Device-Parameter Variations with a Differential-Amplifier-Stage Test Circuit," Workshop on Synthesis and System Integration of Mixed Information Technologies, (2003).

2. O. Matsushima, M. Tanaka, H. Ueno, K. Hara, K. Konno, and M. Miura-Mattausch, "Carrier Transport in Highly Generated Carrier Concentration," 13th International Conference on Nonequilibrium Carrier Dynamics in Semiconductors, (2003).

3. S. Hosokawa, Y. Shiraga, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, H. Masuda, and S. Miyamoto, "Investigation of Enhanced Thermal Noise for 100nm-MOSFETs," International Conference on Solid State Devices and Materials, (2003).

Analysis and Modeling of Carrier Transport in Photodiodes

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1. Research Target

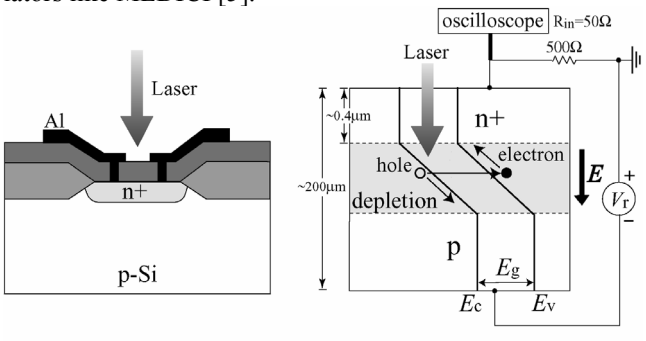
Device dimension in LSI is continuously being reduced to obtain high integration and high frequency operation. However, interconnection propagation delay using metal interconnects overwhelms transistor gate delay [1]. This impedes realization of fast switching circuit operation. Under such a situation, optical interconnection becomes an attractive option [1], which involves light emitting devices, optical waveguide and photodetectors. In order to design optoelectronic integrated circuits (OEICs), models describing the electronic and optical characteristics of optoelectronic devices for circuit simulation become a necessity. To model such characteristics correctly, physical understanding of carrier transport in optoelectronic devices is necessary. In this research work, we focus on the photodiode as an optoelectronic device. We investigated carrier transport characteristics in photodiode and developed an analytical model necessary for high frequency operation [2,3,4].

2. Research Results

2.1 Carrier Transport Feature in Photodiodes at High illumination

In our recently published works [2,3], we investigated the photoresponse of a Si *p-n* photodiode both experimentally and theoretically.

For the theoretical approach, two numerical calculation methods are generally considered. One is the Monte-Carlo simulation, and the other is to solve consistently the closed system of equations composed of the Poisson equation, the continuity equation, and the current-density equation based on the drift-diffusion (DD) approximation. Since the former simulates the transport of each carrier, it needs a very long computational time. On the other hand, as for the latter, the computational cost is significantly reduced because the complexity of microscopic processes is eliminated by introducing the mobility parameter. Therefore, this method is very practical and widely adopted in commercial 2-dimensional device simulators like MEDICI [5].



(a) (b)

Fig 1 (a) Structure of the *p-n* photodiode. (b) Schematic of the experimental setup.

In the DD approximation, the most important factor is mobility, because a correct solution for carrier transport can be obtained for an appropriate mobility model. We note that the condition for the DD approximation is realized in quasi-equilibrium situations. In the photodiode, however, such quasi-equilibrium situations are not exactly true, but rather a fully non-equilibrium condition is expected since reverse bias is applied. Therefore, it is important to clarify the condition when the DD approximation is applicable in investigating the photodiode response.

We performed an experiment as shown in Fig. 1 using a fabricated Si *p-n* photodiode and a 532nm-pulsed laser with pulse duration of ~1ns FWHM. The left-hand side in Fig. 2 shows the measured photocurrents. We also reproduced the results shown in the right-hand side in Fig. 2, using MEDICI [5] under the same condition as the experiment. At low laser intensity, the experimental results coincide well with those obtained by using the simulator. On the contrary, at high laser intensity, we find appreciable discrepancy in the signal waveforms between the experiment and the simulation. It is very interesting to note that the results obtained by MEDICI show plateau-like forms. The plateaus cannot be eliminated even if the mobility model in the simulation is changed.

We concluded via order estimates that the cause of the plateau is due to the space charge limitation effect [6]. The DD approximation is implicitly assumed for the derivation of the conventional space-charge-limited current [6]. This result means that the DD approximation is not precise for the case of high photo-generated carrier density with low reverse bias. Furthermore, our conclusion is proved by numerical calculations for carrier dynamics inside the device.

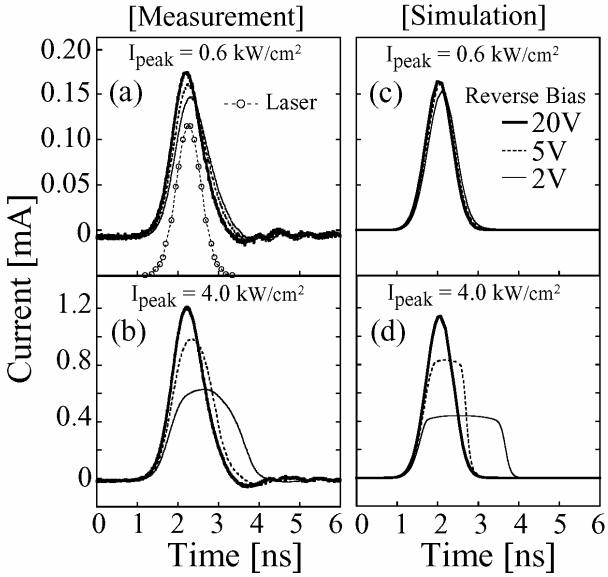


Fig 2 Comparison between measurement and numerical simulation by MEIDCI.

From this work, we suggested a necessity of a modifying mobility models in order to simulate the photodiode response more accurately in the framework of the DD approximation.

2.2 Modeling of Carrier Transport in Vertical *p-i-n* Photodiodes

In order to design OEICs, accurate physics-based models describing the characteristics of optoelectronic devices are necessary. One such device is the *p-i-n* photodi-

ode, which has been generally investigated using two approaches: full numerical approach [7] and analytical approach [8]. For models employed in circuit-simulation, the latter is more appropriate because the computational time is considerably reduced, and thus adopted here.

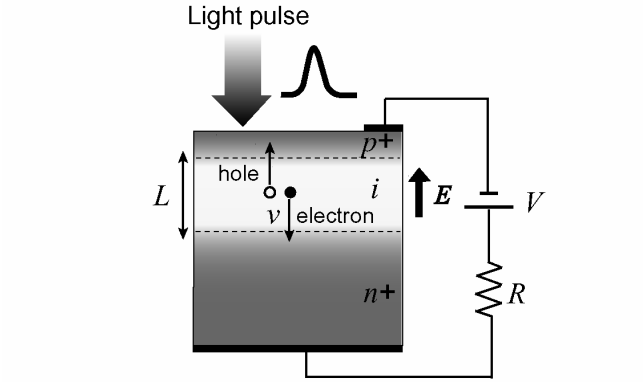


Fig 3 Structure of the vertical *p-i-n* photodiode.

We particularly investigated a vertical *p-i-n* photodiode as shown in Fig. 3. The high frequency response of the photodiode is mainly limited by three factors: (1) drift transit time for carriers to cross *i*-region, (2) *RC* constant, (3) diffusion time. The first and second factors are discussed precisely in Ref. [8]. However, the third factor is often neglected in analytical formulations and its effect on high frequency response is not investigated yet. The diffusion becomes dominant and determines the cut-off frequency in certain cases (see Ref. [4] for details).

In our recent paper [4], we presented a consistent formulation for the current characteristics of the vertical *p-i-n* photodiode by taking into account the carrier diffusion generated in the n^+ or p^+ region. Furthermore, we developed a simulation scheme based on the spectral method [9] to express photocurrent in time domain. In spite of significant reduction in calculation time, accuracy of our calculation results is comparable to those of the conventional 2-dimensional numerical device simulator MEDICI as shown in Fig. 4. Our formulation is very easy to use and compatible especially to the harmonic balance simulation [10] of circuits. Therefore, our result is very useful in performing circuit simulation of OEICs.

3. Summary

We investigated the photoresponse of *p-n* photodiodes at high illumination and elucidated carrier transport characteristics which cannot be described by present mobility models. A necessity of modifying present mobility models is suggested [2,3]. Furthermore, we developed a model of carrier transport in the vertical *p-i-n* photodiode, which has a computational accuracy comparable to a 2-dimensional device simulator [4]. Our model is very useful in performing circuit simulation of OEICs.

4. Future Work

Future research work will consider the lateral-type *p-i-n* photodiode. This type has a high responsivity since light absorption length should no longer be considered during operation. Moreover, the technology is compatible with VLSI processes. At present, we are developing a model for describing the carrier transport feature in this type of photodiode. Moreover we are planning to realize circuit simulation of OEICs with such photodiodes.

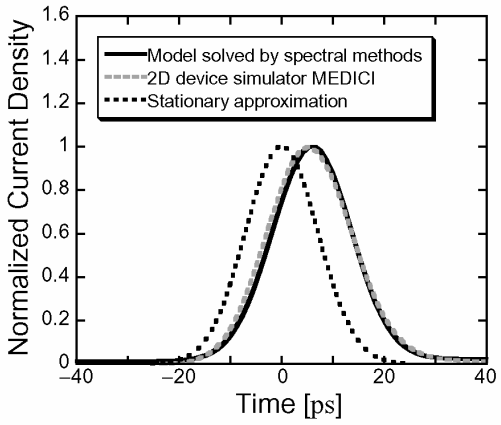


Fig 4 Accurate calculation of the photocurrent using the developed model.

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5. Papers and Presentation

5.1 Refereed Journals

1. O. Matsushima, K. Konno, M. Tanaka, K. Hara, M. Miura-Mattausch, "Carrier Transport in Highly Generated Carrier Concentration", Semicond. Sci. Tech. **19**, S185 (2004)
2. K. Konno, O. Matsushima, D. Navarro, M. Miura-Mattsusch, "Limit of Validity of the Drift-Diffusion Approximation for Simulation of Photodiode Characteristics", Appl. Phys. Lett. **84**, 1398 (2004)
3. K. Konno, O. Matsushima, D. Navarro, M. Miura-Mattsusch, "High-Frequency Response of *p-i-n* Photodiode Analyzed by an Analytical Model in Fourier Space", Submitted to J. Appl. Phys.

5.2 Presentation

1. K. Konno, O. Matsushima, K. Hara, G. Suzuki, M. Miura-Mattausch, "Modeling of Photoresponse of *p-i-n* Photodiodes and Current Simulation based on the Spectral Method", Japan Society of Applied Physics, 2004 Spring Meeting.

To Improve HiSIM-SOI for Real Application

Muhibul Haque Bhuyan (COE Researcher),
Mitiko Miura-Mattausch (Prof., Graduate School of Advanced Sciences of Matter)

1. Research Target

SOI-MOSFET is a candidate for next generation integrated circuit technology due to its reduced junction capacitances and improved subthreshold swing. However, to utilize the technology for circuit application, a robust circuit model is needed. A complete surface-potential based fully depleted SOI-MOSFET model for circuit simulation has been developed by our group and is named HiSIM-SOI [1, 2]. This model considers device features explicitly as well as preserves the charge conservation. To improve HiSIM-SOI for real application is the purpose of this present work.

2. Research Results

One problem focusing now is the influence of bulk oxide thickness on the device performances. The bulk oxide thickness has the effect on body effect factor and in turn on threshold voltage. If the thickness of bulk oxide is very thin then the body effect factor increases. But this increased body effect factor increases the parasitic capacitance between the drain and substrate as well as drive current is degraded mainly due to vertical electric field.

The effect of the bulk oxide thickness and the bulk impurity concentration has been analyzed for fully depleted SOI-MOSFET. Besides, Drain Induced Barrier Lowering (DIBL) effect of SOI-MOSFET has also being investigated. The investigation is done with the 2D device simulator MEDICI. Results are shown in Figs. 1-3. Figs. 4-6 show simulation results characterizing the body effect factor.

3. Summary

The DIBL as well as the body effect factor are found to be very sensitive to device parameters, such as the bulk oxide thickness.

4. Future Plan

The simulation study will be analyzed to develop models describing the phenomena.

References

[1] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch, “Complete Surface-Potential-Based Fully-Depleted Silicon-0n-Insulator Metal-Oxide-Semiconductor Field-Effect-Transistor Model for Circuit Simulation,” Jap, J. Appl. Phys., 43, pp. 2166-2169, 2004.

[2] N. Sadachika, Y. Uetsuji, D. Kitamaru, H. J. Mattausch, M. Miura-Mattausch, L. Weiss, U. Feldmann, and S. Baba, “Fully-Depleted SOI-MOSFET Model for Circuit Simulation and Its Applications to 1/f Noise Analysis,” Proc. Simulation on Semiconductor Processes and Devices, 2004.

Fig.1: Tsoi and Tbox dependence

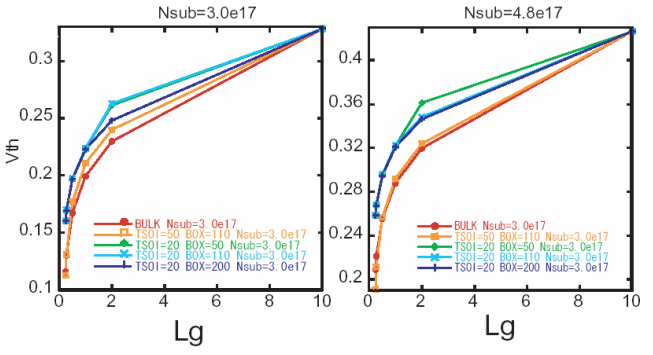


Fig.2: impurity-concentration dependence

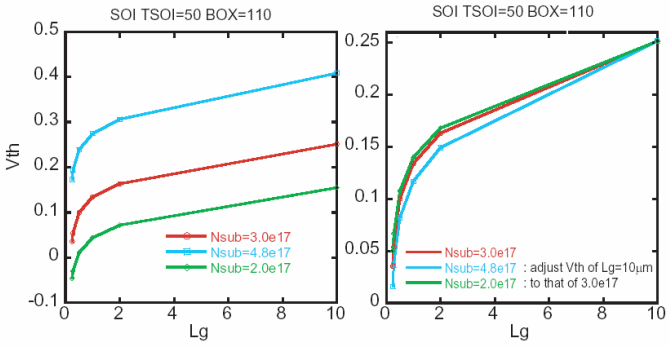


Fig.3: impurity-concentration dependence

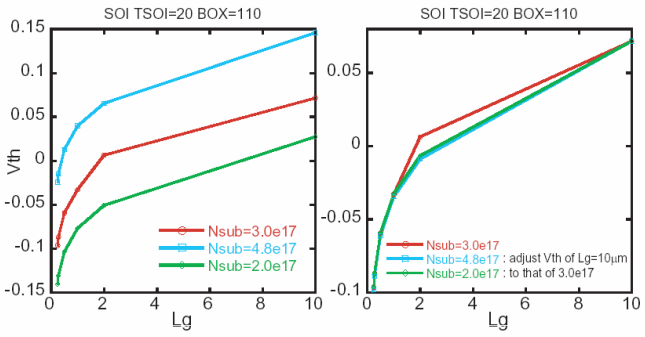


Fig.4: Vth-Vbs characteristics-1

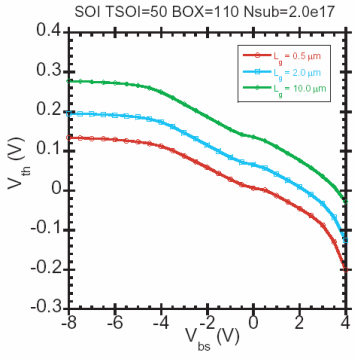


Fig.5: Vth-Vbs characteristics-2

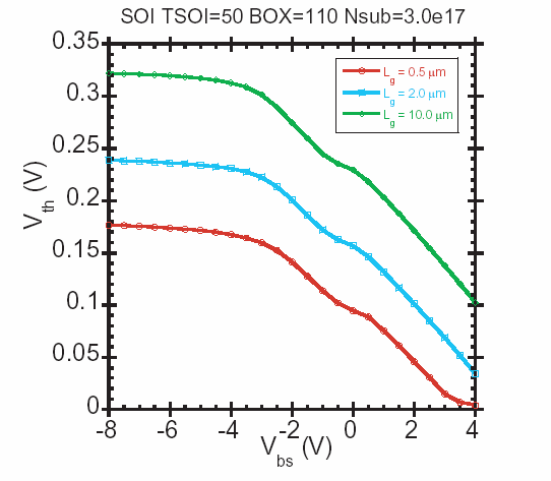
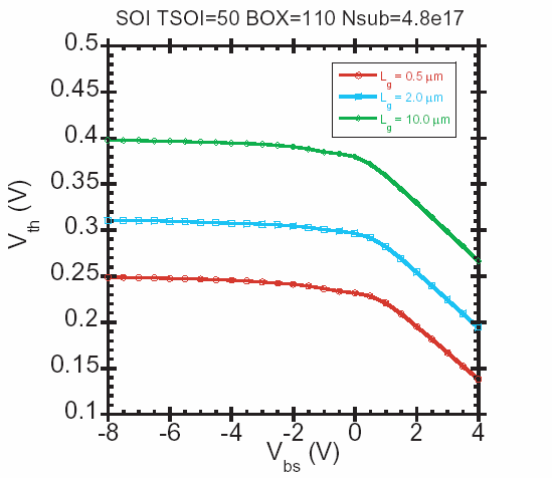


Fig.6: Vth-Vbs characteristics-3



4-III. Nanodevices and Processing

Workfunction Tuning for Single-Metal Dual-Gate CMOS

Representative Kentaro Shibahara (Assoc. Prof., Research Center for Nanodeivices and Systems, Graduate School of Advanced Sciences of Matter)

Cooperator Kousuke Sano (Graduate School of Advanced Sciences of Matter, M1), and Masaki Hino (Graduate School of Advanced Sciences of Matter, M2)

1. Research Target

Dual-workfunction gates with single metal are expected to replace dual-poly-Si gates that accompanies a depletion effect problem. Our target is finding flexible metal-gate workfunction-tuning technology that is applicable to CMOS fabrication maintaining compatibility to conventional CMOS fabrication process.

2. Research Results

Original workfunction tuning of Mo was achieved by nitrogen implantation [1], however, this method causes interface and oxide damage. To avoid the damage problem,nitrogen diffusion from TiN deposited on Mo was attempted. Though expected V_{th} shift due to the N diffusion was 0.45 V that is equal to V_{FB} shift of MOS diodes, the V_{th} shift of fabricated MOSFETs was 0.1 V, as shown in Fig. 1. Nitrogen depth profiles in Mo MOS structure was evaluated to discuss reason why the V_{th} shift was shrunk (Fig. 2). N pileup at the Mo/SiO_2 interface for the diode process reduces by adding source and drain (S/D) activation annealing, in other words, by changing fabrication process to FET process. Nitrogen concentration in Mo was also decreased by the annealing. These results indicate that the nitrogen pileup reduction due to the nitrogen out-diffusion through a Mo film is the origin of reversible workfunction behavior. In the case of the fabricated MOSFETs, Mo gates are surrounded by CVD grown SiO_2 during the S/D activation annealing. N atoms located at the Mo/gate SiO_2 interface are considered to redistribute to other CVD SiO_2 interfaces, as shown in Fig. 3. Based on these results we have modified nitrogen diffusion process to be combined with S/D activation annealing by maintaining a TiN/Mo stack structure to cover the Mo top interface with diffusion source TiN. As a result, the V_{th} shift value was improved, as shown in Fig.4. However, Fig. 4 shows anomalous V_{th} increase behavior for modified devices against the gate length. The Vth increase is attributable to nitrogen reduction at the Mo bottom interface in the short channel devices. Around the gate edge region, some of nitrogen atoms supplied from TiN go to the bottom interface and others go to the side interface. Therefore, nitrogen concentration at the bottom interface around the gate edge is lower than that

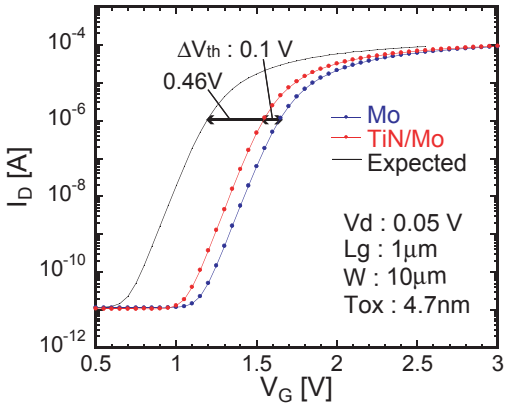


Fig. 1 I_D-V_G characteristics of TiN/Mo and Mo gate MOSFETs. Vth shift due to workfunction change is smaller than the value expected from VFB obtained with MOS diodes.

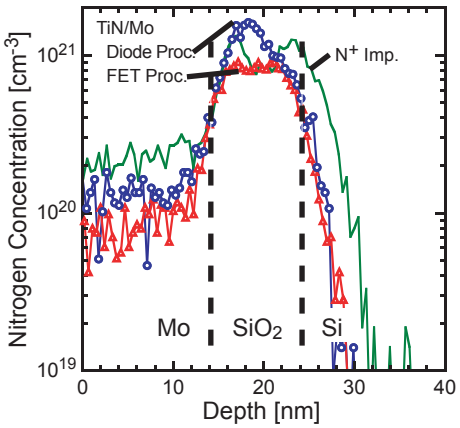


Fig. 2 Nitrogen depth profiles obtained by back-side SIMS technique. Nitrogen pileup formed at the Mo/SiO2 interface reduces by the FET-like process that includes an RTA step after TiN stripping for S/D activation.

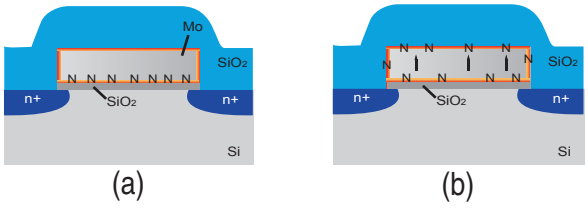


Fig. 3 Nitrogen re-distribution during Mo-gate MOSFET fabrication. (a) befor and (b) after S/D activation annealing.

at gate center. By this short channel device shows smaller workfunction shift, that is smaller V_{th} shift.

In addition to Mo, we are evaluating other materials. Workfunction shift of fully silicided poly-Si gate with Ni, in other words, NiSi gate is recently reported [2,3]. Impurities implanted into the poly-Si gate prior to the silicidation, are swept out towards the oxide interface by snowplow effect. As a result, impurity pileup is formed at the NiSi/SiO_2 by full silicidation of poly-Si (Fig. 5). We have investigated how silicidation condition affects the workfunction shift and the pileup formation with Sb. Sb depth profiles shown in Fig. 6 indicates that Sb pileup is larger for lower silicidation temperature. By lowering silicidation temperature, silicidation rate is also lowered. The snowplow effect is considered to be enhanced by slowing down silicidation rate. The amount of the pileup is reflected to V_{FB} shift evaluated with MOS diodes.

3. Summary and future plan

Workfunction tuning utilizing impurity pileup at the metal/SiO_2 interface has been investigated. In the case of N in Mo-gate, MOSFET fabrication process must be modified to reflect workfunction shift oberved with MOS diodes. We are now testing another modification, to suppress the anomalous reverse short channel effect.

In the case of Sb in NiSi gate, silicidation temperature that affects silicidation rate and the snowplow effect was the key to obtain workfunction shift. Referring this results other silicide materials are evaluated to improve the work function tuning technique.

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2. M. Hino, T. Amada, N. Maeda, and K. Shibahara, "Influence of Nitrogen Profile on Metal Workfunction in Mo/SiO2/Si MOS Structure", Ext. Asbst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 494-495, 2003.
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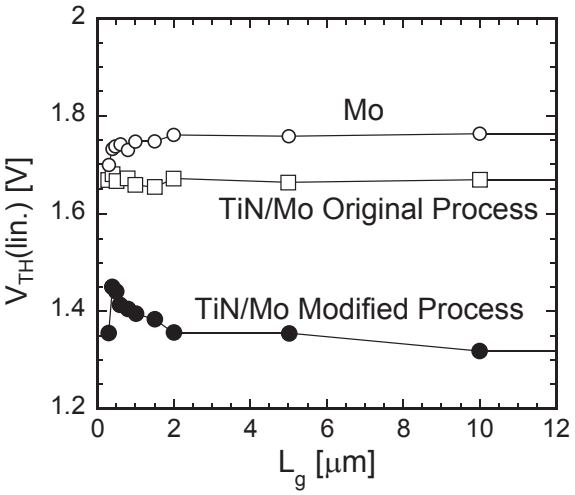

Fig. 4 Relationship between Vth and Lg for Mo gate MOSFETs. Vth was shifted by workfunction shift realized by Nitrogen incorporation into Mo gate.

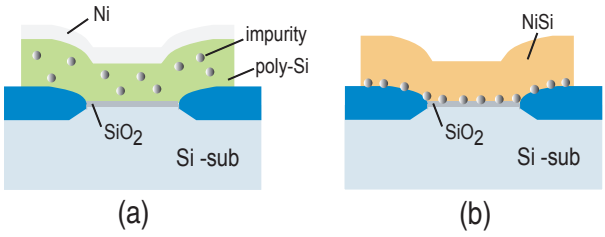

Fig. 5 Pileup formation during NiSi full-silicidation by snowplow effect. (a) before and (b) after full silicidation

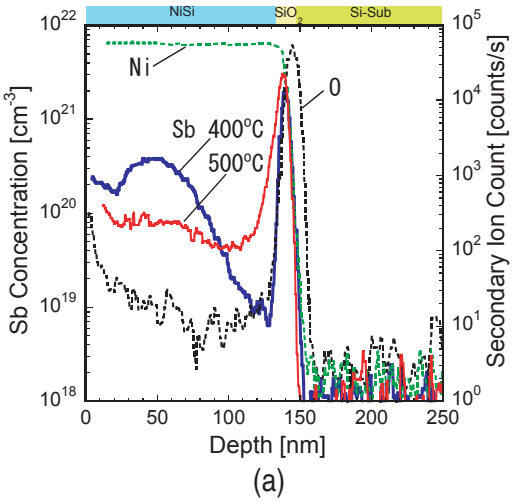

Fig. 6 (a) Sb depth profiles in NiSi-MOS structure obtained with back-side SIMS technique (a) and its closeup around the MOS interfaces. The snowplow effect and pileup formation is prpmoted by lowering silicidation temperature.

Fabrication and Evaluation Technique for Ultra-Shallow Junction

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Cooperator Takanori Eto (Graduate School of Advanced Sciences of Matter, M1), and Eisuke Takii (Department of Enginerring, B4)

1. Research Target

Source and drain junctions have been modified shallower and shallower as the MOSFET scaling progressed. Nowadays, the junction depth must be shallower than 20 nm for leading edge devices. Our primary research target is development of sub-10 nm junctions formation technique and precise evaluation technique for them.

2. Research Results

Short duration annealing is a key to fabricate shallow and low resistive junctions. We have succeeded 10 nm junction formation using KrF excimer laser (248 nm) annealing. In Fig. 1, B depth profiles for junctions with a depth of 9.5 nm are shown. Diffusion during annealing was smaller than 0.2 nm by utilizing short duration pulse laser with FWHM of 38 ns. Usefulness of junction must be discussed referring junction depth and sheet resistance. Even if the junction is shallow enough, high resistive junction degrade MOSFET performance. We have found that sheet resistance can be reduced less than 1 kΩ/sq. by heating a substrate to 450°C. Though Fig. 1 is an example of p^+/n shallow junction formation, n^+/p junction also shallower than 10 nm was achieved using As or Sb as dopant. This heat assist method is also effective for residual defects reduction. Figure 2 shows cross-sectional TEM images after annealing. Without the heat-assist, residual defects similar to Fig. 2(a) are usually observed. By increasing heat assist temperature, defects density was clearly reduced, as shown in Figs. 2(a) and (b). Defect reduction was further enhanced by using Ge pre-amorphization implantation that is useful to suppress long profile tail due to channeling, as shown in Figs. 2(c) and (d). To fabricate shallower junctions, dopant profiles prior to the annealing must be modified shallower. This is usually realized by reducing ion implantation energy. However, in sub-keV regime, junction depth reduction due to the energy reduction shows saturating tendency, as shown in Fig. 3. The mechanism of this tendency is not clear yet.

In addition to KrF excimer laser, we are investigating all-solid-state green laser (532 nm) annealing. All-solid-state lasers have superior equipment size and easiness of maintenance that fit to mass production. However,

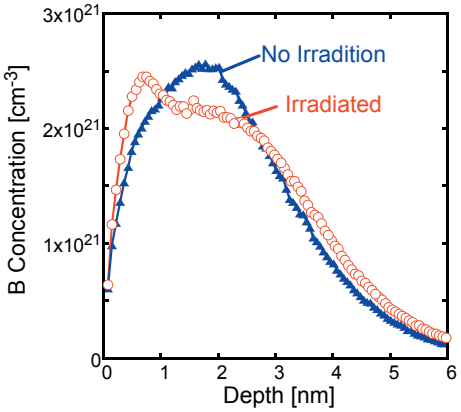

Fig. 1 B depth profiles for (a) before and (b) heat assited laser annealing.

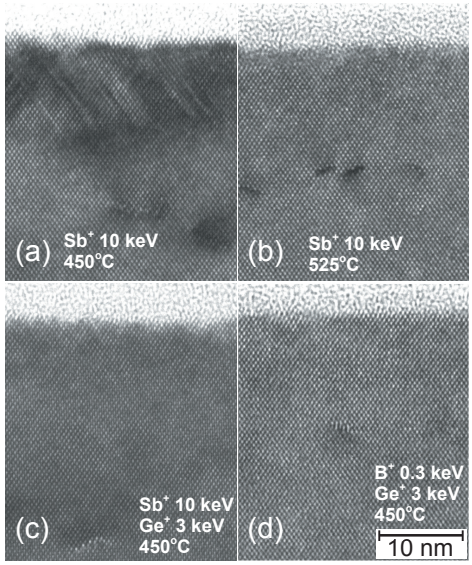

Fig. 2 XTEM photographs to evaluate residual defects after heat-assited laser annealing. Stacking faults seen in (a) are reduced by increasing heat-assist temperature or using Ge pre-amorphization.

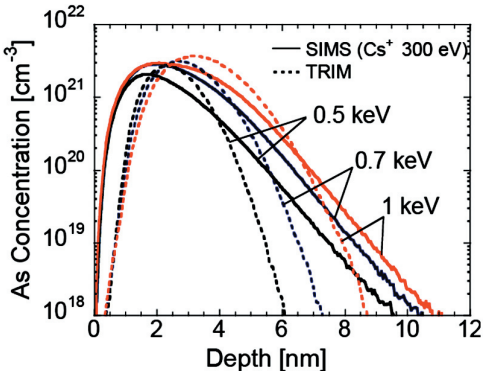

Fig. 3 As implanted As profiles for sub-keV ion implantation.

penetration depth of green light is about 1 μm and much deeper than device dimensions. This leads to wasting power for unnecessary deep area heating and high power laser equipments. Based on such background, green laser annealing utilizing light absorber have been investigated. TiN or Mo was deposited on Si after 2-nm screen oxide formation. Comparison of relationships between sheet resistance and laser energy densities in Fig. 4 showed that TiN light absorber effectively reduced the laser energy density to activate dopant but Mo increased. This result is explained by their optical characteristics. Junction depth fundamentally depended on amorphous layer depth, however, the annealing with the absorber easily lead to overmelt of c-Si (Fig. 5) probably due to absence of a negative feedback effect by reflectance increase by surface melting.

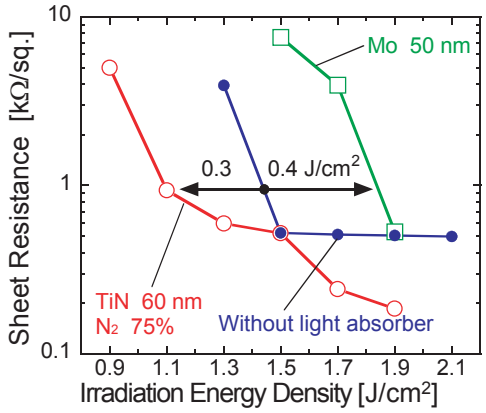

Fig. 4 Relationships between sheet resitance and laser energy density. TiN film deposited on Si as a green-laser-light absober reduces the laser energy density necessay for dopant activation.

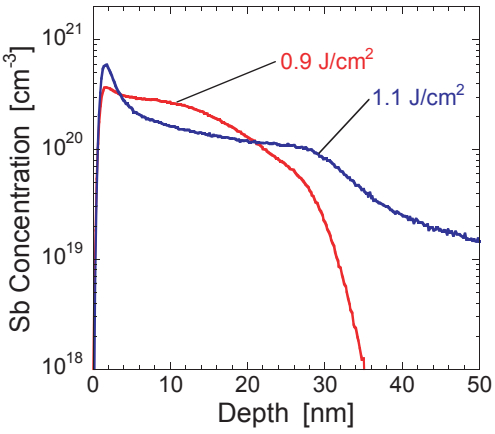

Fig. 5 Sb depth profiles after the green laser annealing with the TiN light absorber. The depth profiles for 1.1 J/cm^2 shows overmelt that makes the junction much deeper.

3. Summary and future plan

Low resistive ultra-shallow junctions were fabricated using heat-assisted KrF excimer laser annealing. This method is also effective for residual defects reduction. Investigation of another laser annealing method with green laser has started. We will improve the later importing the idea of heat-assisted method to it.

4. Published Papers and Proceedings

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Research and Development of Three-Dimensional MOS Transistors

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Colleagues： Kiyoshi Okuyama(COE Researcher), Akira Katakami(Graduate School of Advanced Sciences of Matter, 2003 Graduated), Kei Kobayashi (Graduate School of Advanced Sciences of Matter, M1), Shunpei Matsumura (Department of Engineering B4)

1. Purpose of R&D

Greater integration and higher density of integrated circuits which started around 1970 has achieved almost one million increase in performance. The strongest driving force is scaling of MOS transistor. First transistor of 10 μm in size has been scaled to 1/10 during 15 years and to 1/100 during another 15 years. Transistors of 0.1 μm in size will soon be manufactured. While, a transistor of 5 nm in size has already been presented in research stage, however, its performance is not adequate yet contrary to its size[1].

In response to its miniaturization, performance degradation due to the short-channel effects such as poor controllability of threshold voltage and increase in cut-off current have occurred.

Although precise control of impurity profiles near source and drain and thinning of the gate insulator have been developed to suppress the short-channel effects, limitations are getting close. To cope with thi problem, three-dimensional (3-D) MOS transistors such as DELTA[2], double-gate structure[3], FIN-FET[4] with very thin silicon-on-insulator (SOI) layer have been extensively developed.

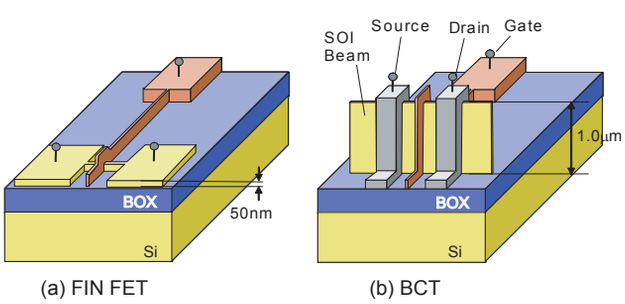


Fig. 1 FINFET (a) as a representative of 3-D transistor and a beam channel transistor, BCT under study.

A 3-D transistor with 10-nm gate length has already been presented. As the transistor has vertical channels on a Si beam, as shown in Fig. 1, drive current per unit planar area can be increased with the increase in the beam height.

To achieve higher drive current, it is planned in this study to get relatively higher beam. Major subjects are listed in Table 1. Difficulty in fabricating tall 3-D transistor rather depends on aspect ratio of the beam than absolute height of the beam.

Table 1 Purpose and subjects of this study

A. 3-D transistor with beam higher than 500 nm.
- (a-1) Delineation of high Si beam
- (a-2) Gate formation around high Si beam
- (a-3) Impurity doping to high Si beam
- (a-4) S/D contact to high Si beam

B. Highly self-aligned transistor with beam lower than 500 nm.

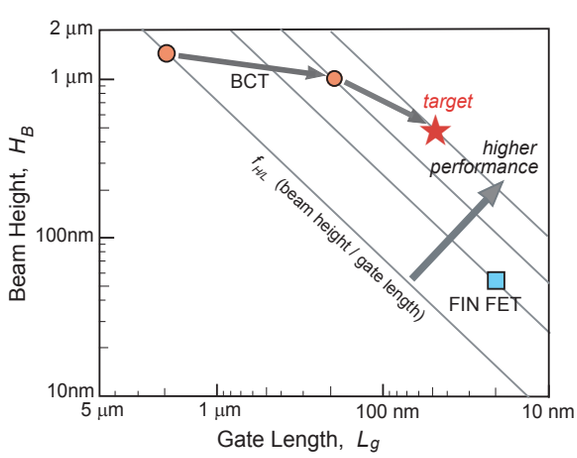


Fig. 2 A figure of merit of beam height / gate length, $f_{H/L}$ of 3-D transistor.

2 Experimental and the Results

2.1 Delineation of high Si beam

It is possible to obtain high aspect-ratio Si beam with present highly directional reactive ion etching, RIE. However, anisotropic etching with tetramethy lammoniumhydroxide, TMAH may be adequate to realize much higher and steeper beam. fabricating tall 3-D transistor rather depends on aspect ratio of the beam than absolute height of the beam. Due to its very low etch rate for (111), as shown in Fig. 3, almost perfect perpendicular sidewall can obtained on (110) Si substrate. Some etched samples are shown in Fig. 4[5] and obtained etch rates are shown in Table 2.

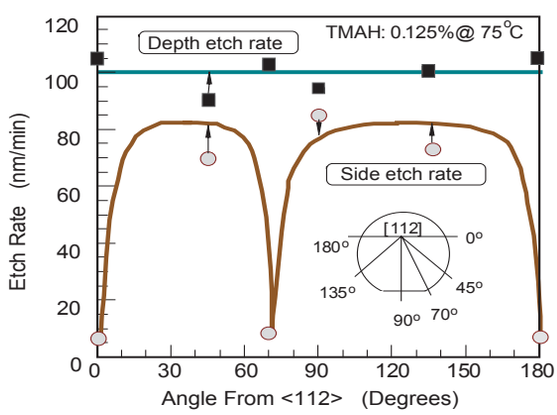
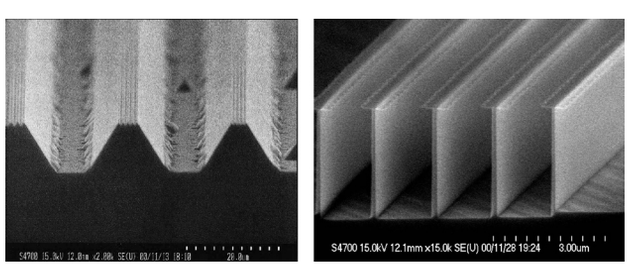


Fig. 3 Etch rate of TMAH on (110) Si surface. Extremely low etch rates correspond to those for (111) surface.



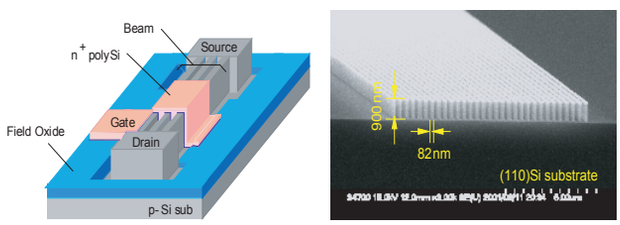
(a) Silicon (100) surface (b) Silicon (110) surface

Fig. 4 Obtained cross sections of Si (100) (a) and Si (110) with TMAH etchant.

Table 2 Etch rates of TMAH (2.5% aqueous solution at 75°C).

Material	Etch Rate	Ratio
(110) Si	606 nm/min	30
(111) Si	30 nm/min	1
SiO_2	0.8 nm/min	0.04

Using this etchant, a corrugated channel transistor with multiple Si beams has been succcessfully fabricated[6] as shown in Fig. 5. The height and the width of the beam are 900 nm and 82 nm, respectively. The I_d-V_d characteristics of the transistor are shown in Fig. 6. While the threshold voltages are below 0 V because the substrate resistivity of 80 Ω-cm and not employing channel doping, there is no degradation concerning carrier mobility and gate oxide integrity.



(a) (b)

Fig. 5 A bird's eye view (a) and an SEM image of etched SI beams. surface.

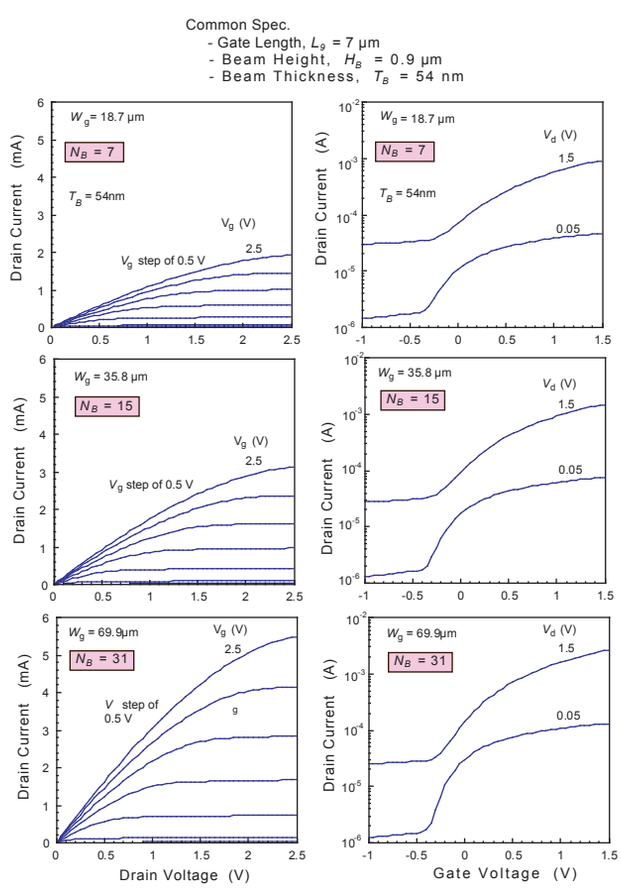


Fig. 6 I_d-V_d and I_d-V_g characteristics of corrugated channel transistor, CCT. Obtained threshold voltages below 0 V are due to high reistivity substrate (80 Ω-cm) and no channel doping.

Substrate bias dependence of the threshold voltage is shown in Fig. 7. Curves of beam thickness T_B of below 0.96 μm are almost the same each other due to throughly depleted beam. Drain currents are shown in Fig. 8 in terms of unit planar area. CCT offers almost 5-fold current as compared to the conventional planar at a planar area of 100 μm^2.

Regarding gate oxide integrity, there may be some problem due to the oxide thinning at edges of the beam.. In fact the thinning are observed at top and bottom edges of the Si beam as shown in Fig. 9. However, there is no substantial failure because applied voltages get lower in response to transistor scaling.

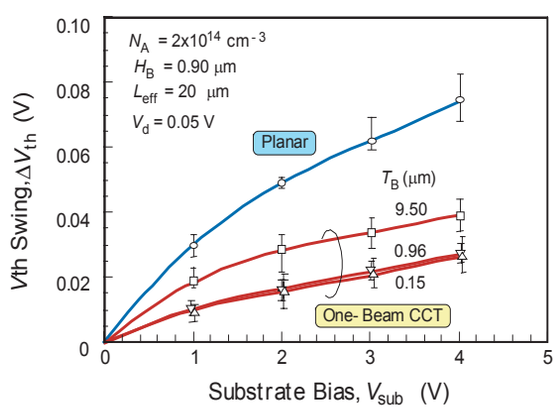


Fig. 7 Threshold voltage swings for one-beam CCT and planar transistor. Note that curves with beam thickness T_B of below 0.96 μm are equivalent.

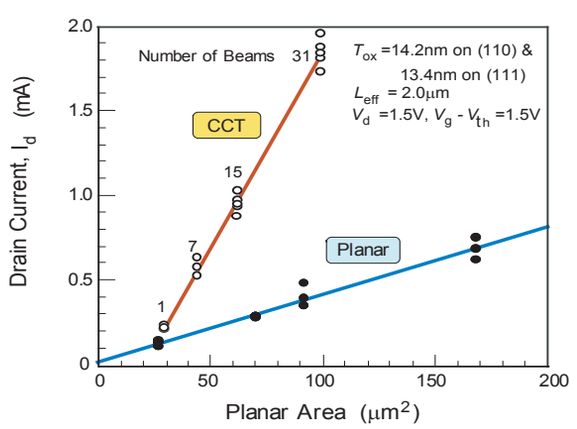


Fig. 8 Drain currents of CCT's with number of beams of from 1 to 31. Almost 5-fold increase is obtained compared to planar transistor at a planar are of 100 μm^2.

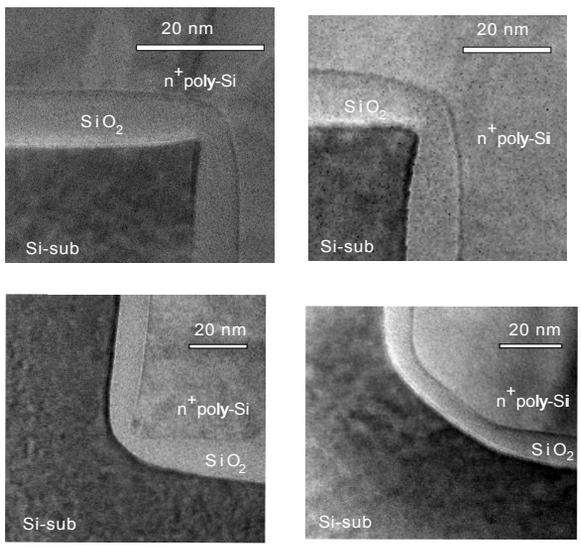


Fig. 9 Cross-sectional TEM images for oxide thinning at beam edges.

2.2 Delineation of gate electrode overlaying high Si beam

The use of conventional anisotropic dry etching to delineate polysilicon gate overlaying Si beam gives rise to residues on sidewalls of the beam as shown in Fig. 10 (a). Thus, isotropic etching is inevitable at present, as shown in Fig. 10 (b).

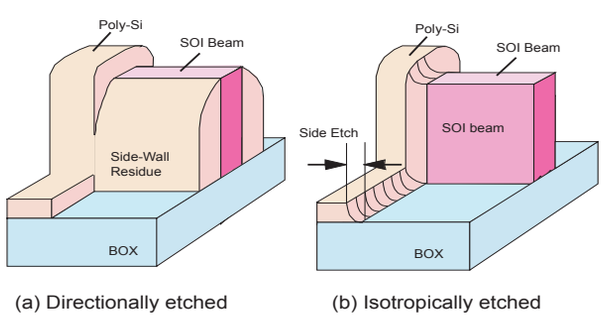
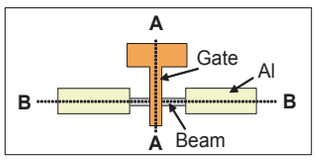


Fig. 10 Gate electrodes formed by anisotropic etching (a) or isotropic etching (b).Cross-sectional TEM images for

To overcome the problem, a novel technique has been developed[7]. This technique makes it possible to wrap the polysilicon gate with its own oxide, as shown in FIg. 11, utilizing impurity enhanced oxidation, IEO[8]. The enhancement occurs with highly doped Si at low-temperature wet oxidation. In certain condition more than 10-fold enhancement is possible. An obtained sample and the IEO are shown in Fig. 12 and Fig. 13, respectively.



(A-A cross section) (B-B cross section)

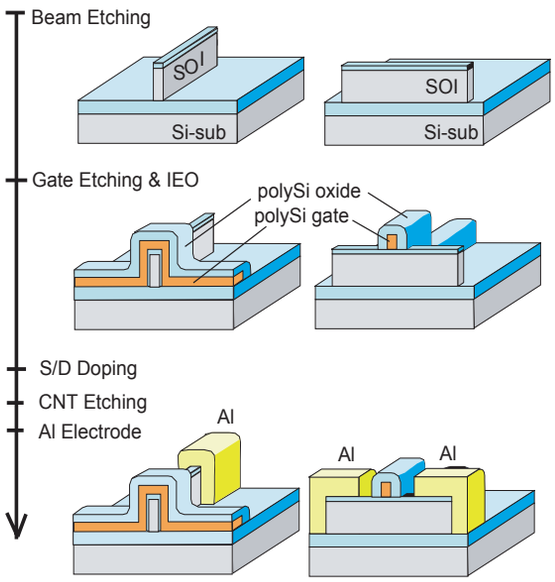


Fig. 11 A proposed process sequence of beam channel transistor.

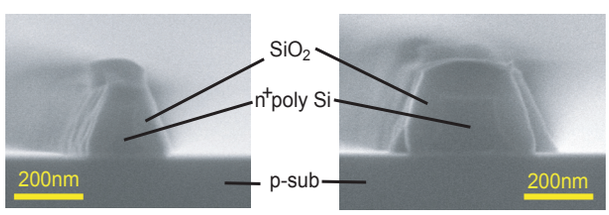


Fig. 12 Polysilicon gates wraped by their own oxide.

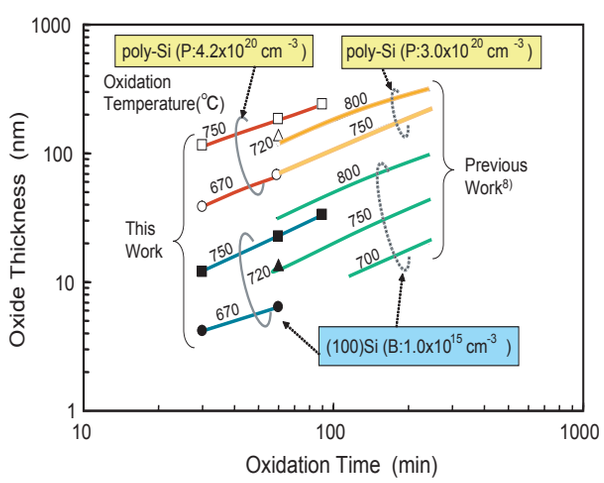


Fig. 13 Experimental results of impurity enhanced oxidation, IEO.

A cross section, I_d-V_d and I_d-V_g characteristics are shown in Figs. 14, 15, and 16, respectively for beam channel SOI transistors fabricated with these techniques described here. These characteristics show no deterioration.

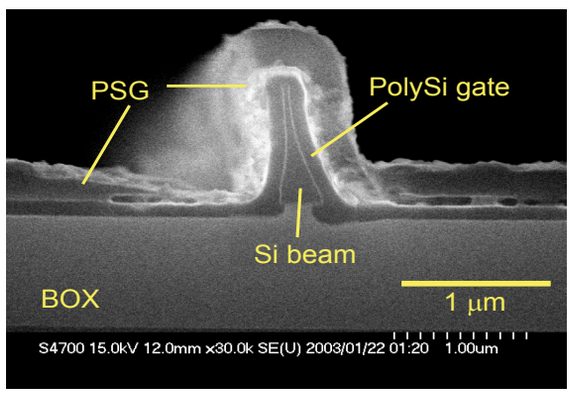


Fig. 14 A cross section of SOI beam channel transitor with 1.0-μm high SOI beam.Ω-cm) and no channel doping.

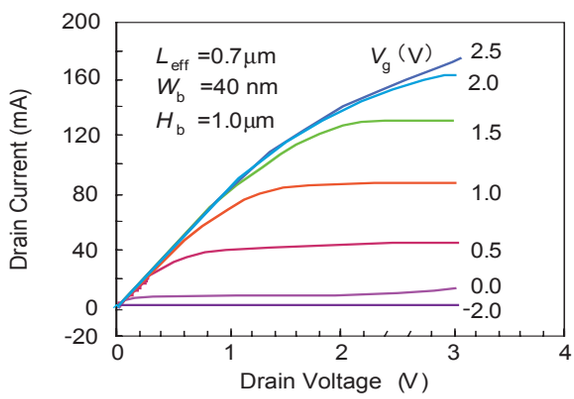


Fig. 15 I_d-V_d characteristics for beam channel transistor with 1.0-μm high and 40-nm thick SOI beam and 0.7-μm channel length. No channel implantation causes weak cut-off.

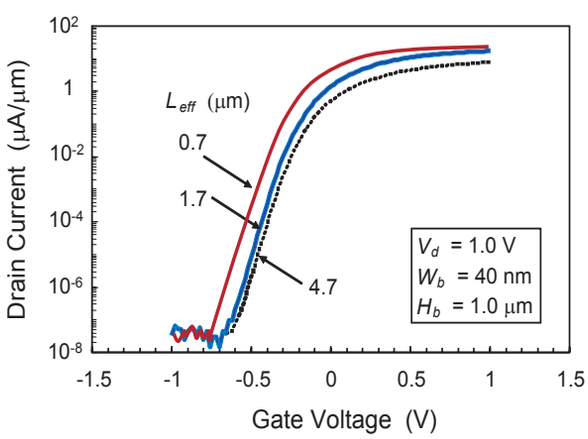


Fig. 15 I_d-V_g characteristics for beam channel transistor with 1.0-μm high and 40-nm thick SOI beam and 0.7-μm channel length. No channel implantation causes weak cut-off.

One of performance factors of MOS transistor is a figure of merit [$I_d L_{eff} T_{ox}/W_{eff}$] . This directly relates to field-effect mobility and integrity of the transistor. Figure 17 shows these for BCT and FIN-FET. It is because mobility decrease that the factor decreases at small beam width region. This should be an inherent problem for very thin Si beam 3-D transistor.

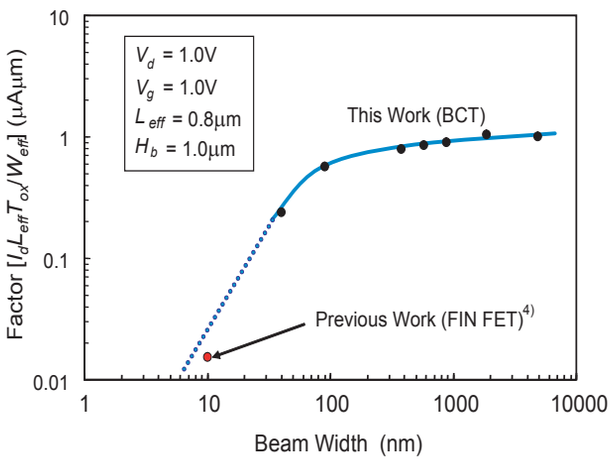


Fig. 17 Dependence of a factor, [$I_d L_{eff} T_{ox}/W_{eff}$] on beam width. cut-off.

While, a ratio of on current to off current is shown in Fig. 18. The ratio is more important rather than on-current itself to design high performance and low power LSI. Beam channel transistor has considerable merit in therms of this performance.

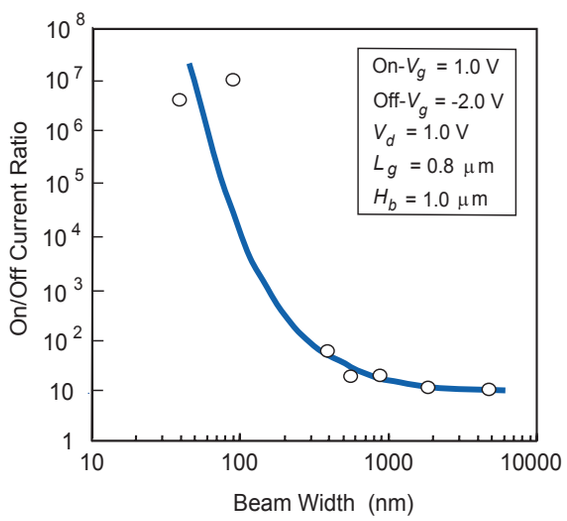


Fig. 18 Beam width dependence of on-current to off-current ratio for SOI BCT (T_{OX}=10 nm).

2.3 Impurity doping to high Si beam

Even though utilizing oblique implantation, there exists certain limitation to conventional ion implantation technique, I/I to make uniform doping to high and dense Si beams. To cope with the problem, nearly isotropic plasma doping, PD is applied in this study.

A comparison of impurity profiles of I/I and PD is shown in Fig. 19 at the same acceleration voltage of 700 V. While, the beam shape is shown in Fig. 20. It is clear that the edges are sputtered and scraped off to some extent by Ar plasma in PD.

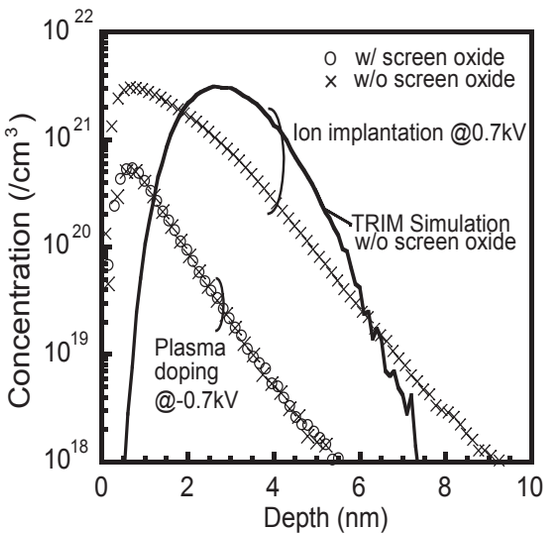


Fig. 19 Srsenc SIM profiled for ion implantation and plasma doping.

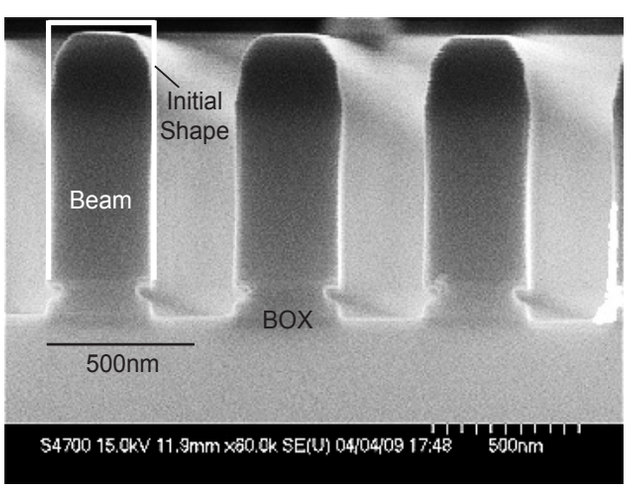


Fig. 20 Si beams doped with Arsenc by plasma doping. Top edges are sputtered and scraped off by Ar plasma at -700-V bias.

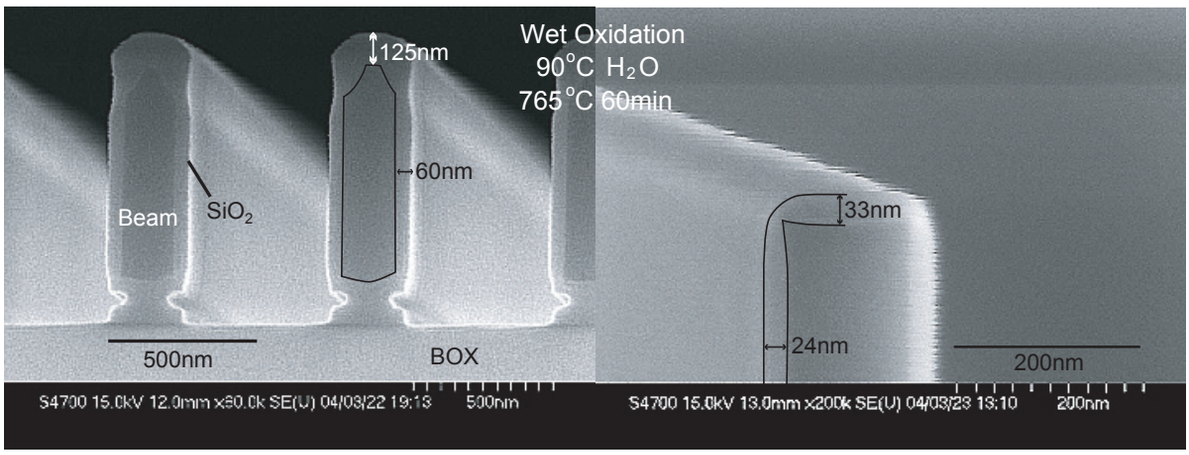


Fig. 21 Cross-sectional SEM images of As-plasma doped Si beam (a) and non-doped Si beam (b) after wet oxidation at 765°C for 60 min. Oxide thickness closely relates impurity concentration.

There is no direct measurement technique to evaluate 3-D impurity profile along vertical wall. Therefore, a novel indirect technique is proposed, which utilizes impurity enhanced oxidation. An oxide profile is shown in Fig. 21. From this profile, Arsenic concentration profile is thus evaluated and shown in Fig. 22. It is clear sidewalls are almost uniformly doped despite that top edges are doped at several times higher concentration. Both side dips in "Non-doped" curve correspond to poor uniformity of oxide, as shown in the right side of Fig. 21.

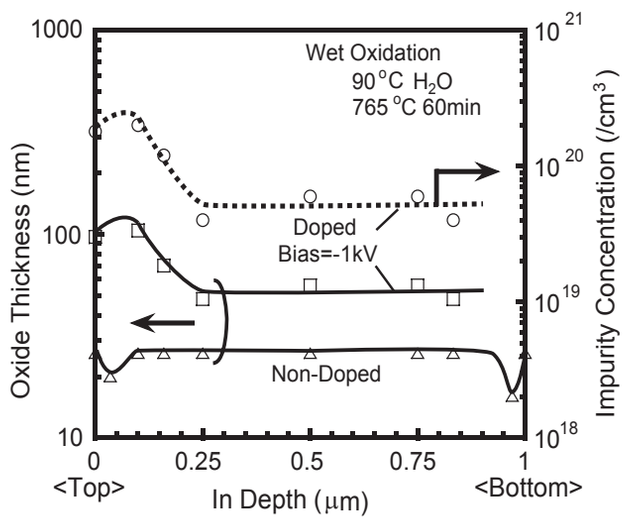


Fig. 22 Measured oxide thickness profile and doped impurity profile for 1.0-μm high Si beam, indirectly evaluated from the oxide profile.

2.4 S/D contact to high Si beam

When a contact to source and drain (S/D) is formed only on the top surface of the beam, a part of source currrent flowing at the bottom portion suffers form parasitic resistance of the source. This causes performance degradation of the transistor. Obtained beam resistance is shown in Fig. 23. It is observed that beam resistance becomes constant at beam width of below 300 nm. It is because thickness of phosphorus-doped region becomes constant at that rgion.

Since the thickness of S/D region of BCT is smaller than 100 nm, S/D resistance can not be neglected. To overcome the problem, some methods efficient to reduce the resistance should be employed. These are as follows:

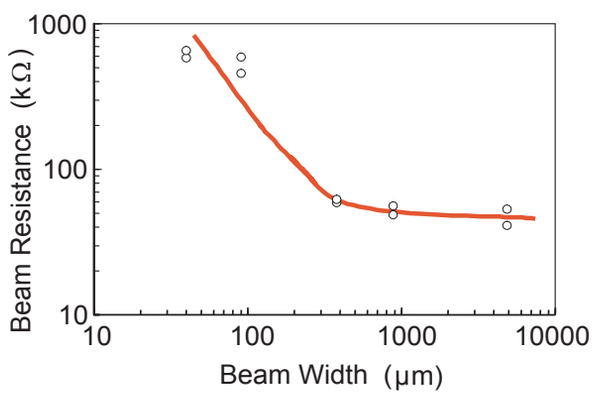


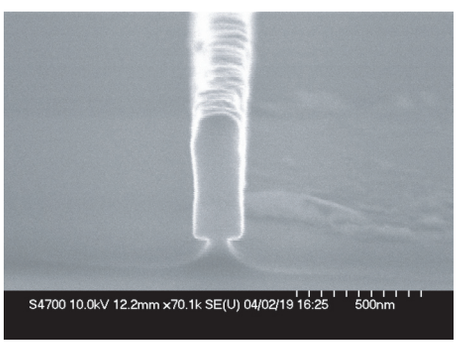
Fig. 23 Beam width dependence of beam resistance for phosphorus-doped Si beam.

(1) silicidation of S/D,
(2) elevated S/D with Si and/or Ge, and
(3) metal wrapping around S/D.

Preliminary experiment for silicidation has been carried out in this study. Phosphorus-doped Si beam is silicided with 100-nm thick sputtered Ni after vacuum baking at 500°C for 30 min, as shown in Fig. 25. Beam width dependence of the beam resistance is shown in Fig. 25.

Estimated resistivity of phoshprus-doped Si beam and its silicided layer are:

- n^+-Si beam resistivity = $4.2\times10^{-4}\Omega$-cm
- Ni silicide layer resistivity = $2.5\times10^{-5}\Omega$-cm



Beam height/width＝550 nm/180 nm

Fig. 24 Ni-silicided Si beam.

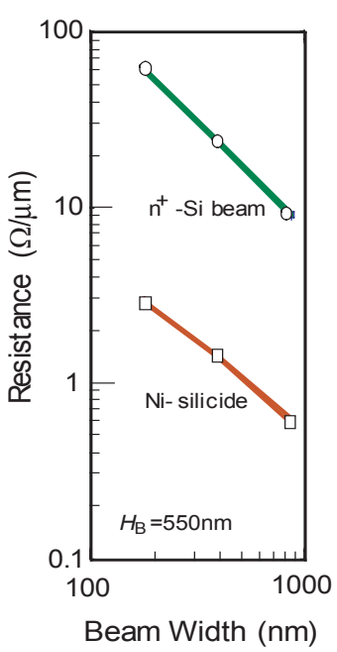


Fig. 25 Resistance of Ni-silicided S/D

Reagarding these values, it is clarified that adequate silicidation occurs. Since the data are taken only for one isolated beam, dense and multi-beams should be investigated.

3 Conclusion and Future Plan

In this study, one set of beam channel transistor, BCT of 1.5-μm beam height and 2.0-μm gate length, and another set of those of 1.0-μm beam height and 0.2-μm gate length are successfully developed. Since BCT with high Si beam can not provide narrow channel width, the BCT is not able to be major conponent of LSI. Therefore, the BCT is suitable to some applications with big power in small area.

They are:
(1) discrete power transistor,
(2) wireless receiver/transmitter IC integrateing RF power transistor, and
(3) power control transistor for ultra-low power.

Some example concerning item (3) is shown in Fig. 26. This is an idea that a pull-down transistor which is connected in series to a circuit block controls power and operation speed of the block in time sharing manner.[9] Since it is desirable that on-resistance of the pull-down transistor is as small as possible, BCT which can provide large current in small planar area is suitable with less area penalty.

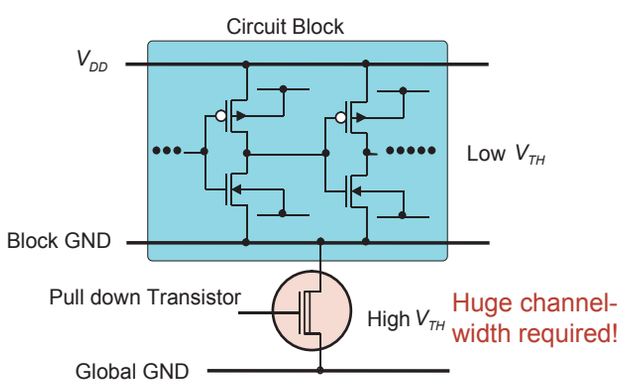


Fig. 26 An idea to control power/operation speed with each circuit block[9].

Regarding to ultra-small 3-D transistors, those of 50-nm thick beam and 20-nm gate length has been already presented by other organization. Taking the aspect ratio of the beam into consideration, our target of those of 200-nm thick beam and 20-nm gate length is not promising target any more.

Thus, highly self-aligned configuration in full use of 3-D structure is our target. One candidate is shown in Fig. 27. Since three planes of a beam act as different transistor, this configuration gives birth to ultra-small three transistors connected in parallel.

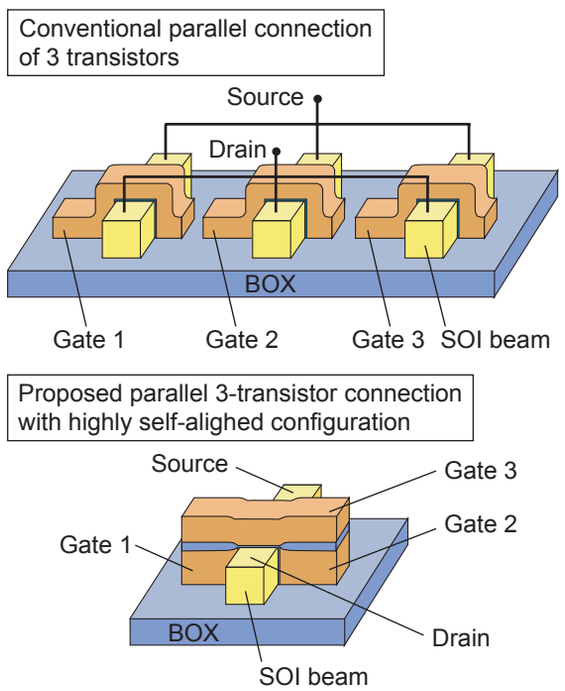


Fig. 27 Three transistors connected in pallarel with highly self-aligned configuration.

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<Results of R&D>

(Journal Paper)

1)T. Furukawa, H. Yamashita, and H. Sunami, "A Proposal of Corrugated-Channel Transistor (CCT) with Vertically-Formed Channels for Area-Conscious Applications," Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2067-2072, April 2003.
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Study in 3-Dimensional new structure MOS Transistor

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Graduate School of Advanced Sciences of Matter)

1. Introduction

It is becoming difficult to control the short channel effect and to integrate conventional bulk devices up to date. To overcome this problem, three-dimensional (3-D) device structures have been proposed [1]. A FinFET of which gate electrode is 10 nm in length was already reported [2]. From now on, not only the scaling of these devices, but also the progress of new structure and/or new operation of 3-D devices become important. In this study, a new vertical structure transistor is proposed.

2. Proposed device and its fabrication processes

The structure of proposed device is shown in Fig. 1. In this structure, three transistors that are formed on a SOI beam can operate independently. This can apply to parallel part of a logic circuit, for example a part of NAND gate. Since transistors are integrated vertically, this structure has advantage from the viewpoint of area efficiency.

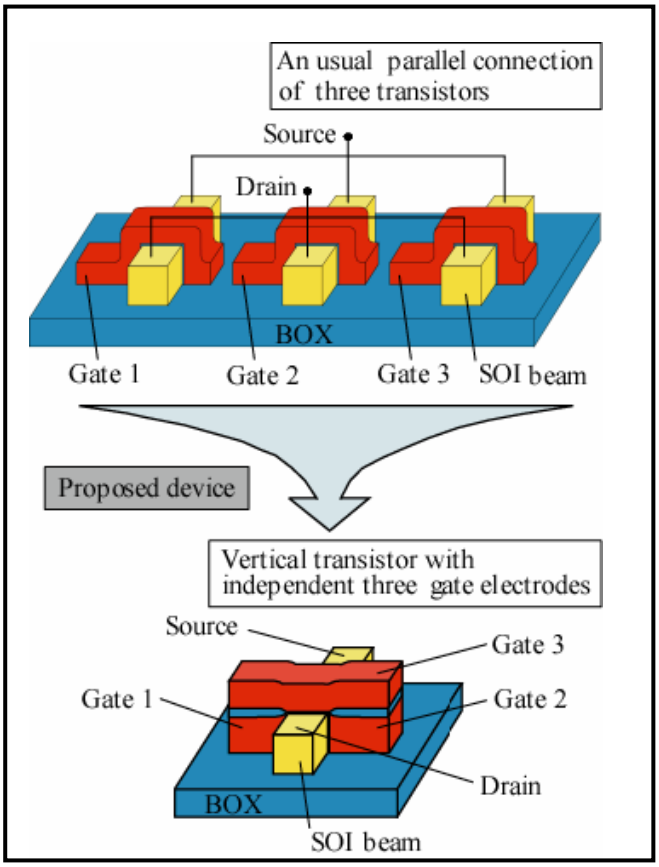

Fig. 1 A usual parallel connection of three transistors and the structure of the proposed device.

In the fabrication of this device, it is important to form three gate electrodes using self-aligned process to realize normal operation of the device. Two types of fabrication processes are devised in consideration of this point. One of these processes is shown in Fig. 2. To realize the proposed device, fabrication processes for Si-beam and gate electrode, and leveling of some kinds of materials are key techniques.

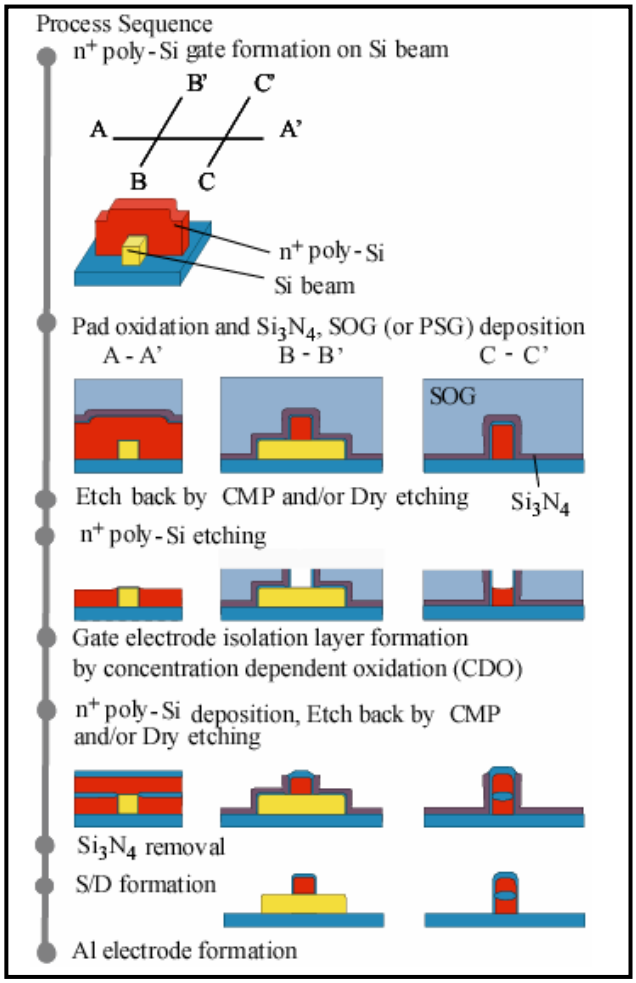

Fig. 2 A process sequence of the proposed device.

3. Experimental results and Discussion

3.1 High aspect ratio fabrication technique

Since the configuration of poly-Si patterns overlaying Si beams determines the shape of final gate electrodes in the sequence, its formation techniques are very important. During the course of the study, a Si beam of 120 nm in height and 60 nm in width and a poly-Si pattern of 100 nm in width overlaying the beam are successfully fabri-

cated (Fig. 3). Furthermore, with respect to the concentration dependent oxidation (CDO [3]) that utilized to form the isolation layer of top gate electrode, the ratio of oxidation thicknesses of phosphorous doped n^+poly-Si and Si substrate((100), boron doped, $1x10^{15}$ /cm^3) exceeds almost 14 times at 750℃ (Fig. 4). From this result, it is concluded that the CDO is applicable to the process.

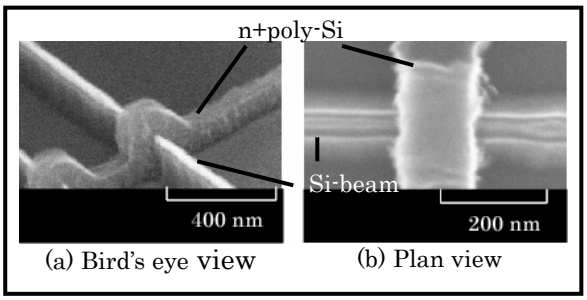

Fig. 3 SEM photographs of a Si-beam of 120 nm in height and 60 nm in width and a poly-Si gate electrode overlaying the beam.

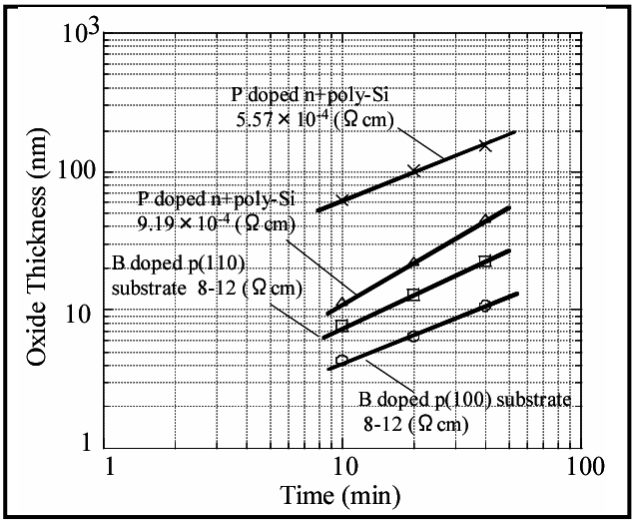

Fig. 4 Concentration dependent oxidation (CDO) at 750℃ (O_2=2 slm, 90℃ H_2O bubbling.).

3.2 Leveling process

Two kinds of methods, RIE and CMP techniques are developed as the leveling process. In this experiment, SOG was used as the leveling material. The etching characteristics of RIE are shown in Fig. 5. In this case, four kinds of materials (SOG, Si_3N_4, SiO_2, n^+ poly-Si) have to be etched with adequate low selectivity, then the etching has been performed under a condition of H_2 = 0 and 4 sccm. In the former case, it was observed that SOG and Si_3N_4 were already etched before leveling the n^+ poly-Si layer. In the latter case, the roughness of n^+ poly-Si surface was degraded and the damage on the top of source and drain regions of Si beam occurred (Fig. 6).

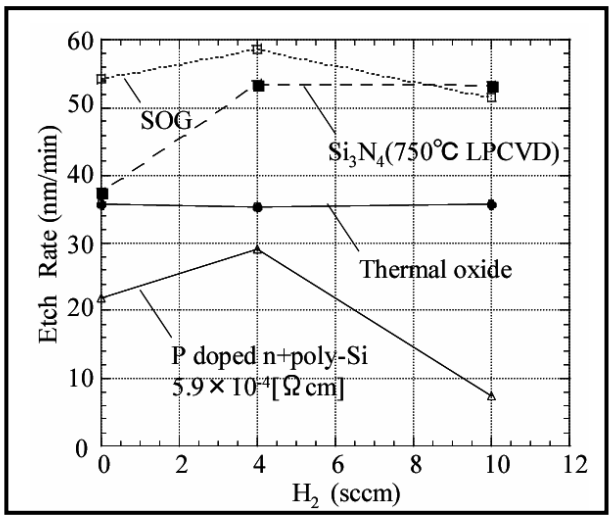

Fig. 5 Etching characteristics of RIE (CF_4 = 20 sccm, etching pressure = 30 mTorr, self bias = –410 V) .

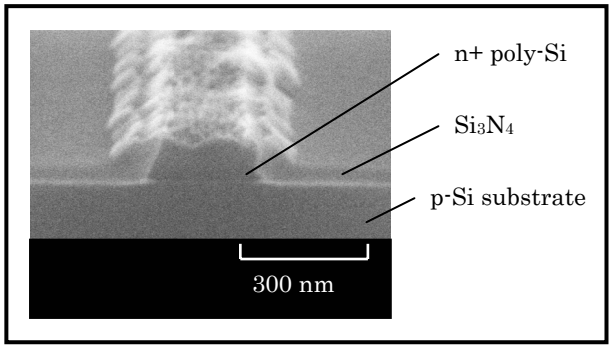

Fig. 6 SEM photograph of an n^+ poly-Si electrode after RIE etch-back.

4. Summary and future work

A novel 3-D transistor structure and its fabrication processes are proposed. With respect to the high-aspect ratio fabrication technique, poly-Si patterns overlaying Si beams are successfully fabricated. Furthermore, the result that CDO can be applicable to the isolation layer formation of the top gate electrode is obtained. Due to the difficulty of RIE etch back in leveling process, the introducing of CMP technique is planned to realize the proposed device structure.

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Development of Novel Functional Si-based Devices Using Self-assembled Nanostructures for Multivalued Memory Operation, Ultimate Photo-sensing and Molecular Recognition

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1. Research Target

The serious limitations in down-sizing conventional MOS devices motivate us to develop novel functional devices operating with a few electrons and a few photons by means of an introduction of well-defined Si nanostructures into the MOS devices.

In this project, for the advanced information processing with a few electrons and photons, we focus attention on the device application of unique physical properties of Si nanocrystals associated with quantum size effects [1-2]and coulomb brocade [3] and have intensively studied MOSFETs with quantum dots (QDs) as a floating gate [4,5] which operate even at room temperature and low voltages. Based on a deep understanding of the multivalued capability of the QDs-floating-gate, we also plan to design and fabricate optically or chemically coupling QDs-floating-gate MOSFETs. For the optically coupling devices, the gate stack structures consisting of a semitransparent metal gate, a gate dielectric with a high dielectric constant (high-k), a QDs-floating gate and the bottom tunneling oxide will be investigated to achieve operations critical to the input of a few photons. And for the chemically coupling devices, porous metal gate will be combined with a high-k dielectric as control gate insulator to selectively adsorb specific molecules on the high-k gate dielectric.

In addition, from viewpoints of the synthesis of new tailor-made electronic materials, we will extend our research work to three dimensionally stacked structures of Si-based dots with a high areal density to control unique transport properties originating from electronic coupling among neighboring dots.

Major research issues are as follows:

1. Development of process technologies to control precisely the dot size, its distribution and position and fabrication of well-ordered array and high density stacked structures of dots
2. Characterization of carrier transport through coupling dots
3. Control of energy band structures with an introduction of Ge core to Si dots
4. Valence control with impurity doping to Si-based dots
5. Fabrication and characterization of QDs-floating-gate MOSFETs for multivalued operation, high photosensitive performance and molecular recognition

2. Research Results

2.1 Self-assembling Formation of Si-QDs by Low Pressure CVD

We have demonstrated that hemispherical single-crystalline Si-QDs with a fairly uniform size distribution and a high areal density ($\sim 10^{12} cm^{-1}$) can be spontaneously formed on thermally-grown SiO_2 layers by controlling the early stages of LPCVD using a SiH_4 gas [6]. The temperature dependences of the areal dot density and the dot size in the early stages of LPCVD in the range of 560-700°C have shown that, for the dot formation on clean as-grown SiO_2, the Si-O bond breaking plays a role in the creation of nucleation sites and the dot size is rate-limited by the SiH_4 decomposition on Si and Si cohesive action. In addition, it has been found that surface Si-OH bonds if any act as reactive sites during LPCVD to efficiently promote the dot formation. Also, the SiH_4 pressure dependence of the areal dot density at 560°C show that, in the pressure region below 0.1Torr, a reduction in the SiH_4 pressure causes a marked decrease in the dot density, especially on as-grown SiO_2, suggesting that the thermal decomposition of small Si clusters before reaching the critical size for stable nucleation growth becomes significant under a low SiH_4 flux. The result indicates that, to obtain high selectivity of Si dot nucleation between as-grown and OH-terminated surfaces, the suppression of the spontaneous nucleation on as-grown SiO_2 is of great importance and the control of the SiH_4 pressure during LPCVD is one of critical factors. The formation of spherical Si QDs with a Ge core is also succeeded by controlling the selective deposition conditions in LPCVD using alternately SiH_4 and GeH_4.

2.2 Positioning of Si-QDs on SiO_2

Based on the better understanding of the Si dot formation mechanism, the spatial control of OH termination on SiO_2 leads into positioning the nucleation site. In fact, the chemical or electrochemical surface modification on a nanometer scale by using AFM/STM probe techniques enables us to make regular arrays of Si dots as shown in Fig. 1, where the as-grown SiO_2 surface just before LPCVD was exposed to the electron beam from the a Pt (20%Ir) STM tip in H_2 ambient of $1x10^{-5}$Pa[7]. Since H atoms are adsorbed on the clean Pt-tip surface through dissociative adsorption even at room temperature and emitted under a high electric field between the tip and the sample surface, reac-

tive sites such as Si-H and Si-OH bonds are formed efficiently.

2.3 Evaluation of Charged States in Si-QDs

We have demonstrated that charges retained in the single Si dot covered with ultrathin SiO_2 are directly quantified from the change in the surface potential of Si dots induced by electron injection or emission through ultrathin SiO_2 as measured with an AMF/Kelvin probe technique [8]. For the Si dots in the range of 4.3-13nm in dot height, stable retention of single electron in each dot on 4nm-thick SiO_2 was confirmed from the comparison between measured surface potential changes on the charged dots with the calculated results in the equivalent circuit mode. For Si-QDs with a Ge core, we have also found that electrons and holes are retained in the Si clad and the Ge core, respectively as predictive in the type II band discontinuity between the Si clad and the Ge core.

2.4 Characteristics of MOS Capacitors with Si-QDs as a Floating Gate

Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of Si QDs floating gate MOS capacitors exhibit unique hystereses which arise from charging and discharging in the Si QDs through the bottom tunnel oxide as shown in Fig. 2. For the case on p-Si(100) with an acceptor concentration of $3x10^{16}cm^{-1}$, the C-V curve measured from –3V to 3V is almost identical to the C-V curves for the case of uncharged Si-QDs floating gate. Similarly, the C-V curve measured from +3V to –3V for the case on n-Si(100) with an donor concentration of $1x10^{15}cm^{-1}$, is almost identical to the C-V curve for the uncharged floating gate. In both cases, a flat-band voltage shift of ~0.27V is observed and the capacitance peak, which is due to the emission of remaining charges to the substrate as seen in I-V characteristics, is measured around the corresponding flat-band voltage, namely the voltage separation of the peaks agrees well with the value expected from the difference in the Fermi level between p-Si(100) and n-Si(100). The results indicate that the dots act as memory nodes. In other words, we can rule out the contribution of traps with specific energy levels to the measured C-V hystereses. I-V characteristics shows multiple-step electron charging (or discharging) characteristics of the Si-dot floating gate are observable, suggesting that Coulombic force arising from charged dots efficiently suppresses the electron charging of neighboring neutral dots. When the floating gate consists of double-stacked dots instead of a single dot layer, the retention characteristics are improved significantly with keeping the tunneling oxide thickness constant for a high writing speed as represented in Fig. 3.

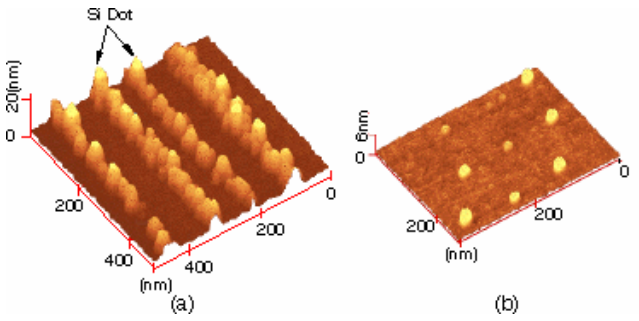

Fig. 1 AFM image obtained after Si dot formation at 560ºC on the SiO_2 surface modified with spot and densely lined patterns by the STM tip. In the STM surface modification prior to LPCVD, the tip bias was applied at -10V with respect to the substrate.

2.5 Characteristics of Si-QDs Floating Gate nMOSFETs

Based on the characteristics of MOS capacitors with the Si-QDs floating gate, n-MOSFETs with adoubly-stacked Si-QDs floating gate. The drain current-gate voltage (I_d-V_g) curves show characteristics hysteresis arising from electron charging and discharging of the Si-QDs floating gate (Fig. 4). Distinct current bumps, which were observed in ramping up the gate voltage after complete discharging at -4V, indicate the multi-step electron charging to the Si-QDs floating gate caused by the Coulomb blockade effect. Considering that, in the region of 0-0.5V, a new current component emerges with increasing sweep rate, four steps of electron injection to the Si-QDs floating gate with an areal dot density of ~$6x10^{11}cm^{-2}$ are confirmed. In addition, the threshold voltage shift at each charging steps is not equal to that of the next charging step and slightly increase with progressive electron charging. This implies

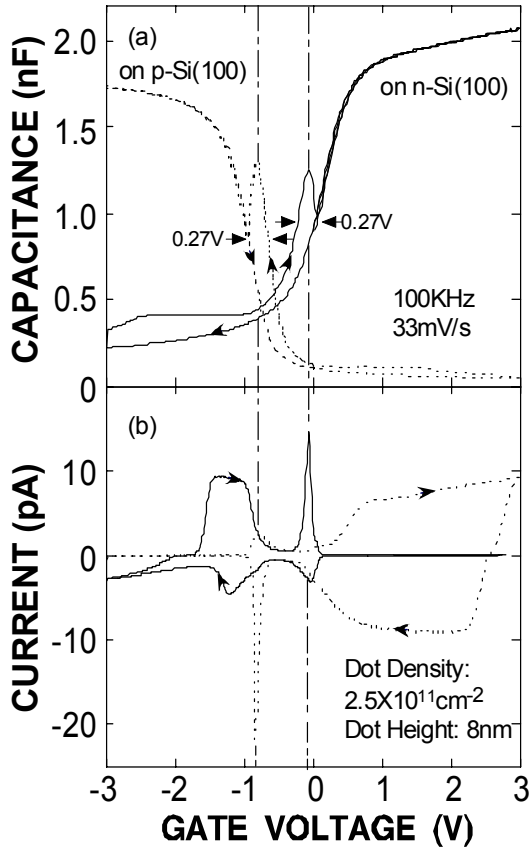

Fig. 2 Capacitance-voltage (a) and current-voltage (b) characteristics of Si-QDs floating gate MOS capacitors fabricated on p-Si(100) and n-Si(100).

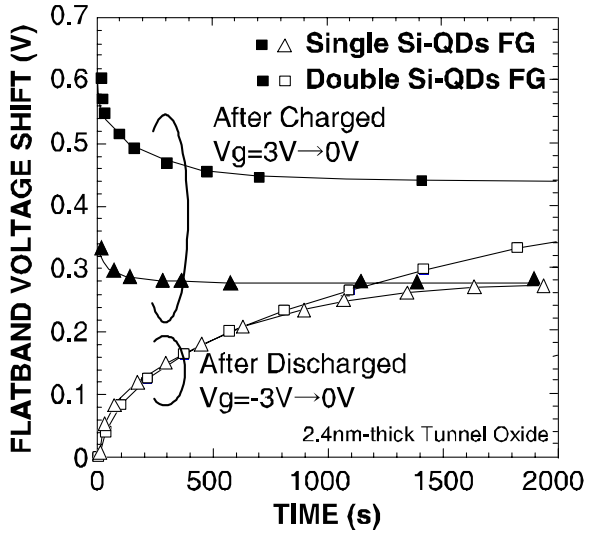

Fig. 3 Retention characteristics of MOS capacitors with the floating gate consists of double-stacked and a single-layer Si QDs.

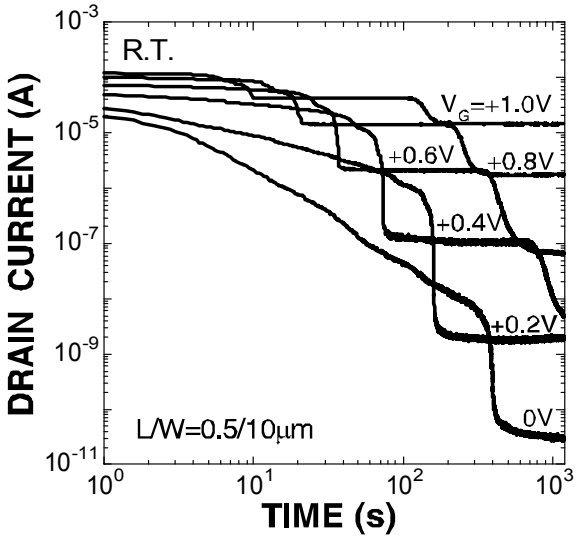

Fig. 5 Temporal change in drain current at various gate biases and a drain voltage of 50mV after complete discharging of a Si-QDs floating gate at a gate voltage of -4V.

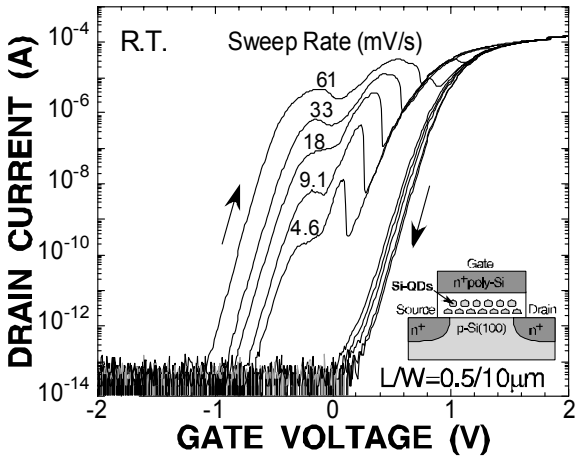

Fig. 4 Drain current vs gate voltage characteristics of a Si-QDs floating gate MOSFET, which were measured after fully discharged at a gate bias of -4V. The drain voltage was 50mV. The voltage sweep rate was changed in the range from 4.6 to 61mV/s. A cross-sectional view of a Si-QDs floating gate MOSFET is illustrated in the inset.

that the Coulomb interaction from the neighboring charged QDs play a subsidiary role on the electron tunneling form the channel to the Si-QDs. In other words, this can be interpreted in terms that the charging energy of the Si-QDs depends on not only charged states of individual Si QDs but also charged states of neighboring QDs. In general, since the charging time of the Si-QDs floating gate strongly depends on the gate voltage, faster the sweep rate is, higher the gate voltage for the charge injection becomes. In fact, with increasing sweep rate, the current bumps appear at higher gate voltages. Besides, the results of Fig. 4 implies that the charging voltage is affected by the redistribution of electrons in the Si-QDs floating gate during the gate voltage sweep as discussed later. Multi-step electron injection to the Si-QDs floating gate is also clearly seen in the temporal change in the drain current (I_d-t) at constant gate biases after complete discharging of the Si-QDs floating gate (Fig. 5). The threshold voltage after each current step corresponds to that of the scanned I_d-V_g characteristics. The distinct metastable state, in which the drain current is almost constant with respect to holding time, indicate that the total amount of effective charge in the Si-QDs floating gate remains unchanged in each of the metastable states. This result suggests that electron injected in the Si-QDs floating gate redistribution during each metastable state to reduce the effect of the Coulomb interaction among the charged QDs, namely to decrease the charging energy of QDs. The temperature dependence of Id-t characteristics measured at a fixed gate voltage show that a decrease in temperarture decelerates the electron charging and prolongs the metastable states, suggesting that the tunneling probability is increased with temperature for redistribution of electrons in theSi-QDs floating gate (Fig. 6). When the charging time (Δt_1 and Δt_2) and metastable time (Δt_3) are defined with a linearly extrapolation method and their reciprocal values are summarized in Arrehnius plots, the activation energy determined from the slope of the Arrehnius plot is found to be in the range of 0.23-0.31eV(Fig. 7). Base on the estimation of the sum of quantized and charging energies for QDs, we found that the obtained activation energy is almost equal to the energy separation between states for tunneling in QDs. It is likely that the electron tunneling between different energy states plays an important role on the observed multiple-step charging characteristics.

The influence of light irradiation on electron injection characteristics in Si-QDs floating gate has also been studied.

The temporal changes of drain current (I_d-t) measured at constant gates in dark and under light irradiation were

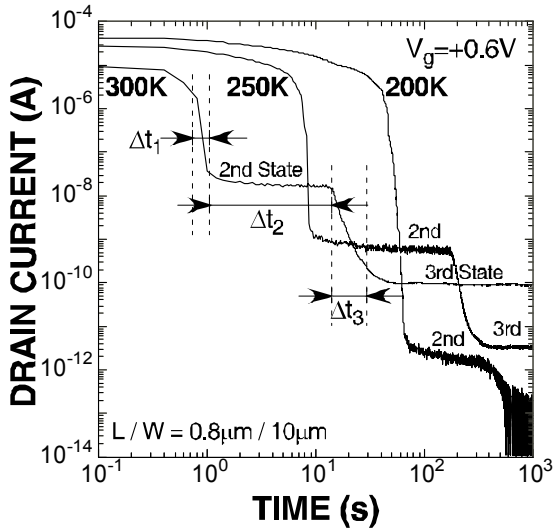

Fig. 6 Temperature dependence of I_d-t characteristics at a gate bias of 0.6V after complete discharging under the same condition of Figs 4 and 5. The drain voltage was 50mV. The definition of characteristics time (Δt_1, Δt_2 and Δt_3) is demonstrated in the curve at 300K.

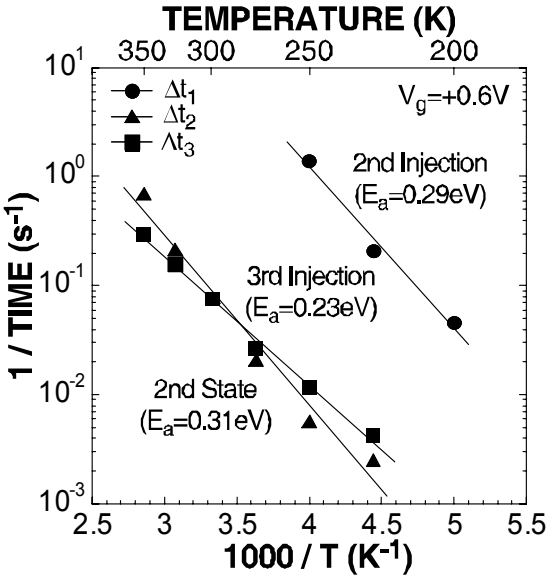

Fig. 7 Arrehnius plots of 2nd injection (Δt_1) and 2nd state (Δt_2) and 3nd injection (Δt_3) times from I_d-t characteristics.

compared as shown in Fig. 8. Although the current level is increased by 1.59eV light irradiation due to the photogenerated electron contribution, multistep electrion charging of the Si-QDs floating gate and a metastable state, in which a slight decrease in the drain current is observable, are still clearly observed as in the case measured in dark. Obviously, 1.59eV light irradiation promotes electron injection to the Si-QDs and reduces the period of the metastable charged state. Notice that when the light irradiation was turned off in the stable state achieved under light irradiation, the drain current coincides with the current level of the stable state obtained in dark. This indicates that the same amount of charges were injected finally into the

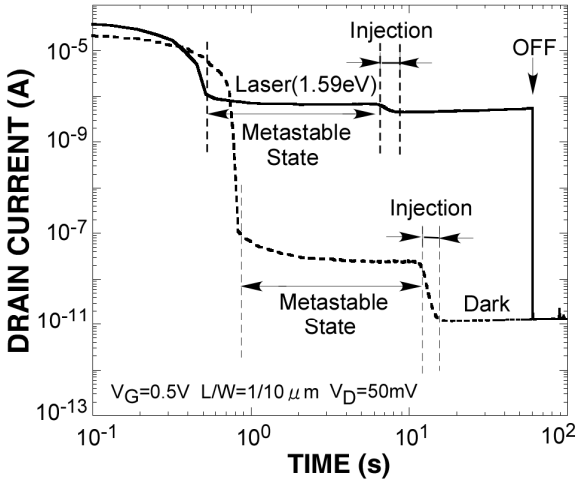

Fig. 8 Temporal changes in the drain current measured at V_g =0.5V under irradiation of 780nm (1.59eV) light and dark condition after complete discharging of the Si-QDs floating gate at V_g = − 4V. Electron charging to the Si-QDs floating gate causes the threshold voltage shift resulting in the decrease in I_d.

Si-QDs floating gate in both cases under light irradiation and in dark condition. In other words, no excess electrons over a thermally equivalent level in dark is not injected to the dots under this light irradiation, which implies sufficient energy separation between the charged state and the next. We also found that the electron injection speed at the transition from the metastable charged state to the finally stable charged state is unlikely to be accelerated with increasing photon flux (Fig. 9) and in the photon energy (Fig. 10) although the time to the final stable state becomes shorter with higher photon flux and/or higher photon energy. The result implies that the light irradiation mainly accelerates the temporal change in the charging during the metastable charged states to trigger the transition to the final stable state. During the I_d-t measurement, when light irradiation was turned off in the early stages of metastable charged states, the drain current quickly decreases to some current level once and recovered partly due to the electron emission from the dots and then followed by the temporal change in dark (Fig. 11). Since the electron emission becomes hardly observed with the time spending in metastable states, the redistribution of electrons in the Si-QDs proceeds during the metastable charged state to further election injection Based on these results, we can suggest that the light irradiation plays an important role on the redistribution of electrons in the Si-QDs floating gate. Considering the fact that, by irradiation of photons with a sub-gap energy (0.8eV, $7x10^{17}cm^{-2}s^{-1}$), no significant promotion in electron charging is observable, the contribution of the photoexcitation effect of injected electrons in the Si-QDs to the electron redistribution in the floating gate can be ruled out. The generation of hot electrons in channel with visible light irradiation is thought to be a crucial factor for the shorten metastable state, in which the electron tunneling

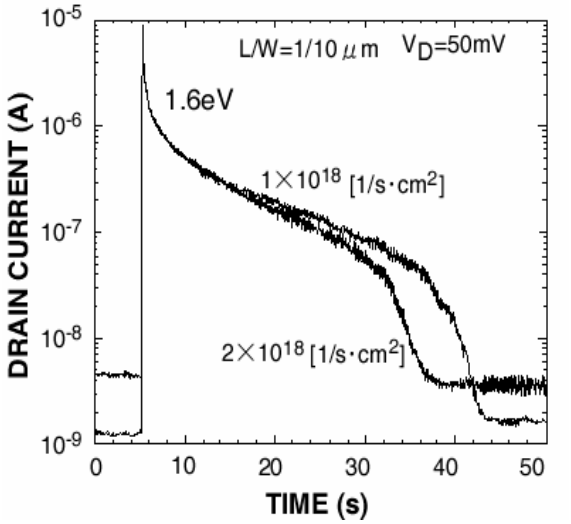

Fig. 9 The temporal changes in the drain current measured at V_G=0V under 1.59eV light irradiation with photon fluxes of $1x10^{18}$ and $2x10^{18}$ cm^{-2}/s after complete discharging of the Si-QDs floating gate at V_g=－4V.

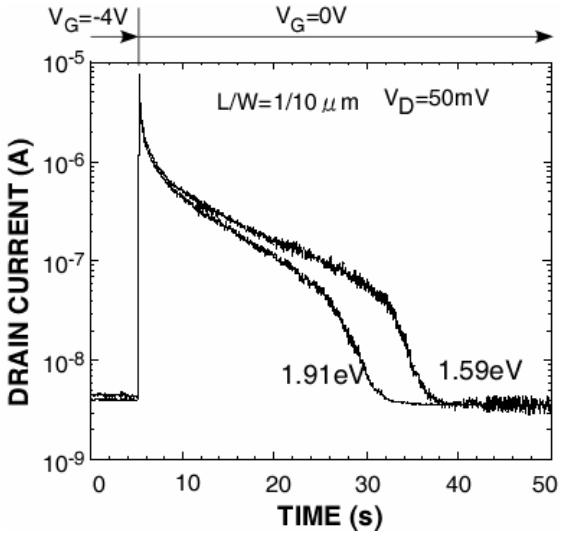

Fig. 10 The temporal changes in the drain current measured at V_g =0V under light irradiation of 1.59eV and 1.91eV photons with the same flux after complete discharging of the Si-QDs floating gate at V_g =－4V.

seems to be controlled by the charging and quantized energy in Si-QDs.

3. Summary

We have prepared nanometer-size Si dots with and without Ge core in a self-assembling manner by controlling the early stages in low pressure chemical vapor deposition on thermally-grown SiO_2. We have evaluated the surface potential change of each of Si dots due to charging or discharging one electron or a few by an AFM/Kelvin probe technique and demonstrated that, for dots consisting of Si clad and Ge core, electrons are stably stored in Si clad

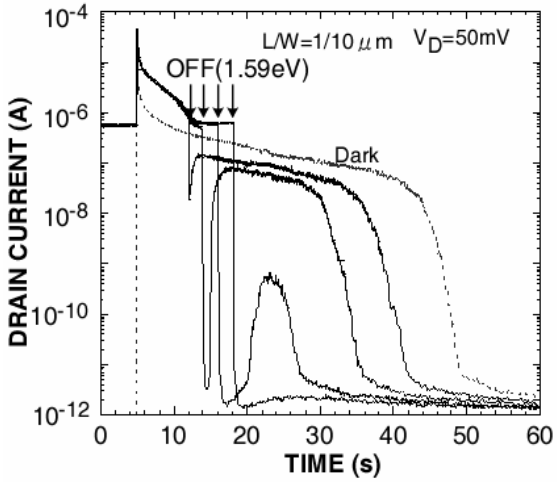

Fig. 11 Temporal change in the drain current, which was measured at V_g =0V when the 1.59eV light irradiation was turned off at various time as indicated by arrows. The result obtained without light irradiation anytime is also shown as a reference.

while holes in Ge core.

Multiple-step electronic charging and discharging characteristics of Si quantum-dots (Si-QDs) floating gates in the MOS capacitors and MOSFETs have been studied in the temperature range of 200～350K. The temporal change in the drain current at a constant gate bias after complete discharging in the Si-QDs floating gate shows specific stepwise reductions accompanied with metastable states in which the drain current also remain unchanged with time until the next quick current reduction. The result indicates that, in the metastable states, injected electrons redistribute in the Si-QDs floating gate with keeping the effective total charge density in the floating gate, and suggests that the Coulomb interaction among electrons stored in neighboring dots plays an important role on the stepwise behavior in electron charging. From the slope of Arrehnius plots of the time for both each electron injection and metastable state, it is likely that a thermal activation process with an energy of 0.3eV is involved in the electron charging to the Si-QDs floating gate. The activation energy (0.3eV) suggests the electron tunneling between different energy states among neighboring Si-QDs, considering the charging energy and quantization energy in Si-QDs. Also, we have demonstrated that the electron charging of the Si-QDs floating gate is accelerated by visible light irradiation and the accelerated charging is mainly attributable to the promotion of electron redistribution in the metastable charged states.

4. Future Research Issues in the COE Program

To further improve the performance of the Si-QDs floating gate MOSFETs, we focus on the precise control of the dot size distribution and the optimization of the dot stacked structure, especially the oxide thickness between the dots. In addition, we will extend our research to

doping control of ionized impurities in Si-based dots for well-discrete charged states. Furthremore, we will fabricate photosensitive functional devices with the stacked Si QDs floating gate for optical interconnect.

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Control of Si Quantum Dot Nucleation by Remote Plasma Treatment

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1. Research Target

The application of Si quantum dots (Si-QDs) as a floating gate to MOSFETs has been attracting much attention because it will lead us to new functionality such as multivalued memory operations even at room temperature [1] or light emission. The growth control of nanometer-scale silicon dots with an areal density as high as ~ 10^{12} cm^{-2} on an ultrathin SiO_2 layer is a crucial factor for the multivalued capability of the Si dots floating gate MOS devices. In our previous work, we demonstrated the fabrication of nanometer-scale Si dots on ultrathin SiO_2 layers by controlling the early stages of low-pressure chemical vapor deposition (LPCVD) using a SiH_4 gas [2]. Also we reported that the SiO_2 surface treatment with a dilute HF solution is very effective to obtain dot density above ~10^{11} cm^{-2} because Si-OH bonds created on the SiO_2 surface act as reactive sites to precursors such as SiH_2 during LPCVD. In addition, by spatially controlling OH- termination on the SiO_2 surface before LPCVD, the selective growth of Si dots has been demonstrated [3]. In fabricating multiple stacked structures of Si dots in SiO_2, it is very necessary to control Si-OH bonds on the SiO_2 surface by a dry process matching with subsequent LPCVD.

In this work, we demonstrate the feasibility of remote H_2 and/or Ar plasma pretreatment for controlling the areal density of Si-QDs. Hydroxylation of the oxide surface, nucleation density and size distribution of Si-QDs as functions of plasma treatment conditions have been evaluated by Fourier transform infrared attenuated total refection (FT-IR-ATR) measurements and atomic force microscopy (AFM), respectively.

2. Research Results

The 4 nm-thick SiO_2 layer was first grown on n^+ Si(100) at 1000°C in dry O_2. The SiO_2 surface was treated with a remote plasma of pure H_2 and/or pure Ar. The plasma was generated by inductively-coupling external single-turn antenna, that is attached to a 10 cmϕ quartz tube and connected to a 60 MHz generator through a matching box. The substrate was placed on the susceptor at a distance of 32 cm away from the position of the antenna. The VHF power and the flow rate were kept constant at 200 W and 100 sccm, respectively. For the H_2 plasma treatment, the gas pressure was changed in the range of 0.1 - 1.0 Torr and the substrate temperature was varied from 27 to 540°C. The time of H_2 plasma treatment is fixed for 5 sec to avoid the reduction of SiO_2 and to minimize plasma damages. For the remote Ar plasma treatment, the VHF power, the gas pressure and the time of the treatment were kept constant at 100 W, 0.5 Torr and 30 sec, respectively. The formation of Si dots on as-grown and plasma treated SiO_2 was performed by LPCVD using pure monosilane at 540°C. During the deposition, the gas pressure was maintained at 0.2 Torr. AFM observations were carried out in air using a Rh - corted Si_3N_4 probe to assess the dot density and uniformity. The influence of chemical bonding of the oxide surface was examined by FT-IR ATR and XPS measurements.

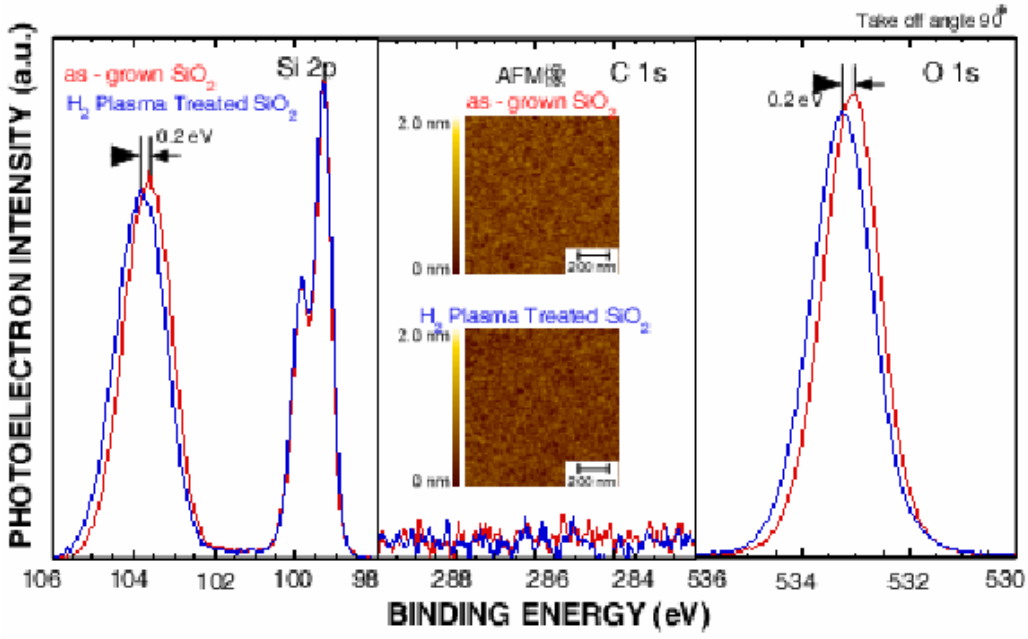

Fig. 1. Si2p, C1s and O1s spectra for the SiO_2 before and after remote H_2 plasma treatment at room temperature for 5 sec, which were taken at photoemission take-off angle of 90°.

Figure.1 shows the Si2p, C1s and O1s spectra for the SiO_2 before and after remote H_2 plasma treatment at room temperature for 5 sec. No significant spectral change in Si2p and O1s spectra and no C1s peak are observed before and after the plasma treatment. These results indicate that the SiO_2 is neither etched by H2 plasma, nor contaminated by carbon. The peak positions of chemically shifted Si2p and O1s signals due to the Si oxidation with respect to metallic Si2p signals from the Si substrate are slightly shifted toward higher biding energy side. This chemical shift can be interpreted as the increase in the component due to OH bonding units by H_2 plasma treatment.

Figure 2 shows AFM images taken after Si dot formation on as-grown SiO_2 and remote plasma treated SiO_2. In the case on as-grown SiO_2, the Si dot density of 6×10^8 cm^{-2} was obtained. When the SiO_2 surface is treated with H_2 plasma prior to LPCVD, the Si dot size is decreased and the density is markedly increased up to 7×10^{10} cm^{-2}. This implies the uniform nucleation of Si-QDs on the SiO_2 surface is enhanced by the remote H_2 plasma treatment. In order to confirm the change in surface bonding states by the plasma treatment, FT-IR-ATR measurement was performed. To avoid the influence of H_2O in the atmosphere, D_2 plasma treatment was used instead of H_2 plasma treatment. The FT-IR-ATR spectrum of the plasma-treated SiO_2 exhibits absorption bands centered at ~2400 and ~2500 cm^{-1}, indicating that the surface is terminated by OD bonds as shown in Fig. 3. From this result, the significant increase in dot density on remote plasma treated SiO_2 surface can be interpreted in terms of the OH termination of

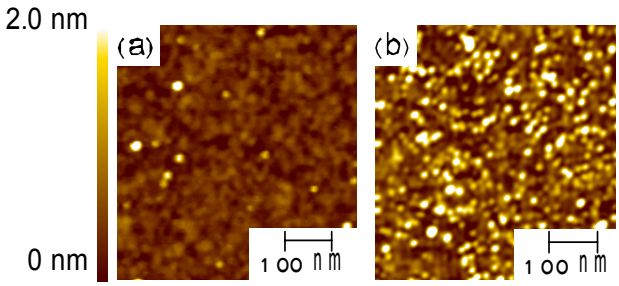

Fig. 2. AFM images of Si dots deposited on (a) as-grown SiO_2 and (b) remote H_2 plasma treated SiO_2.

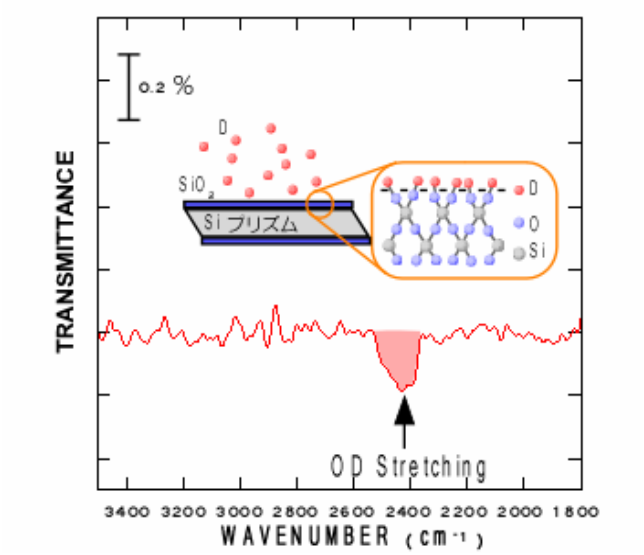

Fig. 3. FTIR-ATR spectrum of D_2 plasma treated SiO_2 on Si(100).

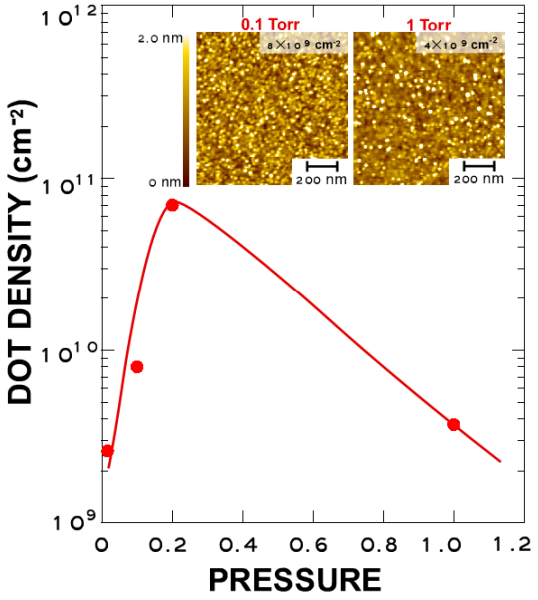

Fig. 4. Si dot density as a function of gas pressure during H_2 plasma treatment.

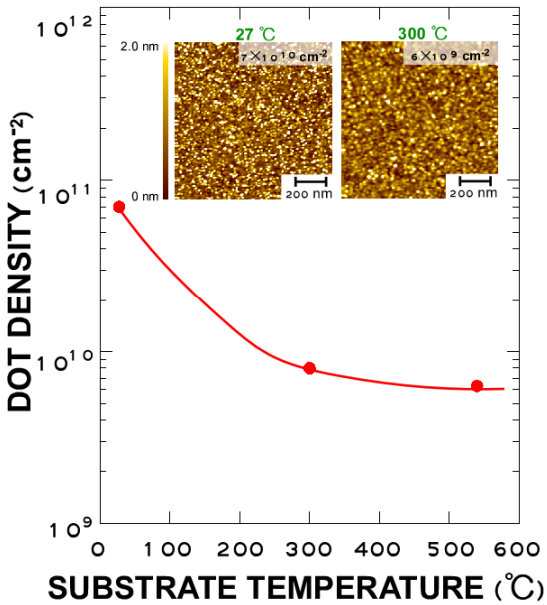

Fig. 5. Si dot density as a function of substrate temperature during H_2 plasma treatment.

the SiO_2 surface and resulting promotion of Si–QDs nucleation.

Then, we investigated the influence of gas pressure during the remote H_2 plasma treatments on Si dots density as shown in Fig. 4. The substrate temperature was kept constant at room temperature. We have observed increasing Si-QDs density with pressure up to 0.2 Torr, then it decreased with pressure. The most likely mechanism is that in the low pressure range, the nucleation is limited by hydrogen radical generation, while in the high pressure range, it is limited by radical diffusion.

Fig.5 shows the influence of substrate temperature during the remote H_2 plasma treatment on the Si-QDs density. The gas pressure was kept constant at 0.2 Torr. Consequently, the Si dots density continually decrease with temperature.

The size distribution of obtained Si dots evaluated from AFM images taken after Si-QDs formation on remote H_2 and/or Ar plasma treated SiO_2 can be fitted to a log-normal function [9] as indicated in Fig. 6. In order to enhance the nucleation density of Si-QDs by remote plasma treatment, Ar plasma, in which ion bombardment may give some effect on the nucleation site formation, was examined in combination with H_2 plasma. In the case of Si-QDs formation on remote Ar plasma treated SiO_2, the Si-QDs density is increased by a factor of 10 compared to the case without the treatment. Note that the H_2 plasma treatment subsequent to the Ar plasma treatment provides a very uniform formation of Si dots with an areal density as high as ~1×10^{11}cm^{-2}. It is likely that weaken bonds and dangling bonds created by Ar plasma exposure react efficiently with radicals, ions and excited molecules generated in H_2 plasma.

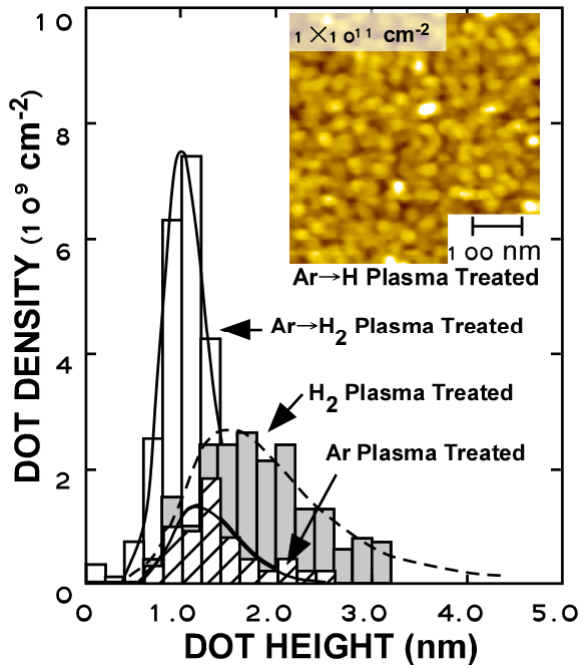

Fig. 5. Distribution of Si-QDs height formed by different pretreatment conditions measured by AFM.

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3. Summary

We demonstrated the control of the nucleation density of Si-QDs by remote H_2 and/or Ar plasma treatment. The density of Si dots was controlled from 6×10^9 to 7×10^{10} cm^{-2} by changing the substrate temperature and pressure at the remote H_2 plasma process. The combination of remote Ar plasma and subsequent H_2 plasma treatments is very effective to achieve a uniform size distribution of Si dots with an areal density of the order of 10^{11} cm^{-2}. These results imply control of Si-QDs nucleation sites utilizing remote plasma treatment is very promising for fabrication of multiple stacked dot structure of Si-QDs.

4. Future Research Plan

In order to realize stack structure of Si quantum dots, process technologies for not only dot formation, but also oxidation of dot surface at low temperature have to be developed. The final goal is to integrate these process technologies into the conventional MOSFETs fabrication and to demonstrate the new functionality in Si-QDs MOSFETs.

5. Published Papers and Patents

① Published Papers

1. K. Makihara Y. Okamoto, H. Nakagawa, H. Murakami, S. Higashi and S. Miyazaki, "Electrical characterization of Ge microcrystallites by atomic force microscopy using a conducting probe": Thin Solid Films 457 (2004)103-108.

② Proceedings

1. K. Makihara, Y. Okamoto, H. Nakagawa, H. Murakami, S. Higashi and S. Miyazaki, "Electrical Characterization of Ge Microcrystallites by Atomic Force Microscopy Using a Conducting Probe" SPSM-16. (2003.) B6-3, p115
2. K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki "Local characterization of electronic transport in microcrystalline germanium thin films by atomic force microscopy using a conducting probe" AWAD2003. (2003). p37
3. K.Makihara, H.Deki, H. Murakami, S.Higasi and S.Miyazaki "Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment" ICSFS to be published.

4. K.Makihara, Y.Okamoto, H. Murakami, S.Higasi and S.Miyazaki “Characterization of germanium nanocrystallites grown on quartz by a conductive AFM probe technique” AWAD 2004 to be published.

③ Patents

1. S. Miyazaki and S. Higashi, Japan Patent Application Number: 2004-091328, “Quantum Dot MOSFET, Memory Device, Photo-Sensor and Their Integrated Circuits”.

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Low resistive gate electrode/high-k gate dielectrics stacked structure and its electron device application

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Introduction

Continuous shrinkage of MOSFET requires the aggressive scaling of gate length and gate dielectric thickness. Shrinkage of poly-Si gate causes various problems, such as increased parasitic resistance, threshold voltage shift, and gate depletion. Poly-SiGe gate is one of the promissing candidate for a gate material of next-generation MOSFETs, because of low resistivity, less poly depletion effect, control of work function and matching with conventional silicon process. However, poly-SiGe has some problems, such as reliability degradation of gate dielectric caused by Ge atoms diffusion from poly-SiGe gate into gate dielectrics when high temperature thermal process. Therefore, Thin silicon buffer layer is formed between gate dielectric and poly-SiGe. For practical application of MISFETs with poly-SiGe, we need to understand mechanism of Ge atom diffusion and control the Ge and dopant profile. In this work, We evaluate Ge diffusion and redistribution effect on poly-Si/poly-SiGe/poly-Si stacked structure. We fabricate MIS capacitor with poly-SiGe gate, and evaluate how does effect germanium redistribution to the electrical properties.

Experimental

The substrates used in this work were p-type and n-type Si(100) wafers in which the acceptor and donor concentrations are $1.5x10^{15}cm^{-3}$ and $5x10^{14}cm^{-3}$, respectively.

After conventional wet-chemical cleaning steps of these wafers, SiO_2 layers in the thickness range of 2.0-4.0nm were grown at 1000℃ in dry O_2 and then poly-Si/SiGe/Si/SiO_2 stacked structures were fabricated on the wafers by the following low-pressure chemical vapor deposition (LPCVD) steps at a substrate temperature of 570℃. First, ~30nm-thick poly-Si as a buffer layer was formed from the thermal decomposition of pure SiH_4 under 0.36torr and subsequently, ~100nm thick poly-SiGe was deposited under 0.42torr of a pure SiH_4 and 10%GeH_4 diluted with He, in which the gas molar ratio of SiH_4 to GeH_4 was varied from 2 to 10, and followed by LPCVD of ~100nm thick poly-Si film as a cap layer with the same conditions as the buffer

Fig1. Cap Poly-Si/Poly-SiGe/Buffer Poly-Si stacked structure.

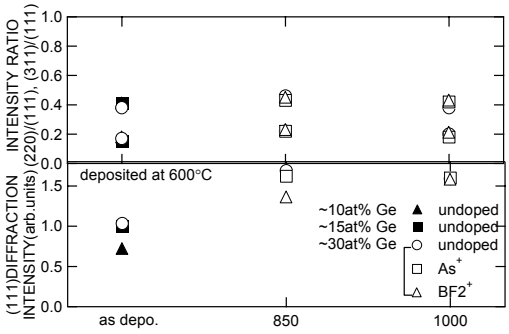

Fig. 2 The (111) peak intensity measured by XRD and the intensity ratio of (220) and (311) peaks to the (111) peak for as-deposited poly-$Si_{1-x}Ge_x$(100nm, x=0.1, 0.15 and 0.3)/SiO_2(2nm)/Si(100) formed by LPCVD at 600°C and annealed samples of x=0.3 after As^+ or BF_2^+ implantation. The annealing time was 30min.

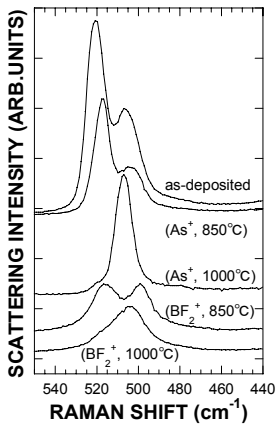

Fig. 3 Raman scattering spectra of as-deposited and N_2 annealed samples of poly-Si/SiGe/Si/SiO_2 stacked structures. The Ge concentration in the poly-SiGe layer before ion implantation was 30 at.%.

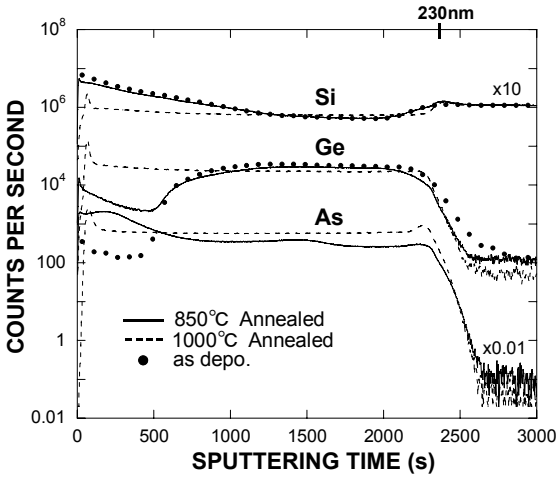

Fig. 4 : SIMS profiles for the as-deposited and N_2-annealed samples after As^+-implantation shown in Fig. 2, which were measured by using Cs^- ions.

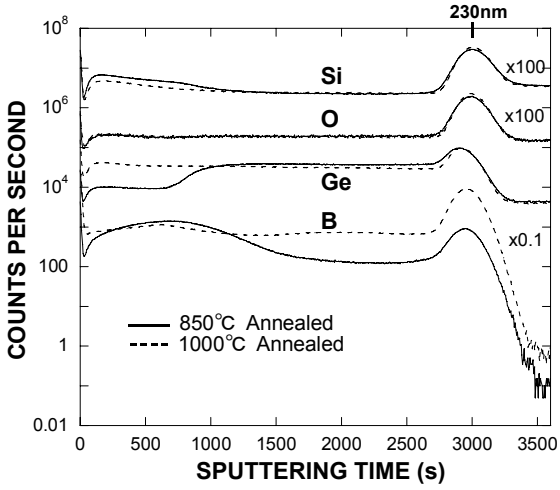

Fig. 5 SIMS profiles for the N_2-annealed sample after BF_2^+-implantation shown in Fig. 2, which were measured by using O^{2-} ions.

layer(Fig. 1). BF_2 ions or As^+ ions accelerated at 30keV or 15keV were implanted with a dose of $5x10^{15}cm^{-2}$ to the stack structures so prepared and followed by activation annealing in the temperature range of 800~1000℃ for 30 or 10 min in N_2 ambient. The crystallinity of the stacked film was evaluated by X-ray diffraction(XRD) using a Cu Kα line and Raman scattering measurements using a 441.6nm light from a He-Cd laser. The depth profiles of Ge, Si and dopant atoms in the stack structures were evaluated by secondary ion mass spectroscopy(SIMS) using Cs^+ or O^{2-} ions beam at 1kV and energy dispersive x-ray (EDX) analysis in a transmission electron microscope (TEM) operated at 200kV. The resistivity measurements for the annealed samples were performed using a four-point probe method. Also, the gate leakage current and capacitance-voltage characteristics of fabricated MOS capacitors were evaluated to check the influence of the Ge redistribution on the gate oxide.

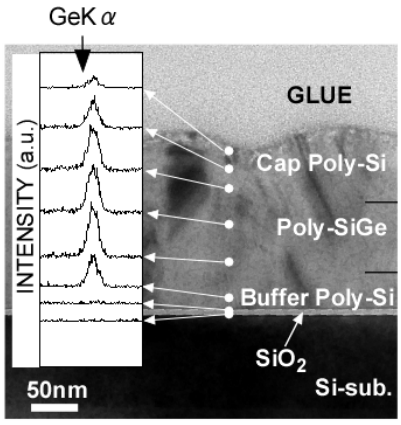

Fig. 6: Cross-sectional TEM image of the stack structures on 4nm-thick SiO_2/Si(100) annealed at 800℃ for 10min after BF_2^+ implantation and EDX spectra taken at different positions. The Ge concentration in as-deposited SiGe layer was ~30%.

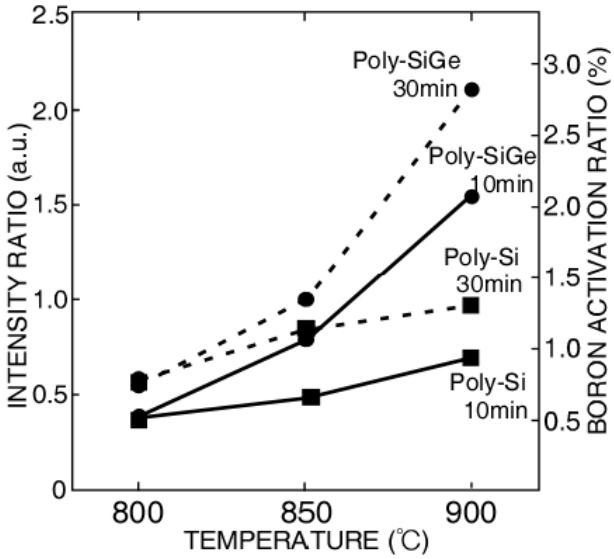

Fig. 7: The Raman intensity ratio of the peak due to acceptors to that due to the Si TO phonon mode for poly-Si and poly SiGe samples annealed at different temperatures for 10 and 30min. after BF_2^+ implantation. The ratio corresponds roughly to the boron activation ratio. The bottom oxide thickness was 4.0nm and the Ge concentration in as-deposited SiGe layer was ~30%.

Results and Discussion

XRD measurements for 250nm-thick $Si_{1-x}Ge_x$ single film formed on 2nm-thick SiO_2 confirm an improvement of the crystallinity by post deposition anneal and no significant different in the crystallinity between the annealed samples as shown in Fig. 2.

The relative intensity of the diffraction peaks due to (111), (220) and (311) planes indicates that polycrystallites are oriented preferentially to the (111) direction, but not strongly, and the preferential orientation is not changed by N_2 anneal subsequent to ion implantation. In 850℃ annealed cases, the

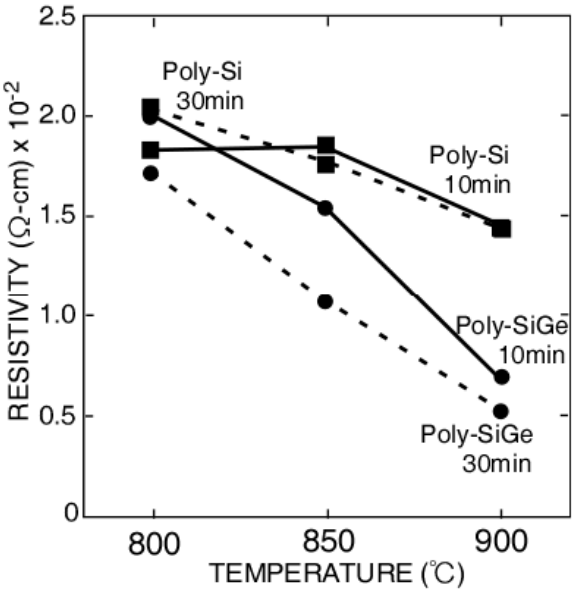

Fig. 8: The resistivity of the samples shown in Fig. 5 measured using a four-point probe.

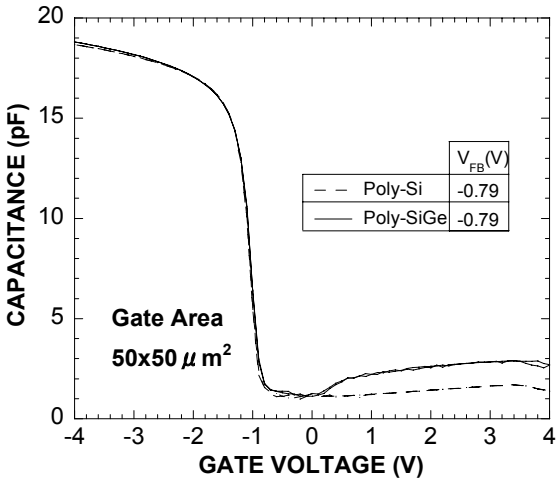

Fig. 9: C-V characteristics of MOS capacitor with n^+poly-Si gate and n^+poly-SiGe gate.

BF_2 implanted sample show a slightly degraded crystallinity in comparison with undoped and As+ implanted samples.

This can be interpreted in terms of a negative impact of implanted fluorine atoms on the crystallization.

Changes in the Raman scattering spectra for poly-Si(100nm in thickness)/poly-$Si_{0.7}Ge_{0.3}$(100nm)/poly-Si(30nm) /SiO_2(2nm)/Si(100) show the diffusion and incorporation of Ge atoms in the Si layer by N_2 anneal as represented in Fig. 3. For as-deposited sample, two sharp peaks due to TO phonons involving Si-Si stretching motions in the poly-Si cap and in the poly-SiGe layers are clearly observable at ~520cm^{-1} and ~505cm^{-1}, respectively, where the signals from the bottom poly-Si layer can not be detected because of the probing depth of the

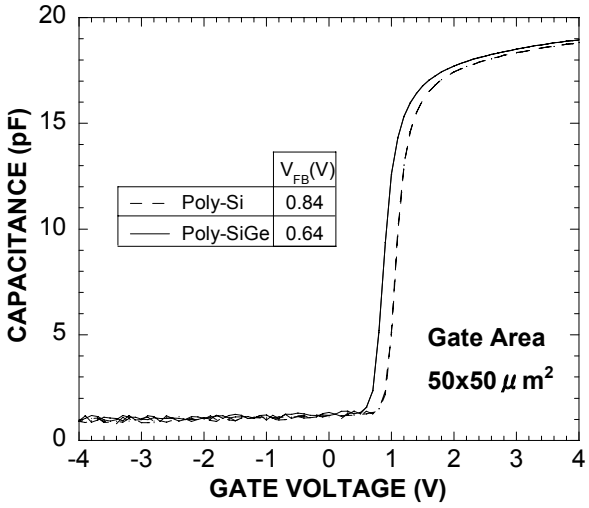

Fig. 10 C-V characteristics of MOS capacitor with p$^+$poly-Si gate and p$^+$poly-SiGe gate.

excitation laser light.

After 850℃ anneal, the TO phonon peaks are shifted towards the lower wavenumber side. The observed peak shift implies the diffusion of Ge atoms into the poly-Si cap layer.

Since, for the BF_2 implanted case, the TO phonon peak at the higher wavenumber side is significantly decreased, the Ge incorporation to the cap is likely to be more pronounced than the As^+ implanted case.

Notice that, by N_2 anneal at 1000℃, the signals from TO phonons in Si-Ge network becomes dominant, suggesting that Ge atoms diffuse uniformly in the cap layer as also confirmed by SIMS measurements.

As shown in SIMS profiles of Figs. 4 and 5, in both BF_2^+ and As^+ implanted cases, the Ge concentration in the cap layer is increased remarkably by 850℃ anneal. Obviously, by 1000℃ anneal, a quite uniform depth profile for Ge atoms is obtained as also seen in that for B or As atoms.

In addition, EDX measurements indicate that, even at annealing temperature as low as 800℃, Ge atoms can diffuse into the cap and bottom Si layers and some reaches near the top surface through the 100nm thick cap layer, presumably because point defects generated by ion implantation can enhance the atom diffusion, and that no incorporation of Ge atoms in the SiO_2 layer was detected as displayed in Fig. 6.

In the Raman scattering measurements, the signals due to the electron transition between acceptors and the valence band appear at ~610cm^{-1}[8]. For BF_2^+ implanted samples, the intensity ratio of the acceptor-derived peak to the Si TO phonon peak is thought to be related to the amount of ionized acceptors. As indicated in Fig. 7, the boron activation in poly-SiGe with annealing temperature is remarkable compared with the poly-Si case. By 900℃ anneal, the boron activation level in the poly-SiGe becomes about twice as large as that in poly-Si although there is no significant difference in the boron activation between poly-Si and poly-SiGe

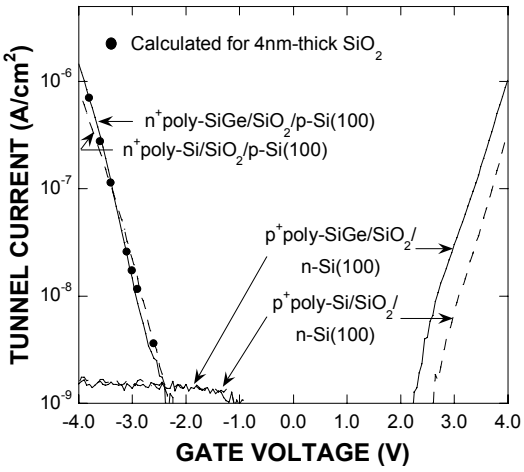

Fig. 11:I-V characteristics for the samples same as fig. 11 and the theoretical curve.

in 800℃ anneal. In consistency with this result, reasonably lower resistivities were measured for poly-SiGe annealed at temperatures higher than 850℃ in comparison to the cases of poly-Si (Fig. 7).

Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MOS capacitors with n^+ and p^+ poly-SiGe stack structures on 4nm-thick SiO_2 were compared to those of controlled MOS capacitors with poly-Si gate in order to confirm less impact of the Ge redistribution in the stack gate on gate SiO_2 in the annealing condition at 850℃ for 30min (Figs. 8). For the cases with n^+ gate, no difference in flat-band voltage(V_{FB}) between poly-Si and poly-SiGe gates was observed. On the other hand, for the cases with p+ gate, a decrease in the V_{FB} of 0.2V was measured for the poly-SiGe gate in comparison to the poly-Si gate, being interpreted in terms of the Fermi level shift attributable to the energy shift of the valence band edge as predicted by the Ge concentration [9]. Thus, the result of Fig. 8 indicates that, by 850℃ for 30min, Ge atoms are diffused well near the interface between the buffer layer and SiO_2.

As for I-V characteristics of the MOS capacitors, the gate leakage current due to Fowler-Nordheim(F-N) tunnel is only observed, indicating the impact of Ge redistribution in the gate stack on the gate leakage is negligible(Fig. 9). In addition, for p^+ poly-SiGe gate, an increase in current level at positive gate voltages, which reflect the V_{FB} shift of 0.2V, is measured compared with the p^+poly-Si gate case, while no difference in the leakages current level at negative gate biases is obtained because the tunneling current is limited by hole generation rate in the substrate. For n^+ poly-Si and poly-SiGe gates the I-V characteristics are almost identical as seen in the C-V characteristics.

Summary

The Ge redistribution in the poly-SiGe stack structure, which consists of 100nm-thick poly-Si cap, 100nm-thick poly-SiGe and 30nm-thick poly-Si buffer, on ultrathin SiO_2/Si(100) by N_2 anneal in the temperature range of 800-1000℃ has been studied. By 1000℃ anneal for 30min, a uniform depth profile of Ge atoms throughout the whole sack structure was obtained. By 850℃ anneal for 30min, expected I-V and C-V characteristics of MOS capacitors with p^+ and n^+ poly-SiGe stack gate with a Ge content of ~30at.% were confirmed. The flat band voltage shift of 0.2V was evident only for p^+ poly-SiGe, being attributable to the difference in the energy band structure between Si and $Si_{0.7}Ge_{0.3}$, without extra current leakage.

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Achievement

① Published Papers

H. Murakami, T. Mihara, S. Miyazaki and M. Hirose, *Jpn. J. Appl. Phys.* Vol. 41 No. 5A (2002)pp. L512-L514

② Proceedings

1. H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi and S. Miyazaki, *2004 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, to be published.*

Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment

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Seiichiro Higashi (Assoc. Prof., Graduate School of Advance Science of Matter),
Seiichi Miyazaki(Professor, Graduate School of Advanced Sciences of Matter)

1. Research Target

The application of Si quantum dots as a floating gate to MOSFETs has been attracting much attention because it will lead us to new functionality such as multivalued memory operations even at room temperature [1]. The growth control of nanometer-scale silicon dots with an areal density as large as ~10^{12} cm^{-2} on an ultrathin SiO_2 layer is a crucial factor for the multivalued capability of the Si dots floating gate MOS devices. In our previous work, we demonstrated the fabrication of nanometer-scale Si dots on ultrathin SiO_2 layers by controlling the early stages of low-pressure chemical vapor deposition (LPCVD) using a SiH_4 gas [2]. Also we reported that the SiO_2 surface treatment with a dilute HF solution is very effective to obtain dot density above ~10^{11} cm^{-2} because Si-OH bonds created on the SiO_2 surface act as reactive sites to precursors such as SiH_2 during LPCVD. In addition, by spatially controlling OH- termination on the SiO_2 surface before LPCVD, the selective growth of Si dots has been demonstrated [3]. In fabricating multiply stacked structures of Si dots in SiO_2, it is very necessary to control Si-OH bonds on the SiO_2 surface by a dry process matching with subsequent LPCVD.

In this work, we demonstrate the feasibility of remote H_2-plasma pretreatment for controlling the areal density of Si dots.

2. Research Results

The SiO_2 surface was treated with a remote plasma of pure Ar and/or pure H_2. The plasma was generated by inductively-coupling between an external single –turn antenna attached to a 10 cmϕ quartz tube and a 60 MHz generator through a matching box. The substrate was placed on the susceptor at a distance of 32cm away from the position of the antenna. The RF power and the flow rate were kept constant at 200 W and 100sccm, respectively. The gas pressure was changed in the range of 0.1-1.0 Torr and the substrate temperature was varied from 27 to 540 ºC. The time of the remote plasma treatment is fixed for 5s to avoid the reduction of SiO_2 and to minimize plasma damages. The formation of Si dots on as-grown and plasma treated SiO_2 was performed by LPCVD using pure monosilane at 540 ºC. During the deposition, the gas pressure was maintained at 0.2 Torr. Figure 1 shows AFM images taken after Si dot formation on as-grown SiO_2 and remote plasma treated SiO_2. In the case on as-grown SiO_2, the Si dot density of 6 × 10^8 cm^{-2} was obtained. When the SiO_2 surface is treated with H_2 plasma prior to LPCVD, the Si dot density is markedly increased up to 7 × 10^{10} cm^{-2}. FT-IR-ATR spectra confirm the formation of Si-OH bonds by the H_2 plasma treatment. In the case of Ar plasma treatment in which ion bombardment may occur and induce some damages, the Si dot density is increased by a factor of 10. The results imply that an incidence of atomic hydrogen generated in H_2 plasma to the SiO_2 surface play an important role in the creation of the reactive sites such as OH bonds and hydrides for the Si dot formation. Note that the H_2 plasma treatment subsequent to the Ar plasma treatment provides a very uniform formation of Si dots with an areal density as high as ~1 × $10^{11}$$cm^{-2}$. This is interpreted in terms of the improved coverage of OH bonds on the SiO_2 surface as confirmed by FT-IR-ATR measurements. It is likely that weaken bonds and dangling bonds created by Ar plasma exposure react efficiently with radicals, ions and excited molecules generated in H_2 plasma.

In conclusion, the combination of remote Ar plasma and subsequent H_2 plasma treatments is very effective to achieve a uniform size distribution of Si dots with an areal density of the order of $10^{11}$$cm^{-2}$.

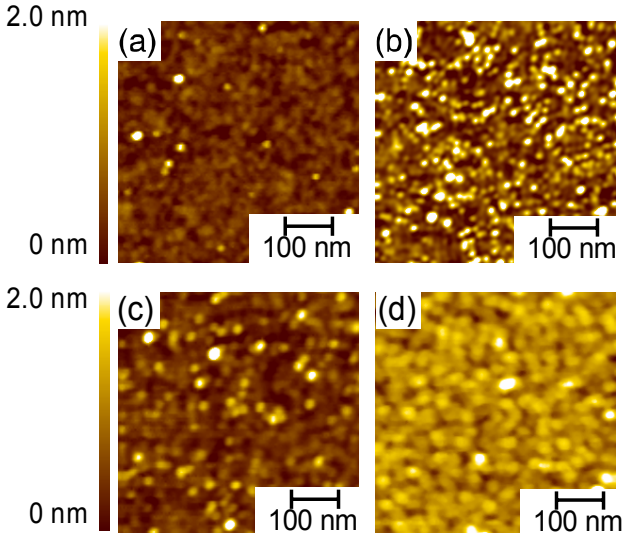

Fig. 1 AFM images of Si dots deposited on SiO_2 as-grown (a), remote H_2 plasma treated (b), Ar plasma treated (c), Ar plasma + H_2 plasma treated (d).

4. Conclusion

We demonstrated the control of the nucleation density of Si-QDs by remote H_2 and/or Ar plasma treatment. The density of Si dots was controlled from 6 × 10^9 to 7 × 10^{10} cm^{-2} by changing the substrate temperature and pressure at the remote H_2 plasma process. The combination of remote Ar plasma and subsequent H_2 plasma treatments is very effective to achieve a uniform size distribution of Si dots with an areal density of the order of 10^{11} cm^{-2}.

5. Relation of the COE program with the result

These results imply control of Si-QDs nucleation sites utilizing remote plasma treatment is very promising for fabrication of multiple stacked dot structure of Si-QDs.

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7. Published Papers and Patents

① Published Paper

1. K. Makihara, Y. Okamoto, H. Nakagawa, H. Murakami, S. Higashi and S. Miyazaki, “Electrical characterization of Ge microcrystallites by atomic force microscopy using a conducting probe”: Thin Solid Films 457 (2004)103-108

② Proceedings

1. K. Makihara, Y. Okamoto, H. Nakagawa, H. Murakami, S. Higashi and S. Miyazaki, “Electrical Characterization of Ge Microcrystallites by Atomic Force Microscopy Using a Conducting Probe” SPSM-16. (2003.) B6-3, p115
2. K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki “Local characterization of electronic transport in microcrystalline germanium thin films by atomic force microscopy using a conducting probe” AWAD2003. (2003). p37
3. K.Makihara, H.Deki, H. Murakami, S.Higasi and S.Miyazaki “Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment” ICSFS to be published.
4. K.Makihara, Y.Okamoto, H. Murakami, S.Higasi and S.Miyazaki “Characterization of germanium nanocrystallites grown on quartz by a conductive AFM probe technique” AWAD 2004 to be published.

③ Patents

1. K. Makihara, K. Takeuchi, M. Ikeda, H. Murakami and S. Miyazaki, The 20h Symposium on Plasma Processing p. 321.
2. K. Makihara, K. Takeuchi, M. Ikeda, H. Murakami and S. Miyazaki, The Japan Society of Applied Physics (The 50th spring meeting, 2003) No2, p975
3. K. Makihara, Y. Okamoto, H. Murakami, S. Higashi and S. Miyazaki, The Japan Society of Applied Physics (The 64th Autumn meeting, 2003) No2, p402
4. K. Makihara, T. Sibaguchi, H. Murakami, S. Higashi and S. Miyazaki, The Japan Society of Applied Physics (The 51st spring meeting, 2004) No2, p839
5. K. Makihara, H. Deki, H. Murakami, S. Higashi and S. Miyazaki, The Japan Society of Applied Physics (The 51st spring meeting, 2004) No2, p853

Investigation on hard breakdown mechanism of high-k gate by conductive-AFM

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Seiichi Miyazaki(Prof., Graduate School of Advanced Sciences of Matter)

1. Research Target

Following the device scaling laws, continuing scaling down of the MOSFET device with the minimum feature size of 90 nm and below would require equivalent oxide thickness of less than 15A. SiO_2 will soon reach its physical limitation such as high leakage current and reliability concerns. High-k materials with high physical thickness have been widely researched as gate to alternative Silicon oxide. So far, a lot of works focus on silicon oxide breakdown mechanism, but it is few for high-k dielectric, which is very important to high-k transistor reliability.

In ours work, high-k MIS structure hard breakdown path was investigated by conductive-AFM with conductive tip. According to the path area, leakage path density and the I-V curve of leak spot from conductive-AFM result, high-k hard breakdown mechanism will be analyzed following the experiment data.

2. The Connection with COE Program and Achievements

High-k material will be applied to quantum dot memory device as the control oxide layer. In my group this work is in progressing. High-k breakdown mechanism will supply theoretical support with the application of high-k to dot memory.

3. Research Results

MIS capacitance with stack high-k gate of HfAlO/SiON were made in this work. Fig.1 shows the MIS structure.

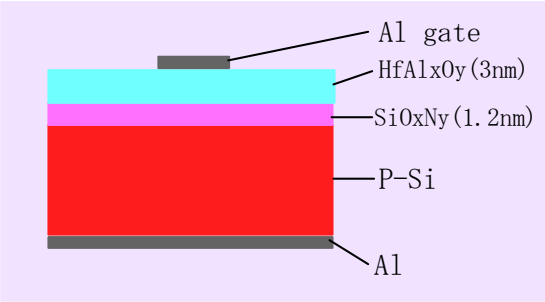

Fig.1 Schematic diagram of stacked high-k gate MIS structure

Hard breakdown was happened at about –4.5 volt showed as fig. 2, the EOT of high-k film was estimated about 2.1nm by C-V characteristic curve (fig. 3). The breakdown electric field was about 20MV/cm. The leakage current was increased significantly after hard breakdown.

Conductive filament path was employed as hard breakdown mode. In this mode, silicon and metal filament path was supposed. According this mode, the leakage current density function after hard breakdown is given by

JpostHD＝(1-Aratio)JFN＋AratioJSM

Where Aratio is the proportion of hard breakdown path area with gate total area, JSM is the schottky current density at breakdown leakage spot.

The Aratio was estimated about less than10^{-7}, in gate area, presumably there are only one or two leakage spot, which means one or two leakage channel through the hard breakdown. In the work, samples with 1 mm diameter gate were fabricated, but searching the leakage spot will be difficult. Because the resolution limit of equip, By far I haven't found the spot by conductive-AFM.

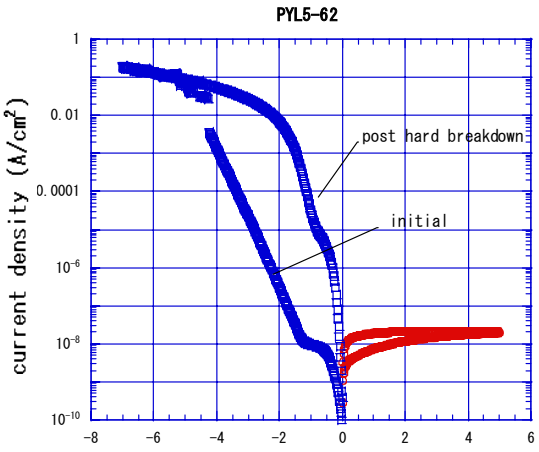

Fig.2 characteristic of current-voltage

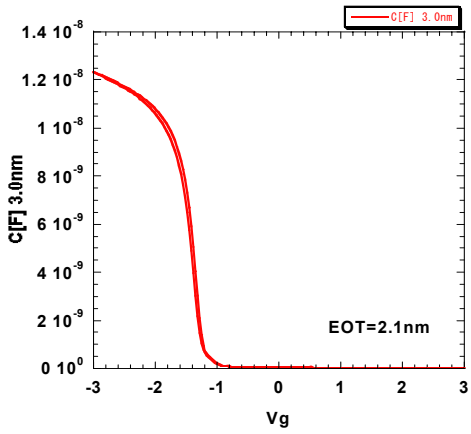

Fig.3 characteristic of capacitance-voltage

4. Research Plan in Future

We consider shrinking the gate area, and then search the hard breakdown path by conductive-AFM to confirm the mechanism of high-k breakdown.

In further, we will apply the high-k to dot memory, and study the characteristic of high-k dot memory (high-k as alternative of CVD silicon oxide in conventional dot memory device).

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Intra/Inter-Chip Wireless Interconnect System for ULSI (1)
－Si Integrated Antenna－

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1. Research Target

According to the scaling rule of silicon ultra-large scale integrated circuits (ULSI) [1,2], transistor performance can be improved by reducing the feature sizes, but interconnect performance is degraded due to the increase of resistances (R) and capacitances (C) of the scaled interconnects. Thus a new technology solution must be adopted to overcome the delay problem of conventional interconnect system .

The goal of this research is to develop a signal transmission technology which can distribute the clock frequency higher than 10 GHz to circuit blocks as well as among ULSI chips. Furthermore, a novel signal transmission technique which can realize reconfigurable wireless interconnects having multiple-channels. For this purpose an ultra wideband (UWB) wireless interconnect systems using integrated antennas is developed [3-6] for future ULSI.

However, there are several issues to be solved. One of them is the transmission loss of electromagnetic waves in Si substrates because Si is a lossy material due to its conductivity. and lossy material properties. Measurement techniques must be developed for antenna propagation through Si and the influence of Si on the transmission characteristics. The transient response of the transmitting and receiving dipole antennas fabricated on a conductive Si substrate are also investigated so that baseband communication between ULSIs by UWB digital signal can be achieved.

Research on intra/inter-chip wireless interconnect system is a new interdisciplinary field so that it is necessary to apply not only electromagnetic wave transmission and antenna theory but also material science and Si integrated circuits technology.

2. Research Results

A concept of intra/inter-chip wireless interconnects using integrated dipole antennas in SI ULSI is shown in Fig. 1. Figures 2 and 3 show layout pattern and a plan-view of transmitting and receiving antennas on a Si substrate. Antenna test structures were fabricated on 260 μm thick Si wafer with a resistivity of 10Ω-cm or 2.29k Ω-cm using 0.5 μm field oxide. Proton implantation was then performed on the patterned wafer with a fixed dose of 10^{15} cm^{-2} and at a fixed energy of 17.4 MeV in a cyclotron chamber from the back side of the wafer. The wafers were kept in a circular flange covered by aluminum sheet and implantation was done in six steps by changing the aluminum absorber thickness in order to provide a uniform proton profile throughout the entire depth of the Si substrate. The thickness of the aluminum absorber was 1630 μm during the first implantation step. In each subsequent implantation steps, the thickness of the aluminum absorber was reduced by 40 μm from the previous value. The concentration profile of implanted proton in Si was calculated using the public domain software named Stopping and Range of Ions in Matter. A schematic cross-sectional diagram of proton implantation into Si substrate is shown in Fig. 4 and the resulting profile of the proton ion implantation at $1x10^{12}/cm^2$ of proton dose is shown in Fig. 5. Figure 6 shows a measurement setup for S-parameters of antennas. It consists of HP8510C Vector Network Analyzer, 180° Hybrid Couplers (6.0-26.5GHz), probe station and Signal-Signal probes. Wafers were measured on wood (2.6 mm thick) on the metal chuck of the probe station. The relative dielectric constant of wood was measured as 2.15 at 1 GHz. Figure 7 shows the measured transmission coefficient (S_{21}) of dipole antennas on a standard and a proton implanted Si substrates as a function of frequency. The transmission coefficient increases +20 dB at 20 GHz by proton implantation. Figure 8 shows the transmission coefficient versus antenna distance. The proton implantation could eliminate the effect of distance on the transmission gain. Figure 9 shows the measured result of the antenna transmission gain at 20 GHz versus the resistivity of the Si substrate with antenna lengths of 1.0, 2.0 and 3.0 mm and is fixed antenna distance of 10.0 mm. The every antenna length, the antenna transmission gain becomes saturated after the resistivity of the Si substrate exceeds 132 Ω·cm. Specifically, when antenna length is 3.0 mm and antenna distance is 3.0 cm, the antenna transmission gain is -43 dB for the Si substrate resistivity of 10 Ω-cm. On the other hand, the antenna transmission gain is -24 dB for the Si substrate resistivity of 2.29 kΩ-cm. The antenna transmission gain was improved by a maximum of +25 dB by making the resistivity of the Si substrate high.

Intra/Inter-chip configurations are shown in Fig. 10, and the measured inter-chip transmission coefficients as a function of frequency were shown in Fig. 11. To improve the inter-chip transmission coefficient of integrated antenna we have increased the resistivity of Si substrate to extremely high value by proton implantation throughout the entire depth of the Si substrate. The proton dose was 5×10^{14} cm^{-2} and implantation energy was 17.4 MeV. The measured value of resistivity after proton implantation was about 65 KΩ-cm. After proton implantation the transmission coefficient for 2 mm long antenna pair separated by 10 mm is increased by 13.4 dB and 21.8 dB at 20 GHz and 25 GHz, respectively. Received sinusoidal signals at the receiving antennas on the

standard and proton implanted Si substrates were shown in Figs. 12(a) and 12(b), respectively. The peak-peak amplitude of the inter-chip transmission of received sinusoidal signal at 20 GHz at the receiver antenna on standard Si was 3.15 mV and 1.04 mV at a distance of 3 mm and 10 mm respectively. When high resistivity Si substrate is used, at a distance of 10 mm the received signal peak-peak amplitude increased by 6 folds to 6.88 mV.

3. **Summary and Future Plan**

A novel signal transmission technology among ULSI chips was developed, which could distribute clock frequencies higher than 10 GHz to circuit blocks as well as among ULSI chips. An ultra wideband (UWB) wireless interconnect system using integrated antennas was developed for reconfigurable multi-channels. It was demonstrated for the first time that a sinusoidal wave clock having frequency of 20GHz could be transmitted between Si chips.

The influence of Si substrate resistivity on the transmission characteristics of integrated antennas was investigated. It is found that Si substrates with the resistivity of 75 Ω-cm as well as the proton implanted Si substrate can minimize the Si substrate loss. A feasibility study of inter-chip characteristics of the integrated antennas was also conducted and consistent results with intra-chip were obtained. The results of transient responses of UWB signals will be reported at IEEE Antenna Propagation Society Conference in June, 2004.

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[5] Brian A. Floyd, Chih-Ming Hung and Kenneth K.O. IEEE Journal of Solid State Circuits, vol 37, No. 5, May 2002, PP. 543-552.

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5. Achievement

Published papers

1. S. Watanabe, A.B.M.H. Rashid and T. Kikkawa, “Effect of High Resistivity Si substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects, Japanese Journal of Applied Physics Vol. 43, No. 4B, 2004, pp.2297-2301.

2. A.B.M.H. Rashid, S. Watanabe and T. Kikkawa, “Characteristics of Si Integrated Antenna for Inter-Chip Wireless Interconnection,” Japanese Journal of Applied Physics Vol. 43, No. 4B, 2004, pp.2283-22287.

3. A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "High Transmission Gain Integrated Antenna on Extremely High Resistivity Si for ULSI Wireless Interconnect", IEEE Electron Device Letters, Vol. 23, No.12, December 2002, pp.731-733.

4. A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, "Characteristics of Integrated Antenna on Si for On-Chip Wireless Interconnect", Japanese Journal of Applied Physics, Vol. 42, No. 4B, April 2003, pp. 2204-2209.

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7. A.B.M. H. Rashid, S.Watanabe and T. Kikkawa, “Inter-chip Wireless Interconnection using Si Integrated Antenna, ” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, Tokyo, Sept. 16-18, 2003, pp. 394-395.

8. S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, “Effect of High Resistivity Si Substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects,” Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, , Tokyo, Sept. 16-18, 2003, pp. 668-669.

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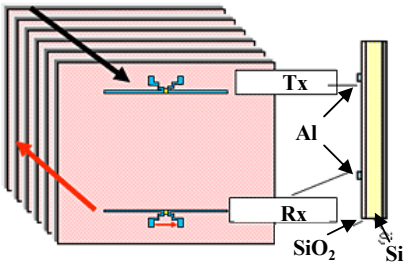

Fig. 1 The concept of inter-chip wireless signal transmission in stacked chip packaging.

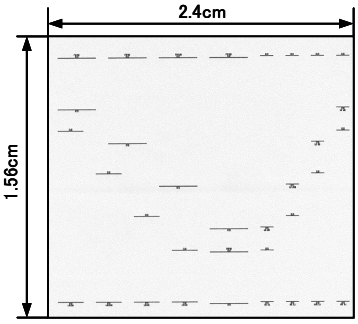

Fig.2. Layout pattern of integrated antennas for intra-chip transmission on silicon.

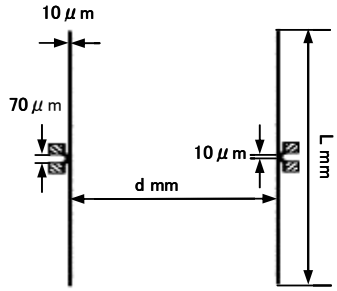

Fig.3. A plan-view of transmitting and receiving antennas on a Si substrate.

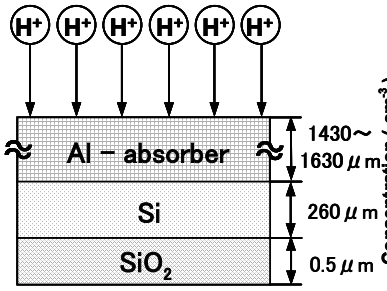

Fig.4. Schematic diagram of proton implantation.

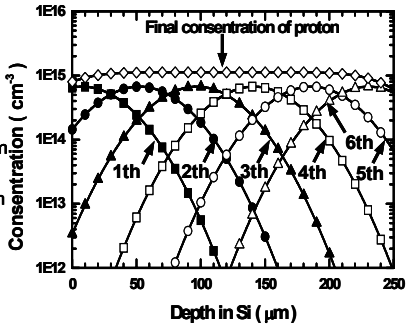

Fig.5. Simulated concentration profile of proton in Si.

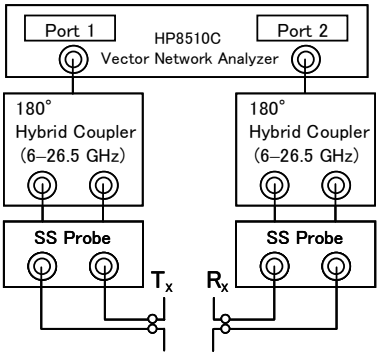

Fig.6. Experimental set-up for inter /intra-chip antenna characterization.

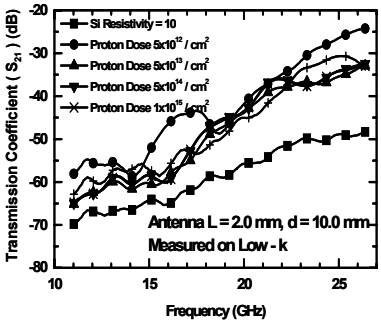

Fig.7 Transmission coefficient (S_{21}) versus frequency. (Effect of proton dose) (Antenna L=2.0mm, d=10.0mm)

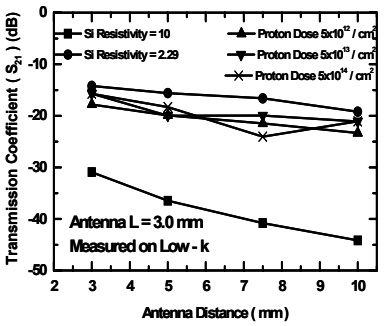

Fig.8 Transmission coefficient versus Antenna Distance. (Effect of proton dose) (Antenna L=3.0mm)

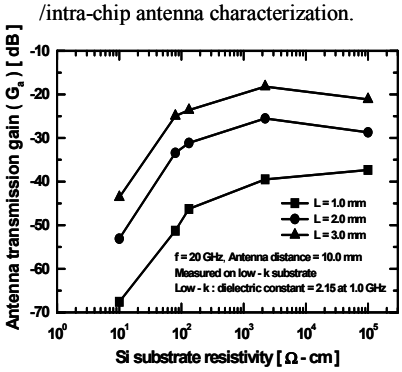

Fig. 9 Antenna transmission gain of dipole antenna versus Si substrate resistivity (ρ) with antenna length (L) as a parameter .

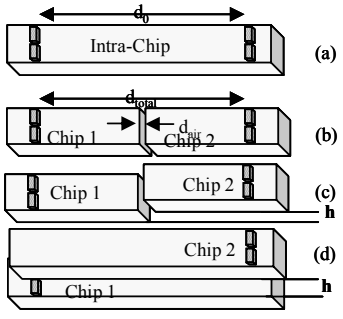

Fig.10 Different configurations used for evaluation. (a) Intra-chip, (b) Inter-chip on the same plane (h=0), (c) Inter-chip with height between the chips h=2.6mm, (d) Inter-chip overlapped with h=2.6 mm.

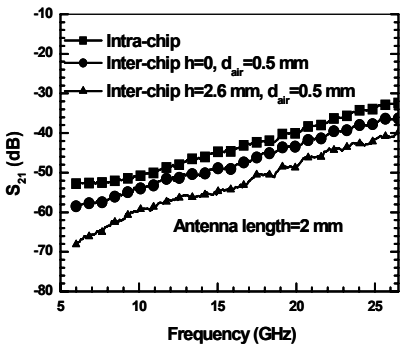

Fig. 11 Measured transmission coefficient of inter-chip wireless signal transmission in various configurations.

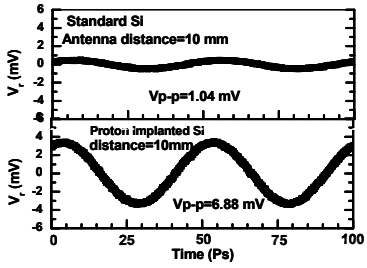

Fig.12 Peak to peak amplitude of received signal increases from 1 mv to 6.9 mV by using proton implanted Si.

Intra/Inter Chip Wireless Interconnect System for ULSI (2)
－A CMOS Ultra Wideband Transmitter－

Pran Kanai Saha (COE Researcher) and Nobuo Sasaki (COE Researcher),
Takamaro Kikkawa (Professor, Research Center for Nanodevices and Systems,
Graduate School of Advanced Sciences of Matter)

1. Research Target

The delay time associated with the parasitic resistance, capacitance and inductance of conventional interconnect system will become the primary obstacle for high speed data and clock distribution among different sub-circuits within a chip and among the chips for future ULSI. Thus a new design or technology solution must be adopted to overcome the delay problem of conventional interconnect system. An ultra wideband (UWB) wireless interconnect systems using integrated antenna shown in Fig. 1 could be a novel solution to avoid any parasitics delay [1] for future ULSI.

In this study we report a single chip UWB transmitter circuit based on time hopping spread spectrum technique [2] for wireless interconnect system as shown in Fig. 2. Thus a new technique based on CMOS technology is also developed to generate the monocycle pulse with a target monocycle pulse center frequency of 5 GHz. As a result, it leads us to design a single chip transmitter for developing the intra/interchip wireless interconnect system of future ULSI.

2. Research Results

This transmitter transmits very short duration Gaussian monocycle pulses with wide bandwidth as a signal without a sinusoidal carrier. The circuit simulation is done from the extracted layout netlist of designed transmitter by HSPICE for TSMC 0.18 μm CMOS process. The simulation results are shown in Figs. 3–10. The frequency stability of the frame clock generated by VCO is an important factor in UWB system. From simulation it is found that the frequency stability with change of V_{dd} and temperature is about 5% in the worst case. The phase noise of the VCO for 100KHz offset is found as about –93.6 dBc/Hz. Precise delay generation is required to generate the time shifting frame clock. Thus voltage controlled delay line is used and its response is shown in Fig. 5. Linear feedback shift registers which consists of four clocked D-type Flip-Flop along with an exclusive-or logic is designed to generate pseudorandom (PN) sequence. It is observed that the generated PN sequence satisfies all its randomness properties such as balance , run and co-relation property. The 8 to 1 multiplexer which is designed using NAND and NOR gate selects the time hopped frame clock according to PN sequence. The time shifted pulse train due to PN sequence and PPM is obtained from the output of 2 to 1 multiplexer. The monocycle pulse generator circuit consists of RLC network with RC filter, pass gate and short rectangular pulse (SRP) and Gate Control Pulse (GCP) generator is designed as shown in Fig. 8 to produce damped sinusoidal like waveform from the time hopped signal (THS) which contains information. The Fig. 9 shows that the generated monocycle pulse (MCP) is symmetry. The FFT of the generated monocycle pulse reveals that it has wide bandwidth characteristics as shown in Fig. 10. The designed transmitter performance data are given in Table. I. The chip die photograph is shown in Fig. 11.

Table I: Transmitter performance data

UWB system	Time hopping Impulse
Carrier Frequency	No carrier
Transmitter Signal bandwidth	3.3 GHz
Data rate	50 Mbps
Single Channel bandwidth	400 MHz
Modulation	Pulse position modulation
Average power consumption	12.5 mW @1.8v
Architecture	All digital except pulse generator
Technology	TSMC 1.8v, 0.18 μm CMOS mixed signal
Implementation	Single chip
Circuit Size	0.729 mm^2 (excluding antenna)
Application	Short distance (on chip wireless interconnection for future ULSI)

3. Summary and Future Plan

A single chip UWB transmitter circuit based on time hopping spread spectrum technique for wireless interconnect system has been developed based on CMOS technology to generate the monocycle pulse with a target monocycle pulse center frequency of 5 GHz. The chip is now under evaluation process.

4. References:

[1] A B M H Rashid, S Watanabe and T. Kikkawa, IEEE Electron device letter, Vol.23, No.12, Dec 2002, pp. 731-733.
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[3] Jeongwoo Han and Cam Nguyen, IEEE microwave, wireless and components Letters, vol. 12, No. 6, June 2002, pp. 206-208.

5. Achievement

Proceeding Papers

1. P. K. Saha . Nobuo Sasaki, and Takamaro Kikkawa, " A Single Chip UWB Transmitter based on 0.18 μm CMOS Technology for Wireless interconnection," Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing, Jan. 30, 2004, pp. 28-29.
2. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa, " A CMOS UWB Transmitter for Intra/Inter-chip Wireless Communication" paper accepted, IEEE 2004 International Symposium on Spread Spectrum Techniques and Application (ISSSTA 2004), Australia, Aug. 30-Sep 2, 2004.
3. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa**, "** A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter-chip Wireless Interconnection", paper submitted, SSDM 2004, Tokyo, Japan.

Oral presentation

1. Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa ,"UWB Transmitter Circuit design for on chip wireless interconnection: Theoretical aspects and simulation," Presented at Mini-symposium and RF technical workshop , 7 October 2003, Osaka University, Japan.

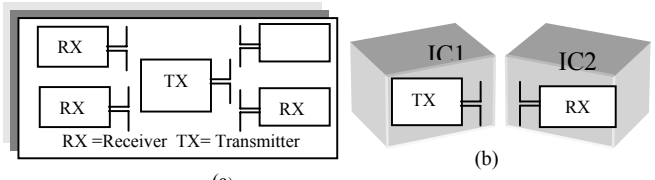


Fig. 1 Wireless interconnect (a) Intrachip ; (b) Interchip

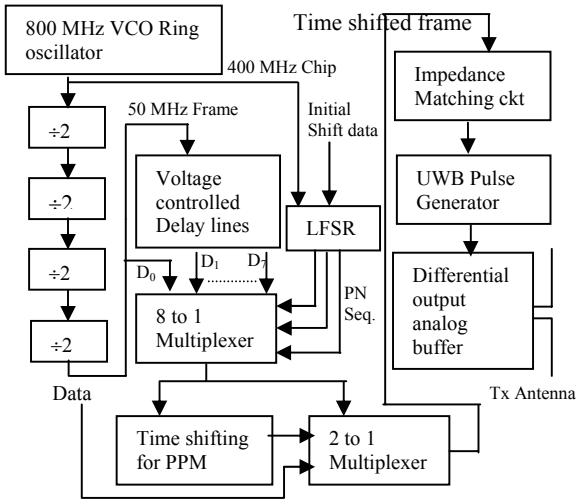
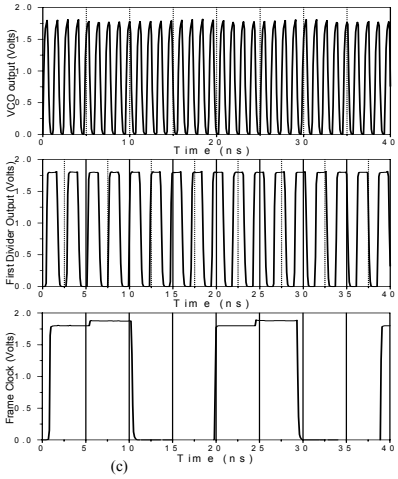


Fig.2 Transmitter circuit Schematic.



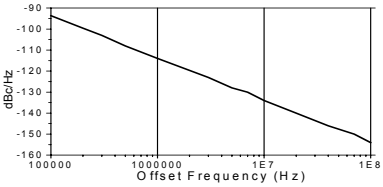


Fig.4 VCO Phase noise.

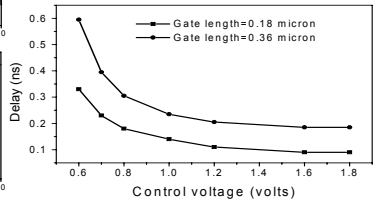


Fig. 5 Voltage controlled delay response.

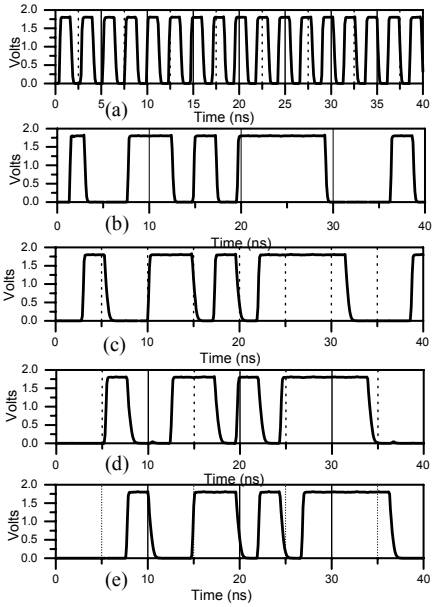


Fig.6 (a) 400 MHz Chip; (b) first tap; (c) second tap ; (d) third tap and (e) last tap outputs of LFSR.

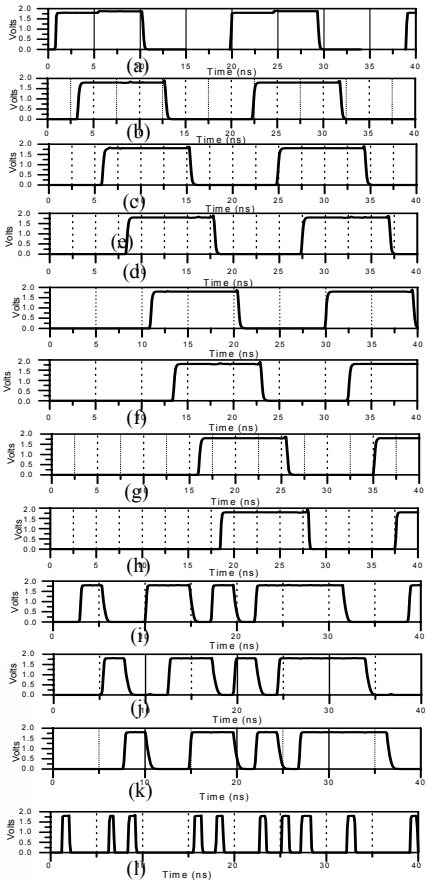


Fig. 7 (a) 50 MHz frame ; (b)-(h) shifted frame (2.5ns-17.5ns); (i)-(k) hopping bits ; (l) 8 to1 multiplexer output according to hopping bits

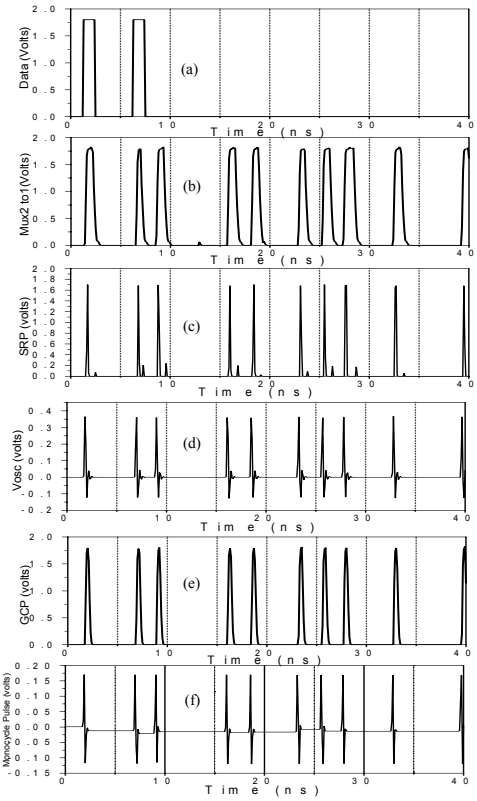


Fig. 9 (a) RZ Data (b) THS ; (c) SRP ; (d) damped sinusoidal signal (Vosc); (e) GCP and (f) Monocycle pulse.

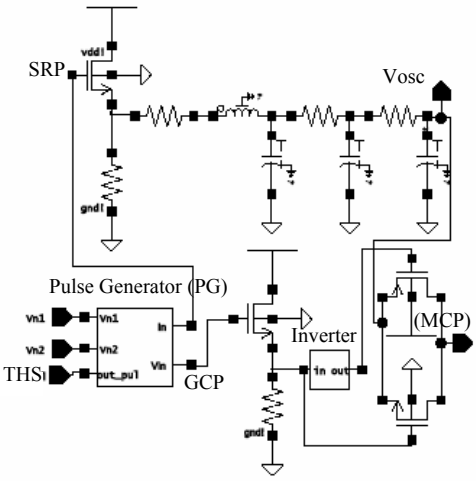


Fig. 8 CMOS monocycle pulse generator circuit

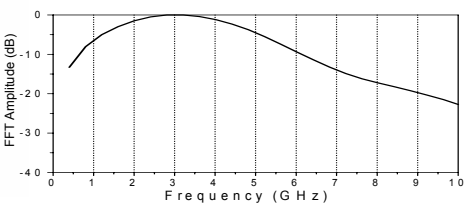


Fig. 10 FFT of Monocycle pulse.

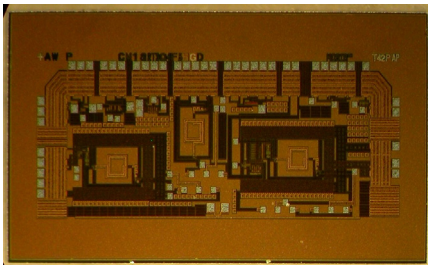


Fig. 11 Die photograph of Transmitter.

Intra/Inter-Chip Wireless Interconnect System for ULSI (3)
－A CMOS Ultra Wideband Receiver－

Nobuo Sasaki (COE Researcher) and Pran Kanai Saha (COE Researcher),
Takamaro Kikkawa (Professor, Research Center for Nanodevices and Systems,
Graduate School of Advanced Sciences of Matter)

1. Research Targets

A wireless interconnect technology has been developed and it can provide a better answer for RC delay problem in future ULSI [1,2]. Recently, UWB (Ultra Wide Band) technology has been developed for indoor communications [3,4]. However, single chip CMOS UWB integrated circuits have not been developed yet. In this study, a prototype of single-chip UWB receiver integrated with dipole antennas is developed based on 0.18μm CMOS technology. The target operation frequency is 4-5 GHz.

2. Research Results

Figures 1 and 2 show a photograph and block diagram of a prototype of single-chip UWB receiver based on 0.18-μm CMOS technology, respectively. It is composed of 200Ω (1GHz) - 107Ω (10GHz) impedance matching circuit (IMC), 15.6dB two stage differential low noise amplifiers (LNA), pulse correlation circuit (mixer + integrator) and analog/digital converter (sample/hold + comparator). An input signal $V_{in}(t)$ is a periodic Gaussian monocycle pulse train (center frequency f_c= 5GHz, pulse width=0.2ns and 3dB bandwidth = 5.8GHz). Fourier expansion and Fourier coefficient F_n of such signals are given as follows,

$$\mathrm{V_{in}}(t) = -\frac{\sqrt{2\pi}}{T}\sum_{n=1}^{+\infty} F_n \sin(2\pi f_n t) \tag{1}$$

$$F_n = \frac{A}{2}\left(\frac{f_n}{f_c}\right) e^{-\frac{1}{2}\left(\frac{f_n}{f_c}\right)^2}\left[erf\left\{\frac{i}{\sqrt{2}}\left(\frac{f_n}{f_c}\right)+\sqrt{2}\pi f_c T\right\} - erf\left\{\frac{i}{\sqrt{2}}\left(\frac{f_n}{f_c}\right)-\sqrt{2}\pi f_c T\right\}\right] \tag{2}$$

where $2T$: cycle time, $f_n = n/2T$: frequency and f_c : center frequency, respectively. The modulation method is pulse position modulation (PPM), i.e., in the case of data d=1, the arrival of the pulse is delayed for a short period of time δ. Pulse correlation circuit performs a demodulation as follows

$$\int_{-T0/2}^{T0/2} V_{in}(t)\cdot V_{template}(t)dt \begin{cases} >0 \ for & d=1 \\ <0 \ for & d=0 \end{cases} \tag{3}$$

where T_0 is a integration time (> pulse width), and $V_{template}$ is called as a template signal, which is defined as a differentiation of input signal. HSPICE simulation data are shown in Figs.3 and 4.

The schematic diagram of differential LNA is shown in Fig. 5. The output signal of the circuit is calculated as follows

$$V_{out}(t) \approx -\frac{A\sqrt{2\pi}}{\mathrm{T}}\sum_{n=1}^{\infty} e^{-\frac{1}{2}\left(\frac{f_n}{f_c}\right)^2}\left(\frac{f_n}{f_c}\right)|A_v(f_n)|\sin(2\pi f_n t+\theta(f_n)) \tag{4}$$

where $|A_v(f_n)|$: transfer function and $\theta(f_n)$: phase shift. Frequency responses of the amplification stage show a monotonous roll-off of the gain in the frequency range of 1-10GHz as shown in Fig. 6. It gives rise to the distortion and phase shift of Gaussian monocycle pulse so that it leads to an increase of bit error rate in pulse position modulation (PPM). Thus, the group-delay characteristics of Gaussian monocycle pulse are studied in detail. Small signal analysis shows almost the same frequency response as HSPICE as shown in Fig. 6. Figure 7 shows the output signal of LNA. It is found that pulse width becomes longer after the LNA because its frequency response rolls off monotonically and higher frequency components of monocycle pulse are cut off. Figure 8 shows that the center frequency of the LNA frequency spectrum shifts from 5GHz to 4GHz, and corresponding pulse width is 0.25ns. It indicates that the template signal should be modified by the LNA roll-off characteristics to reduce bit error rate.

3. Summary and Future Plan

A prototype of single-chip UWB receiver integrated with dipole antennas was designed based on 0.18μm CMOS technology. Small signal analyses and HSPICE simulation of CMOS UWB receiver circuit using Gaussian monocycle pulse were conducted. High frequency roll-off due to parasitics of LNA resulted in the increase of monocycle pulse width. Accordingly, the template signal should be shifted to reduce bit error rate. The results of theoretical analysis were submitted to SSDM 2004.

4. References

[1] B. A. Floyd and Kenneth K. O., IEEE J. of Solid State Circuits, 37 (2002) pp543-592.
[2] A. B. M. H. Rashid, S. Watanabe and T. Kikkawa, Jpn. J. Appl. Phys. Part 1, 4B, 42(2003) 2204.
[3] M. Z. Win and R. Scholtz, IEEE Trans. on Comm. 48 (2000) pp679-691.
[4] S. Yoshizumi. T. Terada, J. Furukawa, Y. Sanada and T. Kuroda, IEEE Ultra Wideband Systems and Technologies (UWBST' 03), pp.438-442.

5. Achievement

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2. Pran Kanai Saha, N. Sasaki and T. Kikkawa, “A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter-chip Wireless Interconnection”, submitted to SSDM 2004, Tokyo, Japan.
3. N. Sasaki, P.K. Saha and T. Kikkawa, “A single chip UWB receiver based on 0.18 um CMOS technology for wireless interconnection”, Proceedings of 2nd Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing, pp98-103.

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1. N. Sasaki, P.K. Saha and T. Kikkawa, " UWB receiver circuit design ", The 1st workshop of analog RF circuits, Osaka University., 2003.10.7.
2. N. Sasaki, P.K. Saha and T. Kikkawa, "A single chip UWB receiver circuit design and simulation", The 51st Spring meeting of JSAP, Tokyo University of Technology, Abstract 28aZH10, p. 958, 2004.

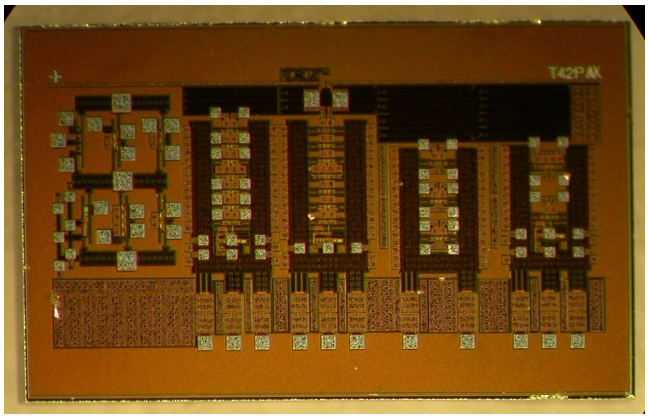

Fig.1. The Photograph of UWB receiver (TSMC CMOS 0.18-μm mixed signal, V_{dd}=1.8V).

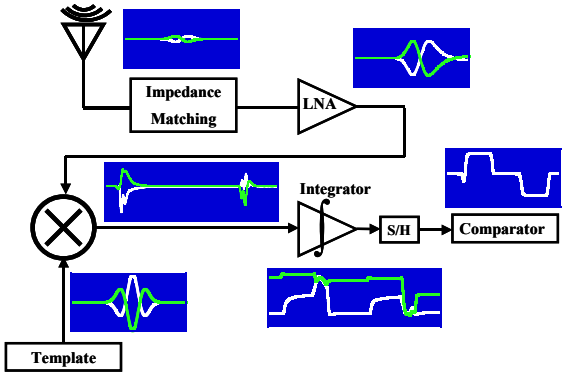

Fig.2. Functional block diagram of UWB receiver.

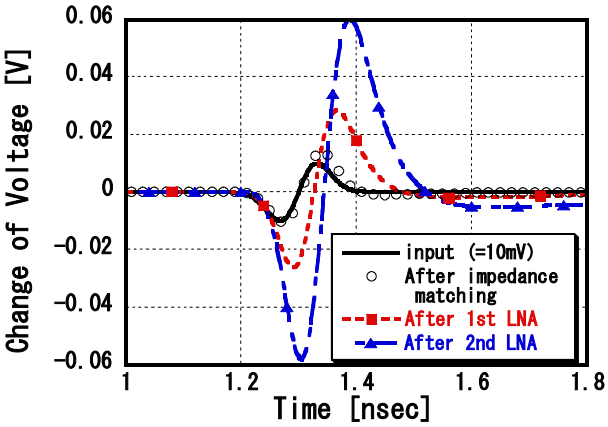

Fig.3 Output of UWB receiver (HSPICE simulation).

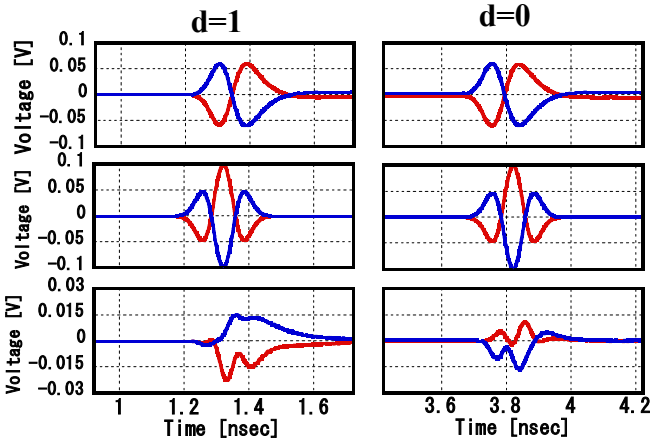

Fig.4. Input , template and output signals of Mixer in the case of d=1 (left) and d=0 (right).

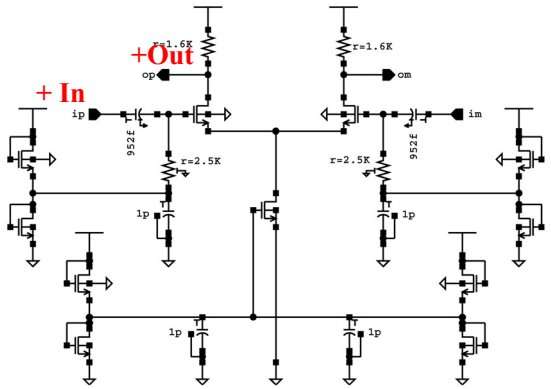

Fig.5. Schematic diagram of differential low noise amplifier.

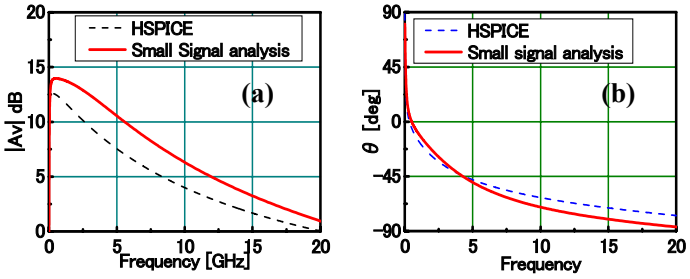

Fig.6. Frequency response of LNA. (a) Voltage gain (b) Phase shift.

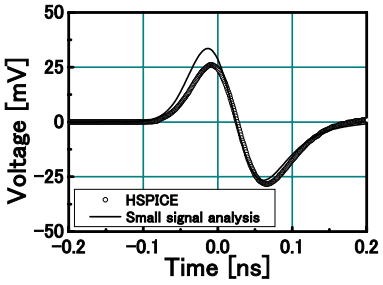

Fig.7. Output signal of LNA.

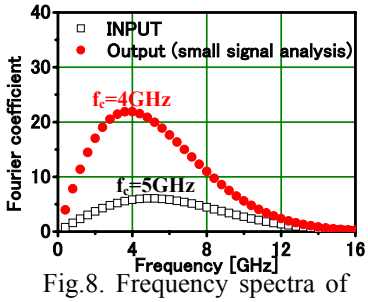

Fig.8. Frequency spectra of Input and output signals of LNA.

Intra/Inter Chip Wireless Interconnect System for ULSI (4)
－Low-k/Cu Interconnect－

Takamaro Kikkawa (Professor, Research Center for Nanodevices and Systems,
Graduate School of Advanced Sciences of Matter),
Susumu Sakamoto (Graduate School of Advanced Sciences of Matter, M2)

1. Research Target

According to the scaling rule [1] for miniaturization of the ultra-large-scale-integrated circuits (ULSI), the interconnect feature sizes of lines and spaces should be reduced. However, the increase of interconnect RC-delay, resistance-capacitance product occurs, therefore, the interconnect technology with low-resistance metal wire and low-dielectric constant (low-k) interlayer film are needed for ULSI. The purpose of this research is to develop low-k interlayer dielectric films with photosensitivity so that low-cost multilevel interconnect systems can be realized.

2. Research Results

Methylsilsesquioxane (MSQ) has been developed as a low dielectric constant material; k=2.7 [2,3]. Methylsilsesquiazane (MSZ) is a precursor component of MSQ as shown in Fig. 1. When the photo-acid generator (PAG) molecule is added to MSZ, it acquires the photosensitivity. The photosensitive MSZ precursor has sensitivity to not only ultra-violet light and but also electron-beam. Then the lithography of photosensitive low-k MSQ was examined by using ultra-violet light, KrF excimer laser, electron beam and SOR X-ray [3-5]. In these lithographies via and trench patterns were formed directly in the MSZ film without using dryetching. The dryetch-less process eliminates the resist coating and ashing, so that it can reduce process steps. Furthermore, the reliability issues such as void formation in the film due to dryetching and ashing [6] can be eliminated. At the same time disuse of hardmask and etch-stop layer enables us to reduce effective dielectric constant of multilevel interconnect interlayer.

MSZ is the precursor component of MSQ as shown in Fig. 1. When the photoacid generator (PAG) molecule is added to MSZ, and MSZ acquires photosensitivity. We call this chemical mixture photosensitive MSZ (PS-MSZ). The PAG molecule releases proton upon ultraviolet ray exposure or electron-beam exposure. The activated proton from the PAG attacks the bonds of its neighboring molecules and chemical reactions are provoked. Then in the exposed region of PS-MSZ film the protons attack Si-NH bonds, and frequently cut this bond. If water, H_2O, is present, Si-NH bond is replaced with Si-OH bond as shown in Fig 2. These microscopic reactions are repeated, and MSZ polymers in the exposed region are cut into small pieces. Along the exposed region of the film, macroscopic patterns are formed.

Reaction path of photosensitive MSZ is shown in Fig. 3. k_1, k_{-1} and k_2 are the rate constants, and which determine the reaction rate of patterning. From these equations, probability function of film patterning is calculated as

$$P(t) = 1 - \exp(-\gamma t), \qquad (1)$$

where

$$\gamma = \left(1 - \frac{k_{-1}}{k_{-1} + k_2[H_2O]}\right) \cdot k_1[H^+]. \qquad (2)$$

The concentrations are governed by the diffusion equation, and then the probability function is dependent on diffusion time and film location. The SEM micrographs of in a conventional process are shown in Fig. 4. Calculated pattern was fitted to these SEM micrographs, and the calculated patterns are given as Fig. 5. Since the energy of the electron beam is 50 keV, protons are distributed around the exposed pattern from the film surface to the bottom, and in subsequent humidification treatment the water diffuses into the MSZ film from the film surface. The H_2O concentration becomes lower level from the film surface to the bottom, and then threshold H_2O concentration determines the development of exposure pattern. An improved process performed uniform H_2O concentration. The calculation of the patterning probability predicts that an improved process can form abrupt pattern shapes. The SEM micrographs of photosensitive MSZ precursor in the improved process are shown in Fig. 6. It is found that the improved process formed abrupt pattern shapes. The minimal developed feature size was 90 nm at 111 μ C/cm^2. This feature size gives the aspect ratio 3.9.

The characteristics of photosensitive porous low-k methylsilsesquioxane (MSQ) were investigated by electron-beam lithography. Pore size distributions were measured by X-ray scattering measurement (XRS) using a Rigaku ATX-E X-ray diffractometer, as shown in Fig. 7. Peak pore radii for photosensitive porous MSQ with 10 wt% porogen and with 20 wt% porogen were 1.37 nm and 2.03 nm, respectively. Average pore radii for photosensitive porous MSQ with 10 wt% porogen and with 20 wt% porogen were 2.30 nm and 3.72 nm, respectively. The dielectric constant of photosensitive MSQ decreased with increasing porogen concentration, as shown in Fig. 8. The dielectric constants for photosensitive MSQ without porogen, with 10 wt% porogen and with 20 wt% porogen, measured by capacitance-voltage (CV) measurement, were 3.25, 3.05 and 2.73, respectively. The effective medium approximation (EMA) method predicts the reduction of dielectric constant with increasing porosity. The dielectric constant of EMA is given by the equation [7],

$$k_p = \frac{(k_s + 2) + 2(1 - x)(k_s - 1)}{(k_s + 2) - (1 - x)(k_s - 1)}, \qquad (3)$$

where k_p and k_s are the dielectric constants of the porous film and its skeleton, respectively, and x is porosity. EMA-calculated dielectric constants are shown in Fig. 8. In the EMA calculation, porosity values were given by the measured values of spectroscopic ellipsometry. It is found that the results of CV measurement were consistent with the EMA-calculated values. The difference between the measured value and EMA-calculated value could be attributed to the absorption of moisture in the porous films [8]. SEM images of photosensitive MSZ with and without porogen, and cured photosensitive porous MSQ are shown in Fig. 9. In micrographs of photosensitive porous MSZ (Fig. 9(b)), it is found that the porogen residue remained on the sidewall of the trench patterns. This is because porogen additives do not dissolve in the TMAH developer. Porogen evaporated at the 400℃ curing process, and then the porogen residue disappeared after 400℃ curing, as shown in Fig. 9(c). Then line-and-space patterns in the photosensitive porous MSQ film were formed by electron-beam lithography without dry etching.

3. **Summary and Future Plan**

Characteristics of photosensitive MSQ low-k film were investigated using electron-beam lithography. The process parameters to define the exposure pattern were investigated. In the post-humidification process the critical dimensions of the exposed patterns were dependent on the hold time from electron-beam exposure to humidification treatment. Diffusion of H_2O molecules from the film surface limited the development of the exposure patterns, resulting in tapered shape patterns. On the contrary, in the improved process the developed pattern showed abrupt shape. This is because H_2O concentration was uniform in photosensitive MSZ film. Consequently, abrupt shape of the pattern with high aspect ratio was achieved. In this process the aspect ratio was 3.9, and the minimal feature size was 90 nm.

A novel photosensitive porous MSQ interlayer dielectric film was developed. Photosensitive porous MSQ (20 wt% porogen) had a porosity of 17%, a pore radius of 2.2 nm, and a dielectric constant of 2.62. The characteristics of the photosensitive porous MSQ film were investigated, and the 50-200 nm photosensitive porous MSQ patterns could be formed successfully by electron-beam lithography without dry etching.

4. References

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[2]. S. Mukaigawa, T. Aoki, Y. Shimizu and T. Kikkawa: Jpn. J. Appl. Phys. 39(2000) 2189.
[3]. T. Kikkawa, T. Nagahara and H. Matsuo: Appl. Phys. Lett. 78 (2001)2557.
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[6]. A. Matsushita, N. Ohashi, K. Inukai, H. J. Shin, S. Sone, K. Sudou, K. Misawa, I. Matsumoto and N. Kobayashi: Proc. IITC (2003) 147.
[7]. N. Hata, C. Negoro, K. Yamada, H. S. Zhou, Y. Oku and T. Kikkawa: Extended Abstracts of the 2002 Int. Conf. Solid State Devices and Materials, (2002) 496.
[8]. S. Sakamoto, S. Kuroki and T. Kikkawa: Extended Abstracts of the 2003 Int. Conf. Solid State Devices and Materials, (2003) 478-479.

5. Achievement

Published papers

1. S. Kuroki, T. Kikkawa, H. Kochiya and S. Shishiguchi, "Low-k Dielectric Film Patterning by X-Ray Lithography", Jpn. J. Appl. Phys. Vol. 42 (2003), pp. 1907-1910.

2. S. Kuroki, S. Sakamoto and T. Kikkawa, "A Novel Photosensitive Porous Low-k Interlayer Dielectric Film", Jpn. J. Appl. Phys. Vol. 42 (2004), pp 1820-1824.

Proceedings

3. S. Kuroki, T. Kikkawa, H. Kochiya and S. Shishiguchi, "Direct Patterning of Low-k Dielectric Films using X-ray Lithography", Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, pp.464-465

4. S. Kuroki, T. Hirota and T. Kikkawa, "A Novel Photosensitive Porous Low-k Interlayer Dielectric Film", Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, pp.468-469.

5. S. Sakamoto, S. Kuroki and T. Kikkawa, “Influence of Humidity on Electrical Characteristics of Porous Silica Films”, Extended Abstracts of the 2003 Int. Conf. Solid State Devices and Materials, (2003) 478-479.

6. S. Kuroki, S. Sakamoto and T. Kikkawa, "Direct Patterning of Photosensitive Porous Low-k Film and Its Electrical Characteristics", Proceedings of The 65th Symposium on Semiconductors and Integrated Circuits Technology, pp.468-469.

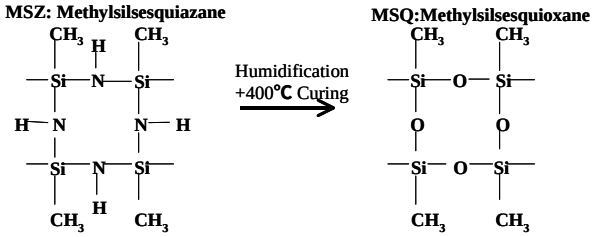


Fig.1. The chemical structure of MSZ-MSQ

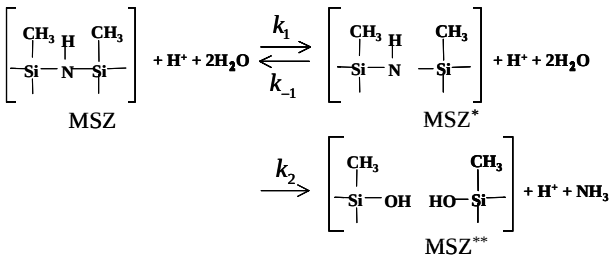


Fig. 3. Reaction path for photosensitive MSZ: MSZ^* shows mol concentration of the activated Si-N-Si bond. MSZ^{**} is mol concentration of broken Si-N-Si bond. , and are the reaction rates for each reaction.

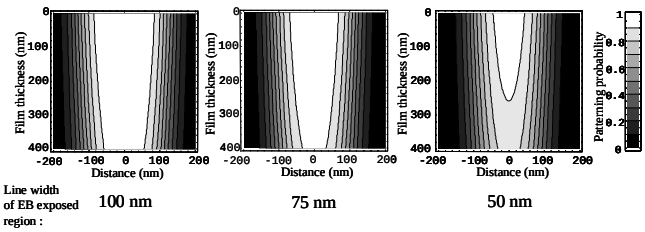


Fig. 5. Reaction probability as a function of EB exposed line width in the post-humidification process: it is found that the exposed pattern form is dependent on the line width. (H^+ diffusion time: 1420 sec, H_2O diffusion time: 180 sec)

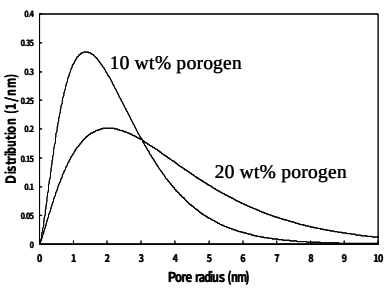


Fig.7. Pore radius distribution of photosensitive porous MSQ: peak pore radii of photosensitive porous MSQ with 10 wt% porogen and 20 wt% porogen were 1.37 nm and 2.03 nm, respectively.

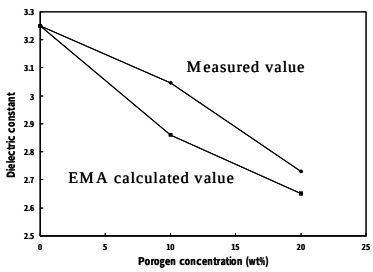


Fig.8. Dielectric constants of photosensitive porous MSQ: the dielectric constant of photosensitive MSQ decreased with increasing porogen concentration.

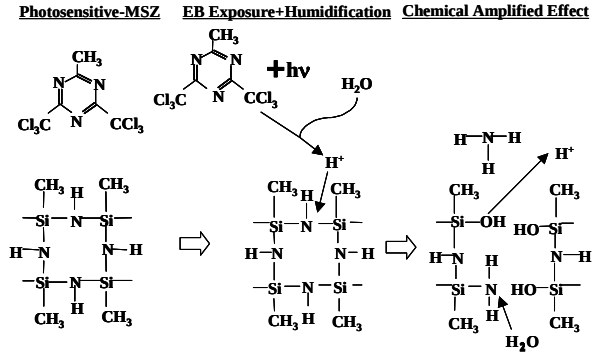
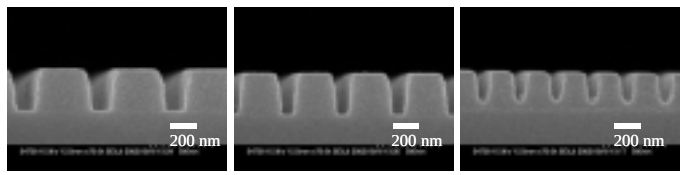
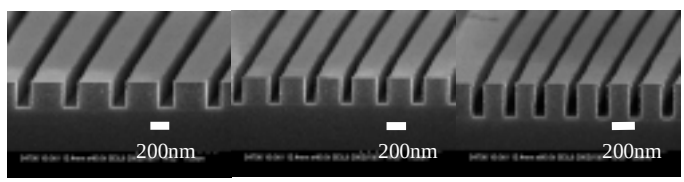


Fig. 2. Schematic diagram of photo-amplified reaction in photosensitive MSZ film.



(a) 100 nm (b) 75 nm (c) 50 nm

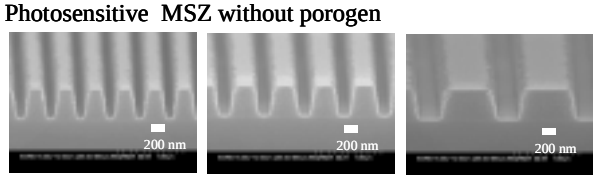
Fig. 4. SEM micrographs of photosensitive MSZ in an conventional process. The lengths given below the images are the design sizes.



(a) 100 nm (b) 75 nm (c) 50 nm

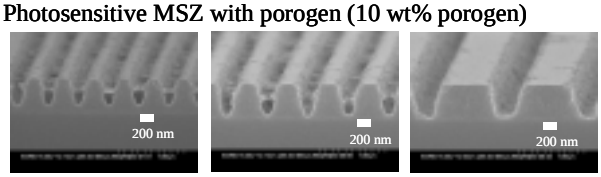
Fig. 6. SEM micrographs of photosensitive MSZ in an improved process (exposure dose: 111 μC/cm2, L/S=1:5) . The lengths given below the images are the design sizes.

(a) Photosensitive MSZ without porogen



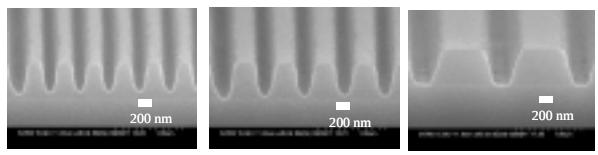
Design Size: 75 nm 100 nm 200 nm

(b) Photosensitive MSZ with porogen (10 wt% porogen)



Design Size: 75 nm 100 nm 200 nm

(c) 400 ℃ Cured photosensitive porous MSQ (10 wt% porogen)



Design Size: 75 nm 100 nm 200 nm

Fig. 9. SEM micrographs of photosensitive porous MSQ: (a) photosensitive MSZ without porogen, (b) photosensitive MSZ with 10 wt % porogen and (c) cured photosensitive porous MSQ (10 wt% porogen). The electron beam exposure dose was 9.0 μC/cm^2.

Development of Optically Interconnected LSI
−Integration of Ring Resonator Switches using Electro-Optic Materials−

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Yuichiro Tanushi (COE Researcher),
Masaru Wake (Graduate School of Advanced Sciences of Matter, M2),
Keita Wakushima (Faculty of Engineering, B4)

1. Research Target

With the progress of the miniaturization and switching speed of transistors, the performance of LSI is now governed by the signal transfer spe ed of the interconnection. Therefore, recently the RF wireless interconnection and optical interconnection are attracting much attention as a next generation interconnects in LSI instead of metal interconnection. In this twenty-first century COE program, the wireless interconnection and optical interconnection are studied. The author is in charge of the development of optical interconnection in LSI.

2. Research Results

The author has been studying optically interconnected LSI. We have so far developed three dimensional optically coupled common memory,[1] pattern recognition chip with optical interconnection,[2] and high-speed lift-off technique of light-emitting devices from GaAs substrate and the method to bond the lifted-off light-emitting devices onto Si LSI.[3] The achievements after this COE program started, are 1) development of stack-type branched waveguides with good light dividing controllability,[4] and 2) proposal of ring resonator switches using electro-optic materials, for which the refractive index is changed by the electric field.[5] In this paper item 2) is described.

2-1 Ring resonator switch using electro-optic materials

We have so far developed the integration technologies by bonding many light-emitting devices on Si chips.[3] However, this method is not so reliable and not suitable to the mass production. Instead of this, we propose a monolithic integration of optical switches, which modulate the light intensity. The schematic of the proposed optically interconnected LSI is shown in Fig. 1. For this purpose, we are studying optical switch using the optical micro-ring resonator,[6] which is recently attracting much attention. In our proposal, the electro-optic materials such as $LiNbO_3$ and $(Ba,Sr)TiO_3$, are used for the core layer of the ring resonator (Fig. 2). Then, the resonance wavelength can be changed by the applied bias voltage. Therefore, the optical switch using the ring resonator with the size of a few tens of microns can be realized by the structure shown in Fig. 2. The another type of tunable ring resonator by temperature control is reported by Kokubun *et al.*[7] However, the high-speed response is not expected by the temperature control method. On the other hand, the response frequency of the electro-optic material is expected to be tera-hertz order because the electro-optic effect is based on the ionic polarization. The speed of the actual devices is determined by the stray capacitance and the series resistance of the electrode.

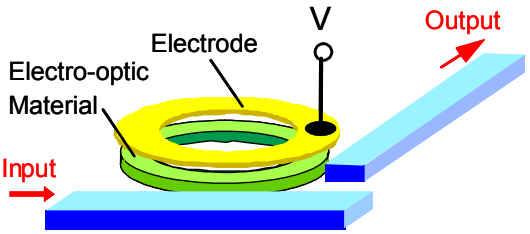

Fig. 2 Ring resonator switch using electro-optic material.

Figure 3shows the cross section and the plan view of the ring resonator switch. The resonance wavelength λ is given by the following formula.

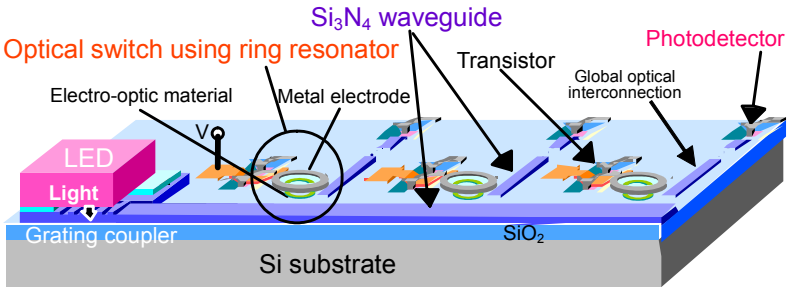

Fig. 1 Schematic of optically interconnected LSI proposed in this research rogram.

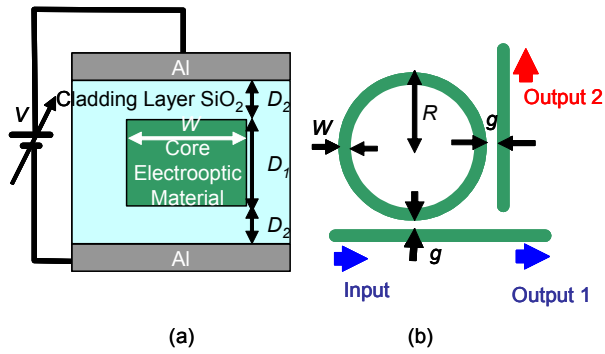

Fig. 3 (a) Cross section and (b) plan view of the ring resonator switch using electro-optic material.

$$\lambda = n_{eff}\frac{2\pi R}{m} \qquad (1)$$

Here, n_{eff} is the effective refractive index, R is the radius of the ring, and m is an integer. Figure 4 shows the simulated light propagation loss with the same cross section as in Fig. 3(a). The core is assumed to be $LiNbO_3$ with refractive index of 2.2 and the thickness is 0.5 μm. The two dimensional finite difference time-domain (FDTD) simulator (Apollo Photonic Solutions Suite) is used. The width of the waveguide is 2 μm, and the wavelength is 850 nm. From this figure, the thicker SiO_2 cladding layer than 0.25 μm is required to obtain a small propagation loss than 1 dB/cm. Such thick cladding layer leads to the higher operation voltage. In order to shrink the cladding layer, we have simulated the core thickness dependence of the propagation loss and the result is shown in Fig. 5. Here, the cladding layer is fixed at 0.1 μm. It is found that the core thicker than 3 μm results in small propagation loss less than 1 dB/cm. The thicker core film does not increase the operation voltage because the dielectric constant of the core film is usually large. Figure 6 shows the simulated resonance characteristics of the ring resonator with the ring radius of 12 μm, width of 2 μm, core ($LiNbO_3$) thickness of 0.5 μm, and cladding layer thickness of 0.1 μm. The gap width is 0.1μm. The electric field, E=3.1×10^{4}V/cm, induces the change in refractive index of 5×10^{-4}, which gives

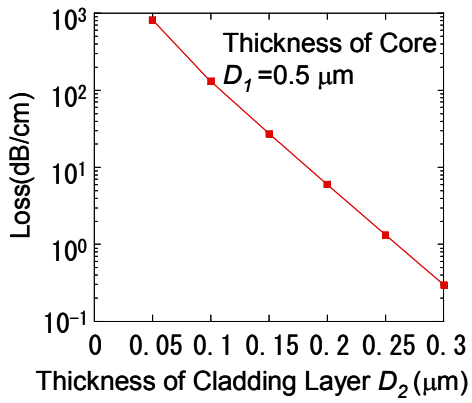

Fig. 4 Propagation loss versus thickness of cladding layer of the waveguide.

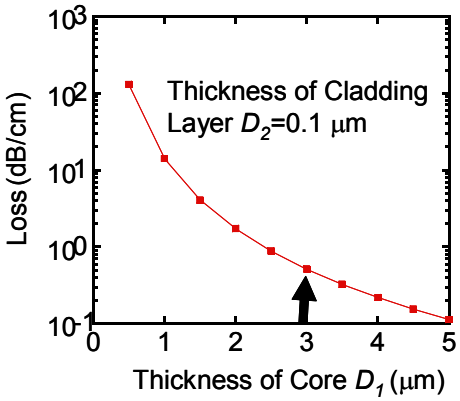

Fig. 5 Propagation loss versus thickness of core layer.

rise to the switching gain of 5 dB at wavelength of 852.35 nm. The switching operation voltage is given by the following formulae and is calculated to be 13.5 V.

$$\left.\begin{aligned}\Delta n &= -\frac{1}{2}n^3 rE \\ V &= D_{core}E + 2D_{SiO2}\frac{\varepsilon_{core}}{\varepsilon_{SiO2}}E\end{aligned}\right\} \qquad (2)$$

Here, n and Δn are, respectively, the refractive index of the core and its change due to the electric field, r is the electro-optic coefficient, D_{core} and D_{SiO2} are, respectively, thicknesses of the core and SiO_2 cladding layers, ε_{core} and ε_{SiO2} are, respectively, the dielectric constants of the core and cladding layers. The operation voltages and frequencies calculated for the various electro-optic materials are shown in Table 1 together with the characteristic constants. The operation frequency is calculated as the reciprocal time constant determined from the resistance and capacitance of the electrode (Al: 0.8 μm in thickness). The $(Ba,Sr)TiO_3$ film is studied for the DRAM application, however, the operation voltage is relatively high (92 V) due to the large dielectric constant. The improvement of the

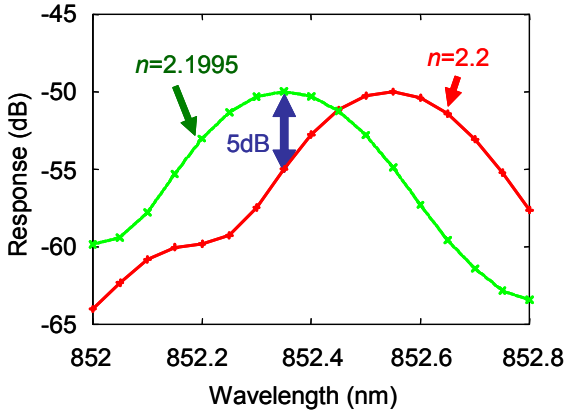

Fig. 6 Simulated response of output 2 in Fig. 3 for different refractive index of core layer.

Table 1 Operation voltage and frequency for ring resonator switches using various electro-optic materials.

	$LiNbO_3$	$(Ba,Sr)TiO_3$	$K(Ta,Nb)O_3$
Electro-optic Coefficient (pm/V)	30.8	23	600
Refractive Index n	2.2	2.1	2.35
Electric Field E (10^4 V/cm)	3.05	5	0.1284
Relative Dielectric Constant ε	28	300	28～300 (assumed)
Operation Voltage V (V)	13.5	91.9	0.57～2.36
Operation Frequency f (THz)	58	47	47～58

resonance sharpness (Q value) is required by, for example, devising the structure. Here, we have, for the first time, measured the electro-optic coefficient of the $(Ba,Sr)TiO_3$ film. The $K(Ta,Nb)O_3$,[8] which was recently developed by NTT results in the small operation voltages of a few V or less.

2-2 Fabrication and evaluation of ring resonator

First, we have developed the fabrication technology and evaluation method for the optical ring resonators. Plasma CVD Si nitride film was used for the core material. Figure 7 shows the developed measurement system. Figure 8 shows the measured resonance characteristics of the ring resonator of ring radius of 10 μm, waveguide width of 3 μm, and coupling gap width of 0.2 μm. The ring resonator was fabricated by electron beam lithography followed by the reactive ion etching of the Si nitride film. A good correlation between the dips in output1 and peaks in output2 is observed, which indicates that the resonance takes place and the resonated light power is transferred to the output2. Also a good agreement between the experimental and simulated results is observed.

2-3 Optical waveguide using electro-optic material

We have fabricated the optical waveguide using $(Ba,Sr)TiO_3$ (BST) film as a core material by spin coat method. The BST film was formed by spin coating the source liquid at an appropriate rotation speed and time, followed by the annealing at 550°C for 5 min. This sequence was repeated until the film thickness reaches the required value. The substrate is thermally oxidized SiO_2/Si substrate patterned by electron beam lithography and reactive ion etching as shown in Fig. 9(a), where the trenches are formed. After spin coating, the planarization takes place and the film thickness in the trench becomes thicker compared to the outside of the trench. Then, the light (He-Ne laser, 633 nm) is confined in the trench, which is shown in Fig. 9(b).

Figure 10 shows the measured propagation loss as a function of the width of the trench. It is noted that for the thicker core film (d=0.3 μm) the propagation loss is larger than that of the thinner one (d=0.2 μm) in the narrow trench region (<28 μm). This is interpreted as follows. As the core film becomes thicker, the film thickness outside the trench region also becomes

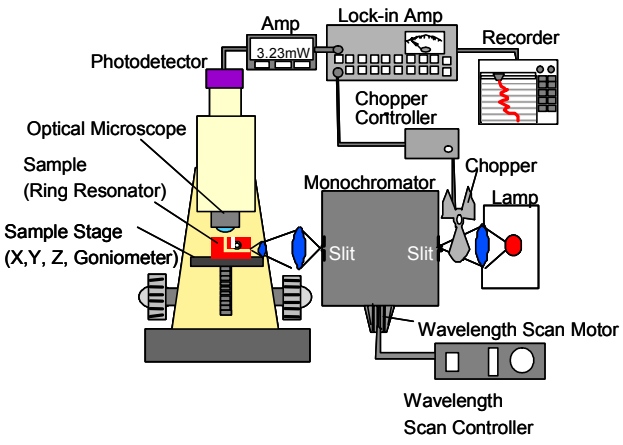

Fig. 8 Resonance characteristics of fabricated ring resonator with Si nitride core.

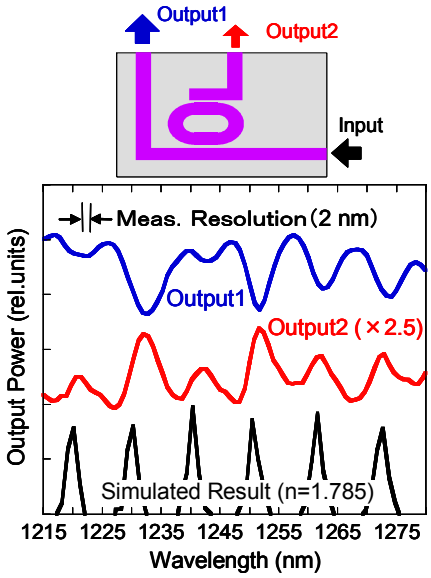

Fig. 7 Measurement system for optical ring resonators.

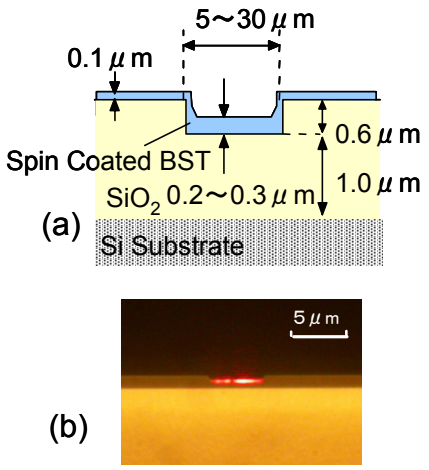

Fig. 9 (a) Cross section of fabricated trench type optical waveguide and (b) optical micrograph of the output light.

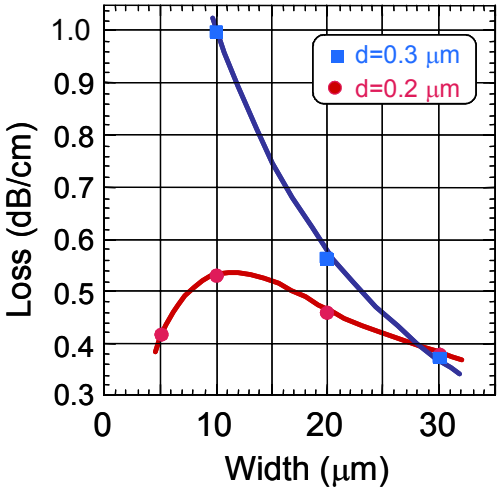

Fig. 10 Light propagation loss for the fabricated waveguide with electro-optic material core.

thicker. Therefore, the light confinement in the trench is weakened.

3. Summary

The ring resonator switch using electro-optic material is proposed and its properties are simulated. As a result, operation voltage is estimated for the several electro-optic materials. The design, fabrication and measurement technologies for the ring resonators with Si nitride core are developed. We have fabricated the optical waveguide using the electro-optic material of $(Ba,Sr)TiO_3$, and the light propagation loss was measured.

4. Future Plan

The ring resonator switch using electro-optic material will be fabricated and measured. The subject to be solved is to improve the crystal quality of the film by adjusting the annealing temperature, to increase the quality factor (Q) of the ring resonator by modifying the resonator structure, and to decrease the operation voltage.

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Design and Fabrication of Race-Track Optical Ring Resonator

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Graduate School of Advanced Sciences of Matter)

1. Research Target

Signal delay in metal interconnection becomes serious problem to limit performances of ultra large scale integrated circuits (ULSIs) . Optical interconnection is promising method to overcome this problem.

Optical microring resonator, of which size is tens micrometers, is being watched with interest because it was shown that microring resonator can be used for optical filter for visible light and infrared region [1]. Optical filter is indispensable for wavelength division multiplexing which realizes broadband telecommunication by propagating many lights with different wavelengths in one optical fiber or waveguide. Ring resonator is the best device for integrated optical filter in optical interconnection on ULSIs because it can be fabricated on Si process.

Chu *et al.* developed stack ring resonator, in which the ring and the bus waveguides are stacked with the spacer, and the coupling efficiency is precisely controlled by the thickness of the spacer [2]. However, the fabrication process is complicated compared with the planer resonators, in which ring and the buses are fabricated in the same plane as shown in Fig. 1. We have fabricated a planer race-track resonator [3]. The race-track resonator enables the precise control of the coupling efficiency by controlling the coupling length, while circle type ring resonator is difficult to control the coupling efficiency.

2. Research Results

The structure of race-track resonator is shown in Fig. 2. Device parameters are the ring radius R, the coupling length L, and the gap between ring and bus g. Light induced from input port partly moved on ring through the gap. Lights with particular wavelengths have the same phase after propagating around the ring, then resonate on the ring and proceed to output 2 port through the gap. Therefore resonance wavelength is given by

$$\lambda_m = n_{eff}\frac{2\pi R + 2L}{m} \quad (1),$$

where n_{eff} is the effective refractive index, and m integer. The coupling efficiency is determined by the gap g and the coupling length L. The long coupling length L needs for resonance of light on the ring. An advantage of race-track resonator is to design large coupling efficiency with the long coupling length even the gap is relatively wide such as 0.2 μm. However, free spectral range (FSR) is inversely proportional to the circumference of the race-track, therefore the short coupling length is good for wide FSR.

We have fabricated two kinds of race-track resonators with long coupling length (Fig. 3(a)) and short coupling length (Fig. 3(b)). The circumference of the race-tracks for (a) and (b) maintained constant, so both resonators have the same resonance wavelength. The ring radius and the gaps are also the same for both ones. First, we simulated the propagation loss of the waveguide with the structure shown in the inset of Fig. 4 for determination of the widths of the ring and bus. Finite difference method (FDM) is used in the simulator (Apollo Photonics Solutions Suite). As a result we chose a width of 3 μm because the loss is sufficiently low at the wavelength region around 1.3 μm which is used for optical telecommunication. Next, we estimated the dependence of the bending loss on the curvature radius by FDM simulation (Fig. 5). The radius R=10 μm was determined for compactness of resonators and wide FSR even the loss is relatively high.

The fabrication procedure is shown in Fig. 6. After the pattern was formed with electron beam lithography and the reactive ion etching in CF_4+N_2 plasma was carried out. Because the etching rate in narrow resist gaps is small, silicon nitride was not etched until the bottom and the gaps were not formed perfectly.

The measured resonating property of the sample shown in Fig. 3(a) is shown in Fig. 7 together with the simulated one by two dimensional finite difference time domain (2D FDTD). A good agreement between the dip positions in output 1, peak position in output 2, and simulated resonance positions is obtained. Figure 8 compares the intensities of output 2 for the fabricated two kinds of samples shown in Figs. 3(a) and 3(b). The output intensity for the sample with longer coupling length is larger because of the larger coupling efficiency. The peak powers of output 2 for these samples are plotted Fig. 9 with 2D FDTD simulation results. For the experimental data the sample with L=12.6 μm is fit to the simulation because the actual light power is unknown. The simulation assumed the gaps were formed perfectly. Therefore the difference in the experimental data is smaller than that of the simulated data.

3. Summary and Outlook

The design and fabrication of race-track ring resonator has been carried out. Its characteristics have been measured and confirmed good agreement with the simulation. The next plan is to optimize the parameter of the race-track resonator and apply to optical switch controlled by electric field by using electro-optic materials as the core of the ring.

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4. Published Papers and Patents

1. Y. Tanushi, M. Wake and S. Yokoyama, "Race-Track Optical Ring Resonators with Groove Coupling," submitted to Int. Conf. on Solid State Devices and Materials (SSDM2004).
2. Y. Tanushi, K. Wakushima and S. Yokoyama, "Very Small Optical Switch using Tunable Optical Ring Resonator Controlled by Electric Field," Extended Abst. of Spring Meeting of Japan Society of Applied Physics (2004) 29a-ZC-9.

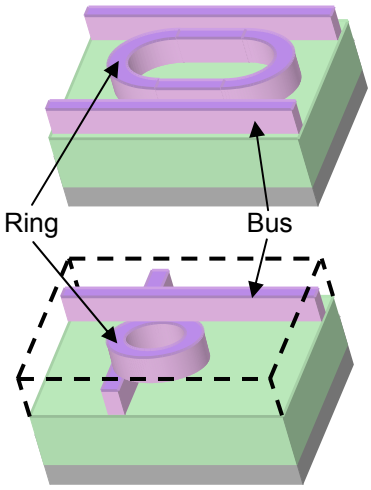

Fig. 1 Planar and Stack ring resonators. Planar resonator has simple structure and can be easily fabricated.

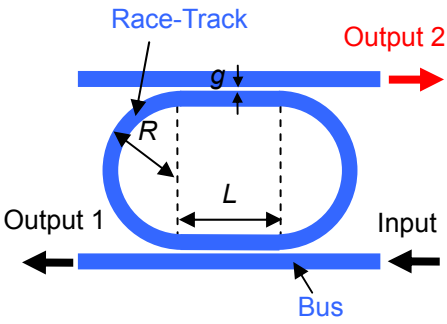

Fig. 2 Structure of race-track resonator. Device parameters are the ring radius R, the gap g, and the coupling length L. The resonating wavelength depends on R and L, and the coupling efficiency depends on g and L.

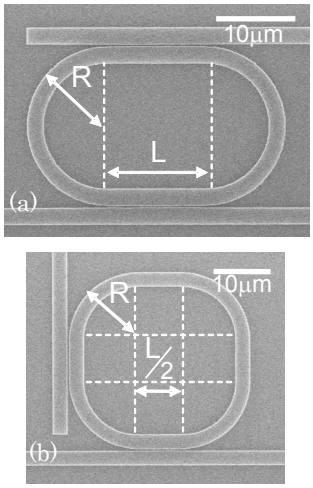

Fig. 3 SEM photographs of the fabricated two kinds of race-track resonators. The coupling length L is (a) 12.6 μm and (b) 6.3 μm respectively. The ring radius R is 10 μm and the gaps are 0.2 μm in both samples.

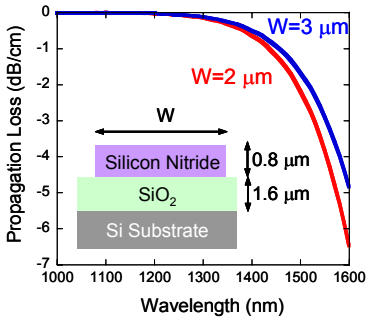

Fig. 4 Simulated propagation loss by FDM. The cross section of the waveguide is also shown.

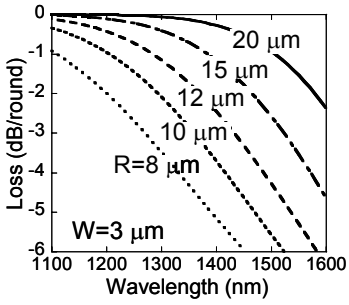

Fig. 5 Simulated bending loss by FDM. The structure of the waveguide is the same as the one in Fig. 4

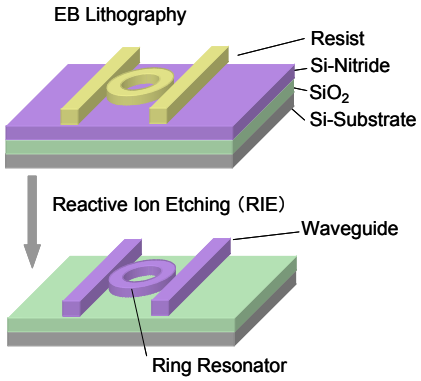

Fig. 6 Fabrication process of the race-track resonator. Silicon nitride film is deposited by plasma enhanced chemical vapor deposition (PECVD) and SiO_2 cladding layer is thermally oxidized.

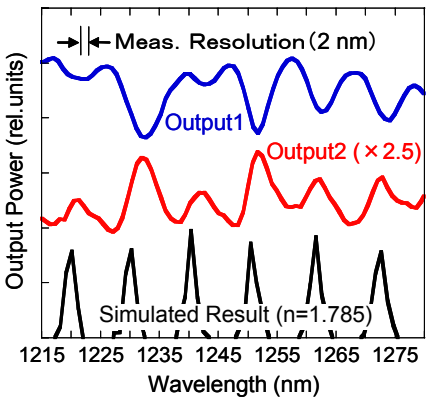

Fig. 7 Measured resonating property of the sample shown in Fig. 3(a). Simulated result is also shown. Simulation method is 2D FDTD.

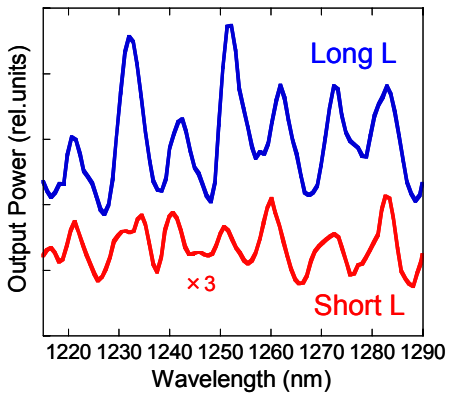

Fig. 8 Comparison between the intensities of output 2 for the fabricated two kinds of samples shown in Figs. 3(a) and 3(b).

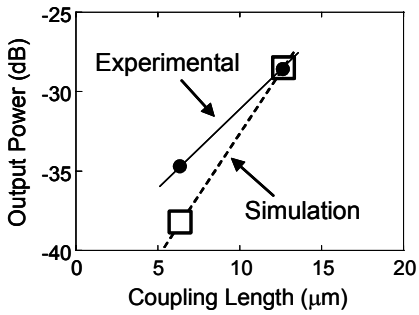

Fig. 9 Power of output 2 for samples (a) and (b) in Fig. 3. In the simulation it is assumed that the groove reaches to the bottom cladding layer.

Etching Properties and Optical Emission Spectroscopy of NH_3 Added C_5F_8 Pulse-Modulated ICP Plasma

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Shin Yokoyama (Professor, Research Center for Nanodevices and Systems,
Graduate School of Advanced Sciences of Matter)

Research Results

1. Introduction

Perfluorocarbons (PFCs) such as CF_4 and cyclic (c-) C_4F_8, which have been used in the dry etching of SiO_2, have big global warming potentials and very long lifetimes as shown in Table 1 [1]. Recently the PFC alternative gases with small global warming potential and short lifetime are strongly required in order to protect the global environment

In this paper, excellent contact hole etching of sub-0.1 μm size in SiO_2 is achieved by adding NH_3 to c-C_5F_8 with small greenhouse effect, and Ar mixing gas in the pulse-modulated inductively coupled plasma (ICP). The influence of the addition gas to the plasma was analyzed with the optical emission spectroscopy (OES). And correlation between flow late of addition gas and OES is studied.

2. Experiments

2.1 Etching system

The ICP etching system we used is schematically shown in Fig. 1. A source RF power of 13.56 MHz modulated using a function generator is introduced into the Cu ring electrode in order to control the plasma density and electron temperature independently. 400 kHz RF is used to generate substrate bias. The wafer is cooled to -11°C to suppress the etching of the resist mask. Pressure is 15 mTorr. Plasma source gas is a mixture of c-C_5F_8 (11 sccm) and Ar (60 sccm) added with NH_3 (1~5 sccm). For the comparison, the effect of other adding gas such as H_2 or O_2 was investigated. The optical emission spectra from the plasma were measured to investigate the reactive species in the plasma.

2.2 Sample preparation

The (100) p-Si wafers with 900 nm thick phosphosilicate-glass (PSG) layer were used for the investigation of the etching profile. The photoresist (posi-type) was patterned using electron beam lithography to investigate the several size of contact hole pattern. After etching, photoresist and deposited polymer were removed by O_2-plasma and sulfuric acid/hydrogen peroxide/water mixture cleaning.

3. Results and Discussions

3.1 Effect of addition gases

Adding oxygen to C_5F_8/Ar plasma greatly influences the etching profiles and selectivity (Fig. 2(a)). The oxygen addition decreases the amount of excess deposition of C_xF_y polymer, leading to the suppression of etch stop, but it also decreases the selectivity [4].

Adding hydrogen to C_5F_8/Ar plasma greatly improves the selectivity (Fig. 2(b)). The hydrogen addition decreases the amount of fluorine radicals, which induces excess etching of Si, leading to the suppression of Si etching. However, the amount of C_xF_y molecules is maintained, and etch stop is still caused [5].

Adding NH_3 to C_5F_8/Ar plasma can realize contact hole of sub-0.1μm size with high aspect ratio and high selectivity (Figs. 2(c), 6). NH_3 in plasma generates hydrogen radicals which decrease the amount of fluorine radicals. And reaction of generated HCN and FCN may reduce the C_xF_y polymer [6].

3.2 Optical emission spectroscopy

In order to monitor the radicals in the plasma and understand the etching mechanism, we exploited the optical emission spectroscopy (OES). Etching concerned species such as CF_2 (321.4nm), F (703.7nm), CN (386nm), NH (338.3nm), and H (Hα at 656nm) are monitored, and the relation between flow rate of addition gas and the intensity of luminescence was discussed.

In the case of NH_3 addition, the result of OES is shown in Fig. 5. The flow rate of NH_3 increasing, the amount of H, NH and CN (precursor of HCN, FCN) is increasing. The intensities of H, NH and CN luminescence peaks are increased but those of CF_2 and F luminescence peaks are slightly decreased. This result may indicate that reaction of generated HCN and FCN reduces the C_xF_y polymer. The C_xF_y polymer reduction reduces excessive protection film deposition which causes etchstop.

Relation to 21st COE Program

This research was performed as part of a "Fundamental Technologies for Scaled Devices".

Conclusions and Next Work

By addition of NH_3 to C_5F_8/Ar pulse-modulated plasma, sub-0.1μm size and high aspect ratio (>10) contact hole etching with vertically and excellent selectivity (SiO_2/Si≈80) is achieved.

This process could be used for the next generation ULSI devices (about 65 nm node MOSFET).

Furthermore, correlation between OES and etching properties is observed.

My next works are metal filling to small hole, and measuring characteristic of the device using this technique.

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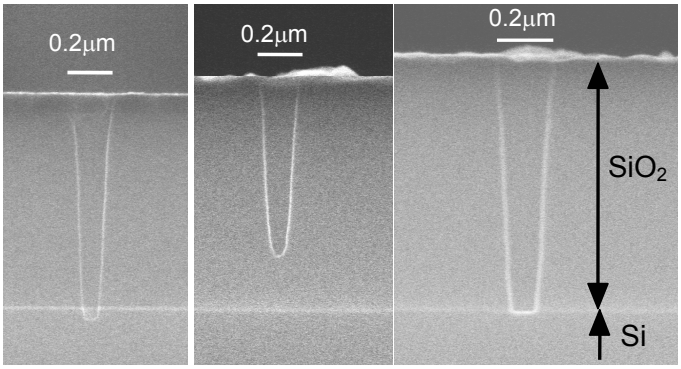
Published Papers and Patents

① Published Papers

M. Ooka, S. Yokoyama "SiO_2 Hole Etching Using Perfluorocarbon Alternative Gas with Small Global Greenhouse Effect": Jpn. J. Appl. Phys. **43** (2004) (in press).

Table 1 GWP and lifetime of some etching gases.

Gas	GWP_{100}	Lifetime (year)
CO_2	1	50-1200
CF_4	6500	50000
c-C_4F_8	8700	3200
c-C_5F_8	90	1



(a) O_2 added (b) H_2 added (c) NH_3 added

Fig. 2 SEM photograph of cross section of the 0.2μm contact hole etched with different addition gas.

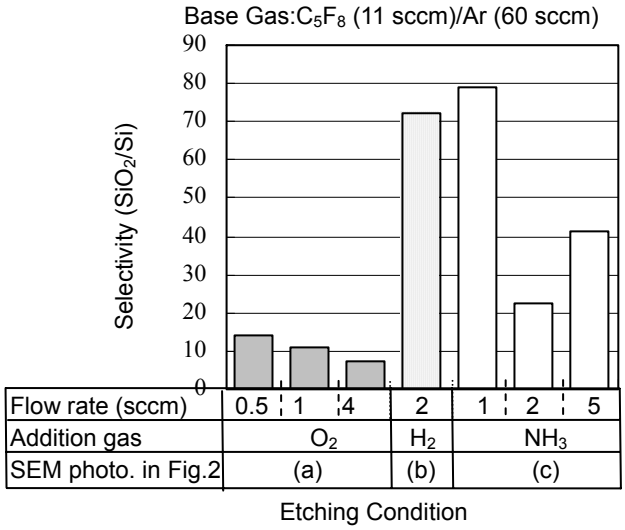


Fig. 4 SiO_2/Si etching selectivity for different addition gas and flow rate.

② Proceedings

1. M. Ooka and S. Yokoyama, "Excellent Contact-Hole Etching with NH_3 Added C_5F8 Pulse-Modulated Plasma" Extend. Abst. of the Int. Conf. on Solid State Devices and Materials (SSDM2003) (2003) pp. 454-455.

③ Patents

Nothing.

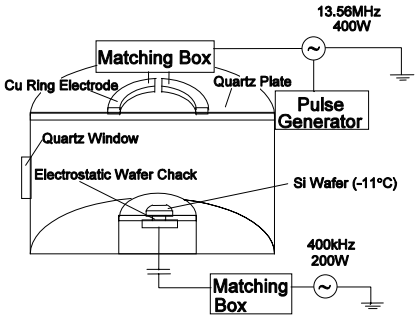


Fig. 1 Schematic diagram of ICP reactor.

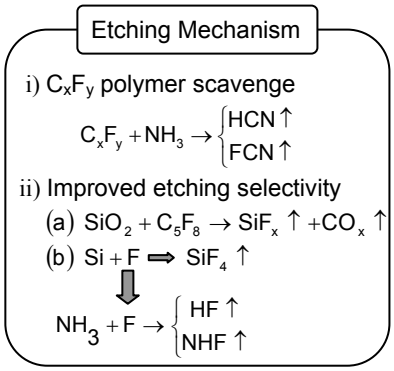


Fig. 3 Mechanism of NH_3 adding effect.

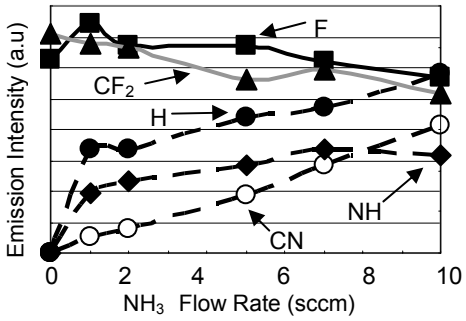


Fig. 5 OES intensity vs NH_3 flow rate.

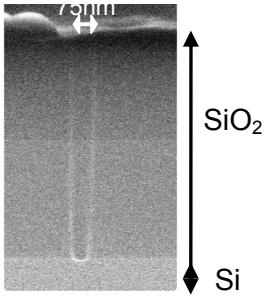


Fig. 6 SEM photograph of the cross section of the sub-0.1μm contact hole (RF ON: 50 μsec/OFF: 25 μsec, 70% over etch).

Photonic crystal for optoelectronic integrated circuits (OEICs)
-Technology and application of photonic crystal-

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Masaru Wake (Graduate School of Advanced Sciences of Matter, M2)

1. Introduction

Photonic crystals are new optical materials having periodically changed refractive index and considered to act as a base medium for future ultra-small large-scale photonic integrated circuits (PICs).[1] In order to realize high performance PICs, a three-dimensional photonic crystal with a perfect photonic bandgap is necessary.[2] The functional devices such as nano-ampere laser arrays and optical waveguides with sharp bends can be integrated using the three-dimensional photonic crystals in the PICs.

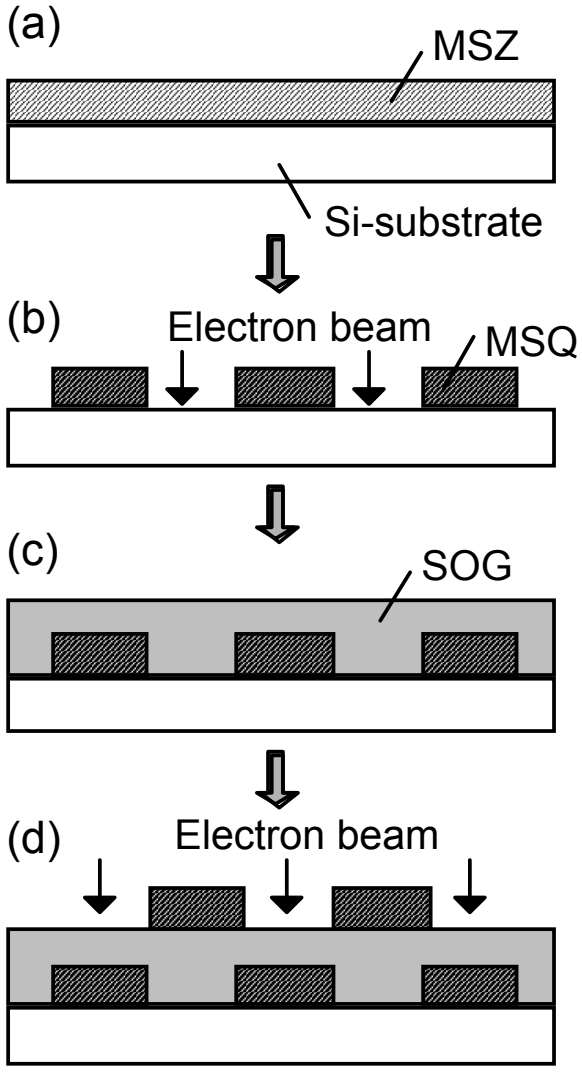

Figure 1 The proposed realization method for three-dimensional photonic crystals.

Therefore, we need the fabrication technique for three-dimensional photonic crystal to control the structure easily.

At the Research Center for Nanodevices and Systems (RCNS), Hiroshima University, we are studying the technology of three-dimensional photonic crystals not only for the Si-based large-scale PICs but also for optoelectronic integrated circuits (OEICs). The research topics developed so far are demonstrated.

2. Research Results

There have been a few reports of such a fabrication technique of three-dimensional photonic crystal. However, the reported methods for fabricating three-dimensional photonic crystals are fairly complicated[3,4] or have less flexibility of structure designing.[5] Also, realization of optoelectronic integrated circuits (OEICs) with low cost is difficult when Si-based materials[4,5] are not used for the fabrication. Recently, we have developed a direct patterning technique of interlayer dielectric films using the photosensitive methylsilazane (MSZ) film for multilevel interconnetions in ultra-large scale integrated circuits (ULSIs).[6-8] The photosensitive MSZ film can be directly patterned (without using the resist) by the use of electron-beam (EB) or ultraviolet lithography. In this process, EB-resist or photo-resist coating and dry etching is not necessary for the patterning. We applied this direct patterning technique to the formation of three-dimensional photonic crystals. Owing to this technique, the number of process steps can be reduced by about half for the fabrication of three-deminsional photonic crystals.

Figure 1 shows the proposed method. A photosensitive MSZ precursor (refractive index of 1.55) is spin coated on a Si wafer to form a 150-nm-thick film [Fig. 1(a)]. After prebaking, to form a basic two-dimensional structure, EB lithography is carried out [Fig. 1(b)]. After the development and curing, the photosensitive MSZ film is changed to methylsilsesquioxane (MSQ) film (refractive index of 1.45).[6] In these processes, both EB-resist and dry-etching processes are eliminated for the pattern formation and the desired pattern of MSQ film is formed. Then, spin-on-glass (SOG, refractive index of 1.38) film is spin coated on the

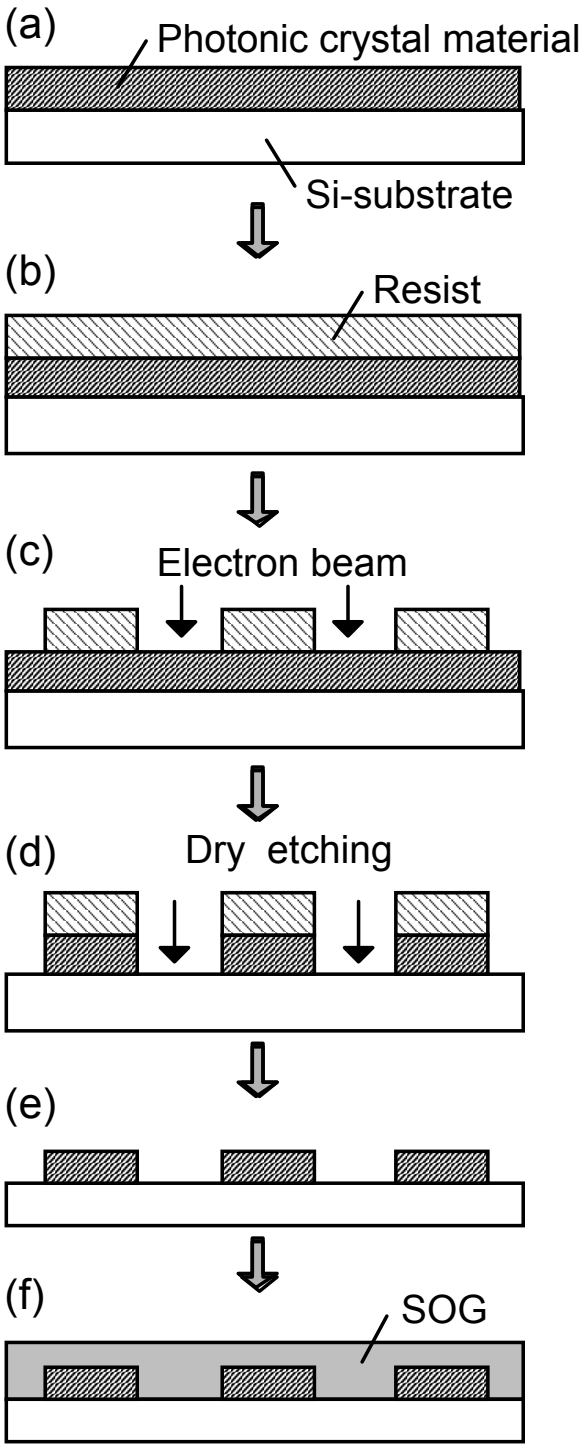

Figure 2 A conventional method for the fabrication of three-dimensional photonic crystals.

patterned film (200-nm-thick film is formed for a plane film) [Fig. 1(c)]. After baking, SOG film with flat top surface is formed. Repeating above processes, we can easily fabricate a three-dimensional photonic crystal having the periodically changed refractive index [Fig. 1(d)].

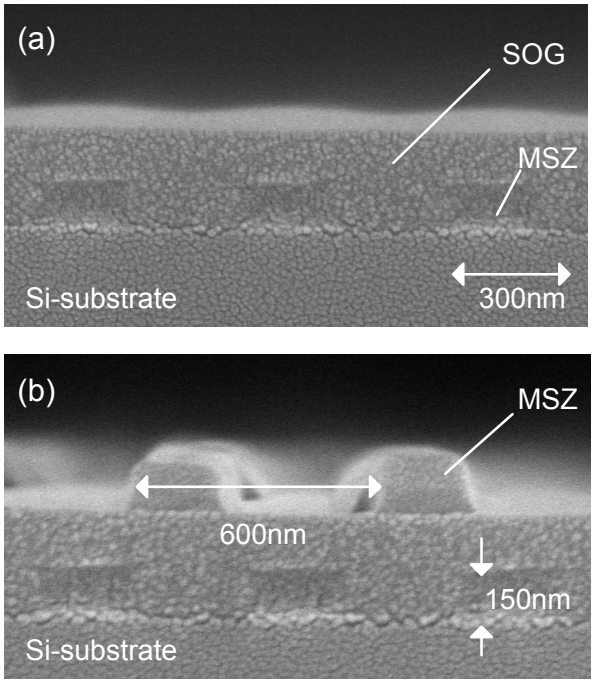

Figure 3 Cross sectional SEM image of the fabricated structure having MSZ stripe patterns.

On the other hand, in the conventional fabrication method, resist coating [Fig. 2(b)] after the film formation of the photonic crystal material having the refractive index different from that of SOG [Fig. 2(a)], dry etching of the material with the resist mask [Fig. 2(d)], and the resist mask stripping [Fig. 2(e)] are added compared with the proposed processes (Fig. 1). Therefore, the number of process steps in the proposed method is reduced by about half.

Figure 3 shows a SEM image of the fabricated structure. As seen in Fig. 3(a), a basic two-dimensional structure of the MSZ film with the stripe pattern is indeed formed and covered by the SOG film having the flat top surface. The line and space of the stripe pattern is 300 nm, which is suitable to the photonic crystal in the optical wavelength region (500 ~ 1600 nm). Owing to the flatness of the top SOG surface, the periodic two-dimensional structure of the MSZ can be stacked repeatedly [Fig. 3(b)].

Figure 4 shows the bird's-eye view SEM image of the woodpile structure fabricated using the proposed process. The stripe patterns of the stacked MSZ layer crosses over the underlying one.

Figure 5 shows a SEM image of a two-dimensional structure with a Y-branch wave guide fabricated using the proposed technique. Thus, we can easily incorporate such basic two-dimensional structures into three-dimensional photonic crystals for functional devices.

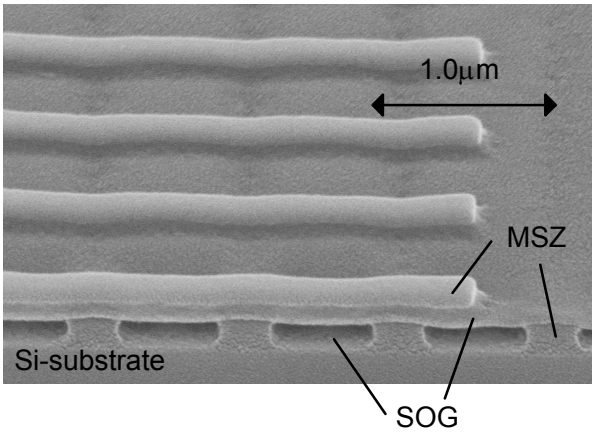

Figure 4 Bird's-eye view SEM image of the fabricated woodpile structure.

Our process proposed in this study is compatible with those of ULSIs because the direct patterning technique has been primarily developed for the dielectrics for interconnections in ULSIs. The compatibility leads to the capability of utilizing state-of-the-art nanostructure-fabrication technologies in ULSIs. Moreover, we can combine the fabricated photonic crystals with ULSIs easily. This is advantageous to the realization of OEICs with low cost.

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3. Summary

In summary, we have successfully applied the direct patterning technique to the formation of three-dimensional photonic crystals. The basic structures with stacked striipe pattern, woodpile structure, and two-dimensional Y shape waveguide have been realized. Utilizing this process, the number of process steps can be reduced by about half. The proposed process is promising for realizing low cost OEICs.

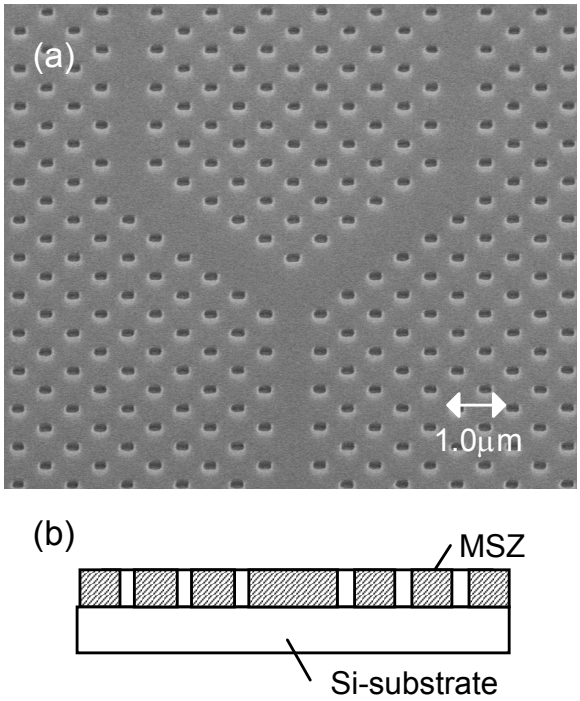

Figure 5 Top view SEM mage of the fabricated two-dimensional Y-branch waveguide structure (a) and the schematic of the cross section (b).

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Achievements

Photonic Crystal

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