

Contents

Foreword from President

Message from Program Leader

1. Outline of the Objectives and Research Results of the 21 st Center of Excellence “Nanoelectronics for Terabit Information Processing”	1
2. Members of the 21st Century COE Program	7
3. Achievements, Published Papers, Patents, and Awards	11
4. Research Results of Each Subject	
4-I. Circuits and Systems	
4-I-1. Three Dimensional Integration Architecture for Tera-bit Information processing A. Iwata, M. Sasaki, S. Kameda. H. Ando, T. Yoshida, M. Siozaki, and M. Ono	43
4-I-2. Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors M. Sasaki, D. Arizono, and A. Iwata	47
4-I-3. A Brain-type Vision System with Wireless Interconnections S. Kameda and A. Iwata	51
4-I-4. Development of Real-time Multi-object Recognition System H. Ando and A. Iwata	53
4-I-5. A Study on Neural Sensing System T. Yoshida and A. Iwata	55
4-I-6. CDMA Serial Communication Chips for Highly Flexible Robot Brain M. Siozaki, A. Iwata, and M. Sasaki	57
4-I-7. Design of a Strategy Learning Model for Robot Brain and LSI Implementation of the Model M. Ono, M. Sasaki, and A. Iwata	59
4-I-8. Associative-Memory-Based Systems with Recognition and Learning Capability — Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search in Large Reference-Pattern Space — H. J. Mattausch, T. Koide, Yuji Yano, K. Kamimura, and K. M. Rahman	61
4-I-9. Associative-Memory-Based Systems with Recognition and Learning Capability H. J. Mattausch, T. Koide, M. Mizokami, and Y. Shirakawa	67

4-I-10. Image Processing Front End for Associative Memory-Based Systems — Hardware-Efficient Low-Power Motion-Picture Segmentation by Pipeline Processing of Tiled Images with Cell-Network —	73
T. Koide, H. J. Mattausch, T. Morimoto, Y. Harada, H. Adachi, and O. Kiriama	
4-I-11. Optimized Mixed Digital-Analog Nearest-Match Circuit for Fully-Parallel Associative Memories	79
K. M. Rahman, K. Kamimura, H. J. Mattausch, and T. Koide	
4-I-12. Development of Digital-CMOS-Based Real-Time Color -Motion Picture Segmentation Architecture and its LSI Chip Verification	81
T. Morimoto, T. Koide, and H. J. Mattausch	
 4-II. Device Modeling	
4-II-1. TEG Design for HiSIM Model-Parameter Extraction and Parameter Extraction with Single Structures	83
M. M.-Mattausch, T. Mizoguchi, and Y. Uetsuji	
4-II-2. Measurement of Thermal Noise for 100nm-MOSFET and Its Modeling	85
M. M.-Mattausch and S. Hosokawa	
4-II-3. Inversion Charge Model of SOI-MOSFET for Circuit Simulation and $1/f$ Noise Analysis	87
M. M.-Mattausch and N. Sadachika	
4-II-4. Modeling of Optoelectronic Devices	89
M. M.-Mattausch, K. Konno, O. Matsushima, K. Hara, and G. Suzuki	
4-II-5. Modeling of $1/f$ Noise with HiSIM for 100 nm CMOS Technology	92
H. Ueno and M. M.-Mattausch	
4-II-6. Analysis and Modeling of Carrier Transport in Photodiodes	98
K. Konno and M. M.-Mattausch	
4-II-7 To Improve HiSIM-SOI for Real Application	100
M. H. Bhuyan and M. M.-Mattausch	
 4-III. Nanodevices and Processing	
4-III-1. Workfunction Tuning for Single-Metal Dual-Gate CMOS	103
K. Shibahara, K. Sano, and M. Hino	
4-III-2 Fabrication and Evaluation Technique for Ultra-Shallow Junction	105
K. Shibahara, T. Eto, and E. Takii	
4-III-3. Research and Development of Three-Dimensional MOS Transistors	107
H. Sunami, K. Okuyama, A. Katakami, K. Kobayashi, and S. Matsumura	
4-III-4. Study in 3-Dimensional new structure MOS Transistor	115
K. Okuyama, K. Kobayashi, S. Matsumura, and H. Sunami	

4-III-5.	Development of Novel Functional Si-based Devices Using Self-assembled Nanostructures for Multivalued Memory Operation Ultimate Photo-sensing and Molecular Recognition	117
	S. Miyazaki, M. Ikeda, Y. Darma, T. Shibaguchi, S. Higashi, and H. Murakami	
4-III-6.	Control of Si Quantum Dot Nucleation by Remote Plasma Treatment	125
	S. Higashi, K. Makihara, H. Murakami, and S. Miyazaki	
4-III-7.	Low resistive gate electrode/high-k gate dielectrics stacked structure and its electron device application	129
	H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi, and S. Miyazaki	
4-III-8.	Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment	133
	K. Makihara, S. Higashi, and S. Miyazaki	
4-III-9.	Investigation on hard breakdown mechanism of high-k gate by conductive-AFM	135
	Pei yanli, S. Higashi, and S. Miyazaki	
4-III-10.	Intra/Inter-Chip Wireless Interconnect System for ULSI (1) — Si Integrated Antenna —	137
	T. Kikkawa, K. Kimoto, and S. Watanabe	
4-III-11.	Intra/Inter Chip Wireless Interconnect System for ULSI (2) — A CMOS Ultra Wideband Transmitter —	140
	P. K. Saha, N Sasaki, and T. Kikkawa	
4-III-12.	Intra/Inter-Chip Wireless Interconnect System for ULSI (3) — A CMOS Ultra Wideband Receiver —	142
	N. Sasaki, P. K. Saha, and T. Kikkawa	
4-III-13.	Intra/Inter Chip Wireless Interconnect System for ULSI (4) — Low-k/Cu Interconnect —	144
	T. Kikkawa and S. Sakamoto	
4-III-14.	Development of Optically Interconnected LSI — Integration of Ring Resonator Switches using Electro-Optic Materials —	147
	S. Yokoyama, Y. Tanushi, M. Wake, and K. Wakushima	
4-III-15.	Design and Fabrication of Race-Track Optical Ring Resonator	152
	Y. Tanushi, M. Wake, and S. Yokoyama	
4-III-16.	Etching Properties and Optical Emission Spectroscopy of NH ₃ Added C ₅ F ₈ Pulse-Modulated ICP Plasma	154
	M. Ooka and S. Yokoyama	
4-III-17.	Photonic crystal for optoelectronic integrated circuits (OEICs) — Technology and application of photonic crystal —	156
	A. Nakajima, S. Yokoyama, and M. Wake	