広島大学21世紀COEプログラム
テラビット情報ナノエレクトロニクス

成果報告書
(２００５年度要約版)

広島大学

ナノデバイス･システム研究センター
先端物質科学研究科　半導体集積科学専攻

http://www.rcis.hiroshima-u.ac.jp/21coe/

２００６年3月

目次

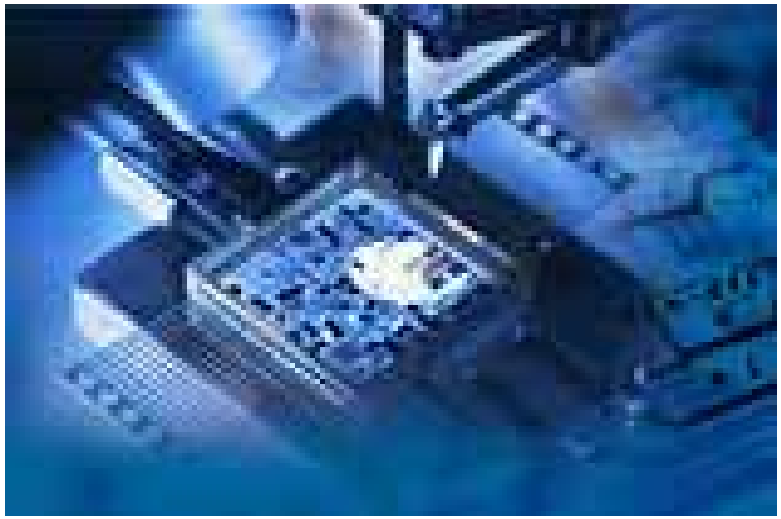
ＣＯＥの概要･目標

研究

･回路･モデル･デバイスの3領域を融合した新学問領域の形成
･三次元集積技術と学習･認識システムの基盤技術の構築

教育

･広い視野と実行力を備えた
次世代のリーダの
資質を持った博士研究者の育成



三研究領域と主要研究メンバー

回路・システム アーキテクチャ

1．RF・アナログ回路
（岩田，佐々木、吉田）
2．連想メモリベース、画像処理システム
（マタウシュ、小出）
3．三次元集積画像認識システム
（岩田，佐々木）

デバイス モデリング

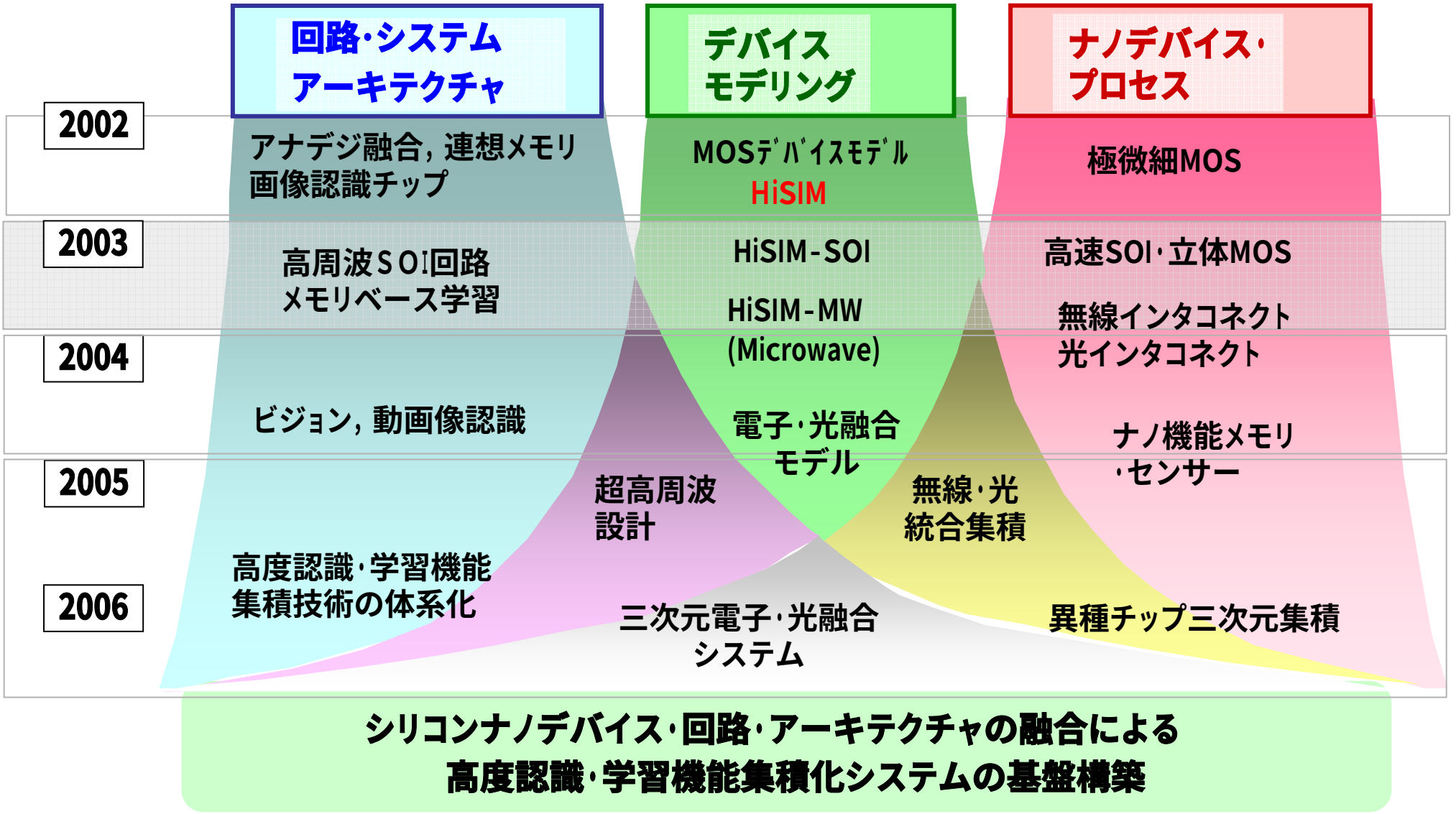
ドリフト・拡散物理に基づくデバイスモデル
HiSIM
電子光融合デバイス
三次元MOS
（三浦、江崎、マタウシュ）

ナノデバイス・プロセス

1．微細化基盤技術
（芝原，中島，宮崎）
2．微細SOIデバイス
（角南，三浦）
3．ナノ機能メモリ
（宮崎，東，村上）
4．無線インタコネクト
（吉川，佐々木）
5．光インタコネクト
（横山，三浦）

ポスドク研究員：10名、ドクター学生：16名

拠点形成計画（3本柱の研究領域と融合）



シリコンナノデバイス・回路・アーキテクチャの融合による
高度認識・学習機能集積化システムの基盤構築

2008年の研究到達点

1．テラビット情報処理三次元集積システム（3DCSS）の基盤技術

2種の無線方式によるテラビット・チップ間通信の実現

3D通信プロトタイプでTbit通信性能を実証

2．3DCSSを応用した高度な学習・認識システム基盤技術

人間より高速なマルチオブジェクト認識システムの基盤技術

試作チップを用いたプロトタイプでTbit情報処理の原理を実証

3．HiSIMモデル：国際貢献と回路・デバイス融合技術の進展

4．微細デバイス技術：Tbit情報処理実現の基盤技術

テラビット情報（処理）の定義

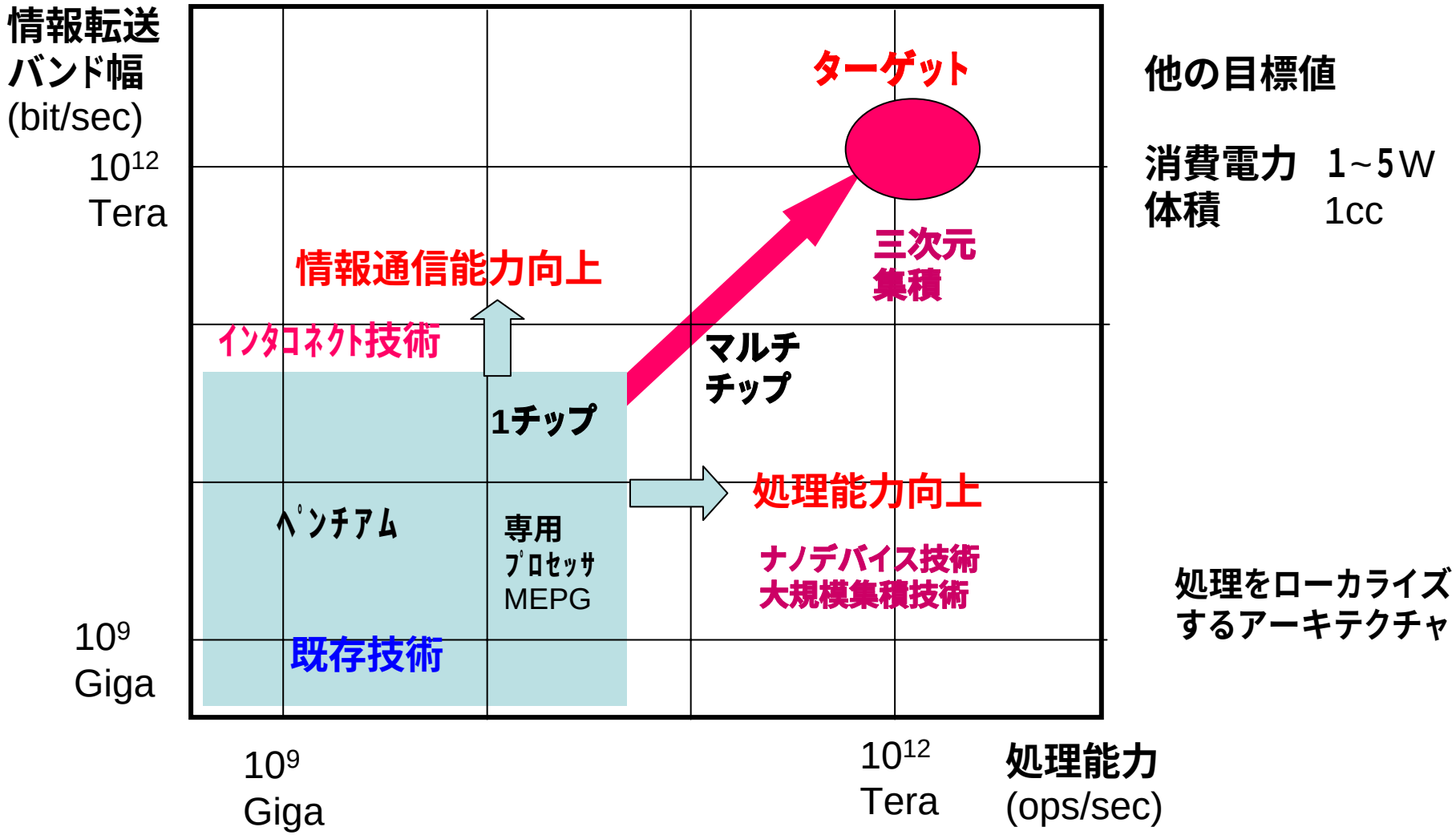
Tops情報処理能力／Tbps情報転送レートを実現し，

人間より高速な視認機能を実現する

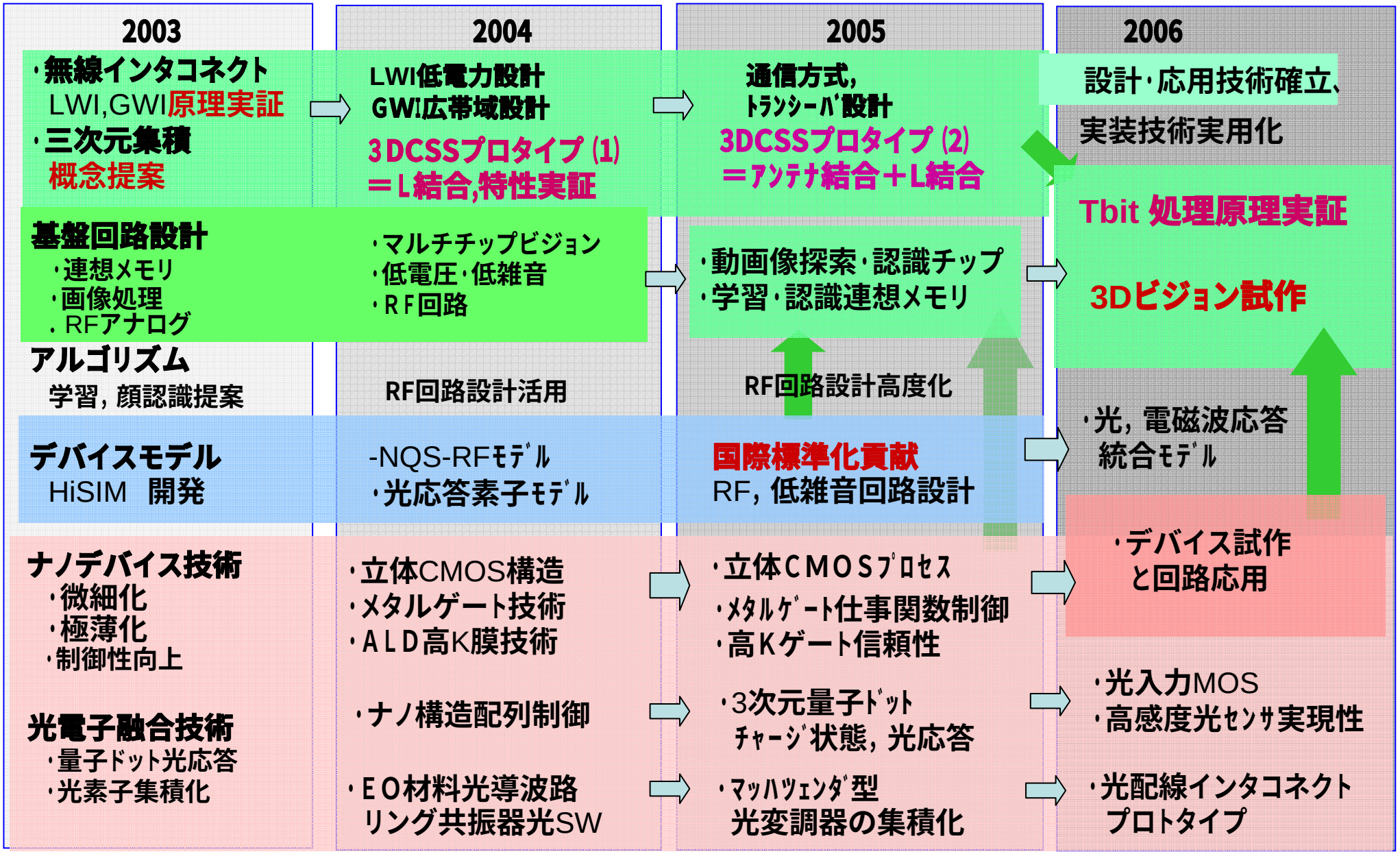
情報処理能力　Tops= 1Gops x 1000 Proc.〜10Gops x 100 Proc.

情報転送能力　Tbps=1Gbps x 100CHx 10chip 〜5Gbps x 20CH x 10chip

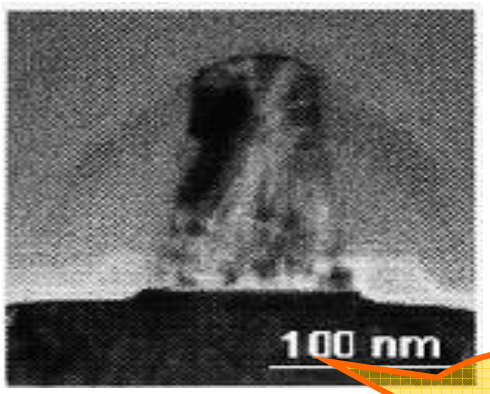
三次元集積テラビット情報処理のターゲット



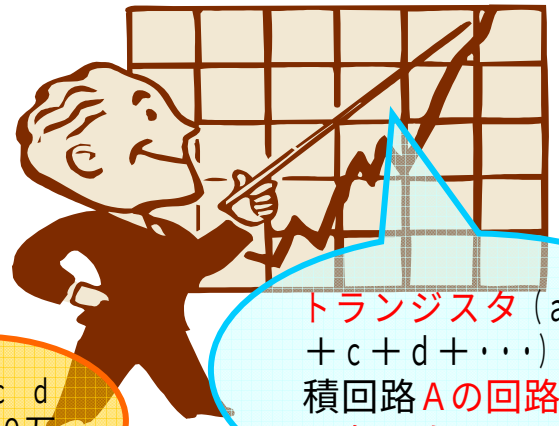
ＣＯＥのゴールへの道筋



MOSトランジスタのモデル：HiSIM

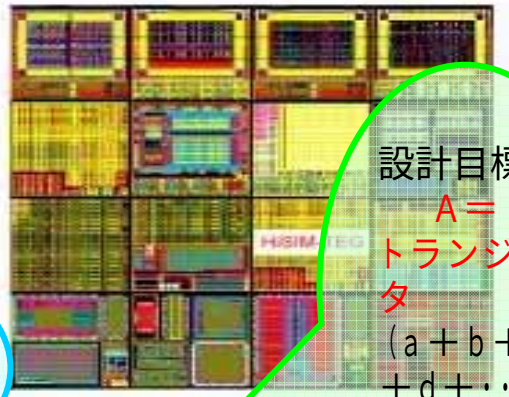


トランジスタ



a b c d ･･･100万個

トランジスタ（a＋b＋c＋d＋･･･）＝集積回路Aの回路特性となるかシミュレーション



集積回路

設計目標 A＝トランジスタ（a＋b＋c＋d＋･･･）？

トランジスタを１０００万個組み込むための橋渡し役

表面ポテンシャルモデル（HiSIM）が優れている点

（1）計算時間が短い
（2）表面ポテンシャル（モデルの核）が正確
（3）モデルパラメタのスケーリングが可能
（4）技術の変化に対応
（5）ノイズ特性の予測が可能
（6）ＲＦ回路シミュレーションが容易
（7）Multi-Gate MOSFETへの拡張が容易

HiSIM: Hiroshima University STARC IGFET

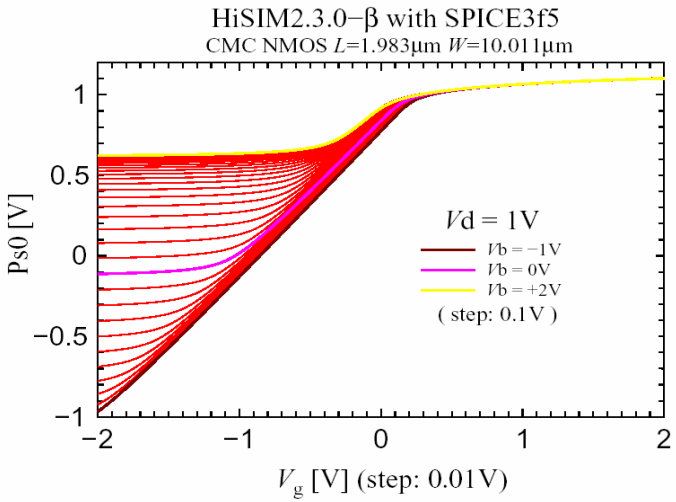
HiSIMがPSPより優れた点

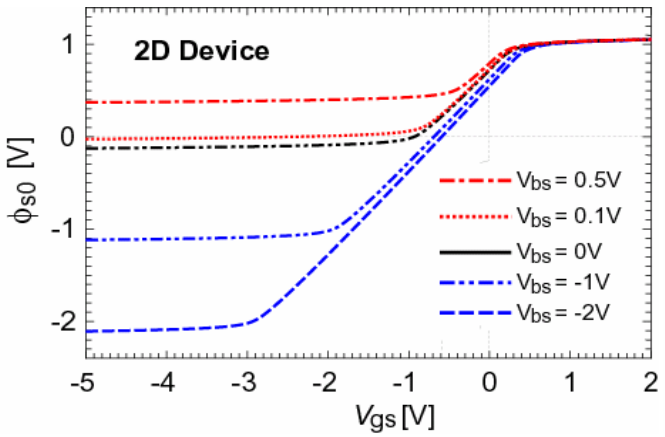
(2) 表面ポテンシャル (モデルの核) が正確

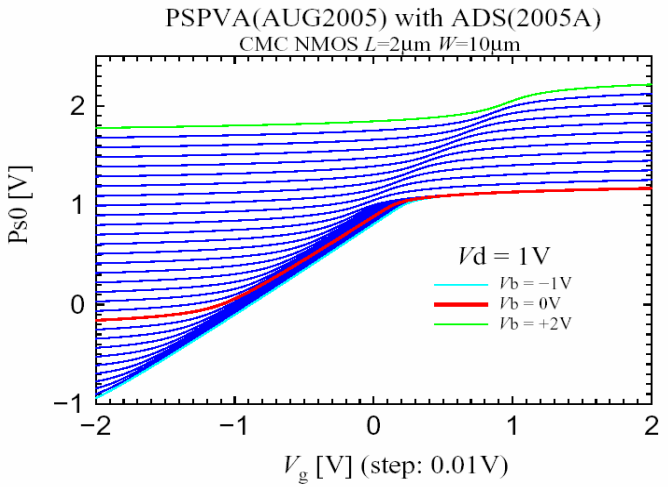
HiSIM

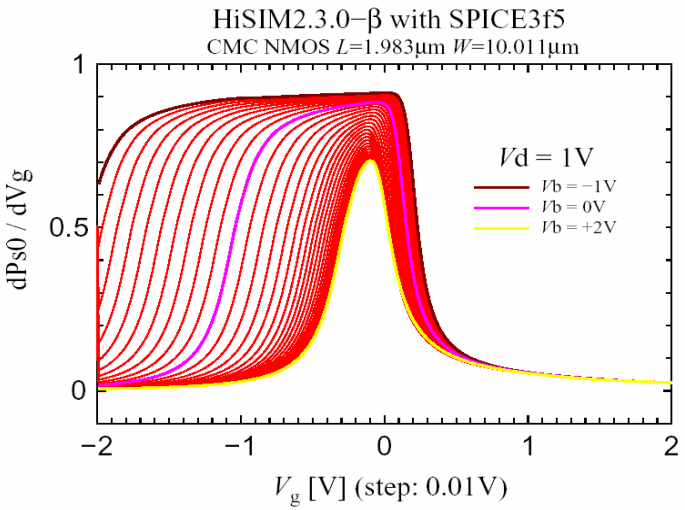
2Dデバイスシミュレーション

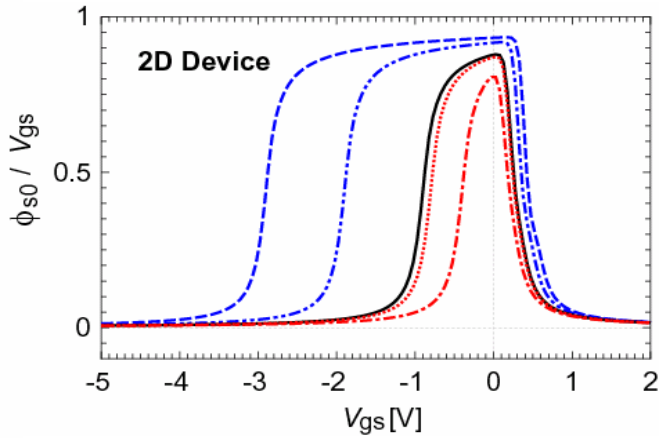
PSP

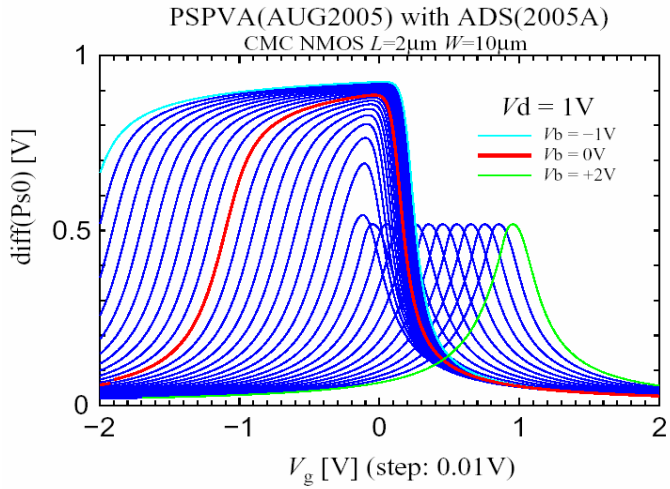








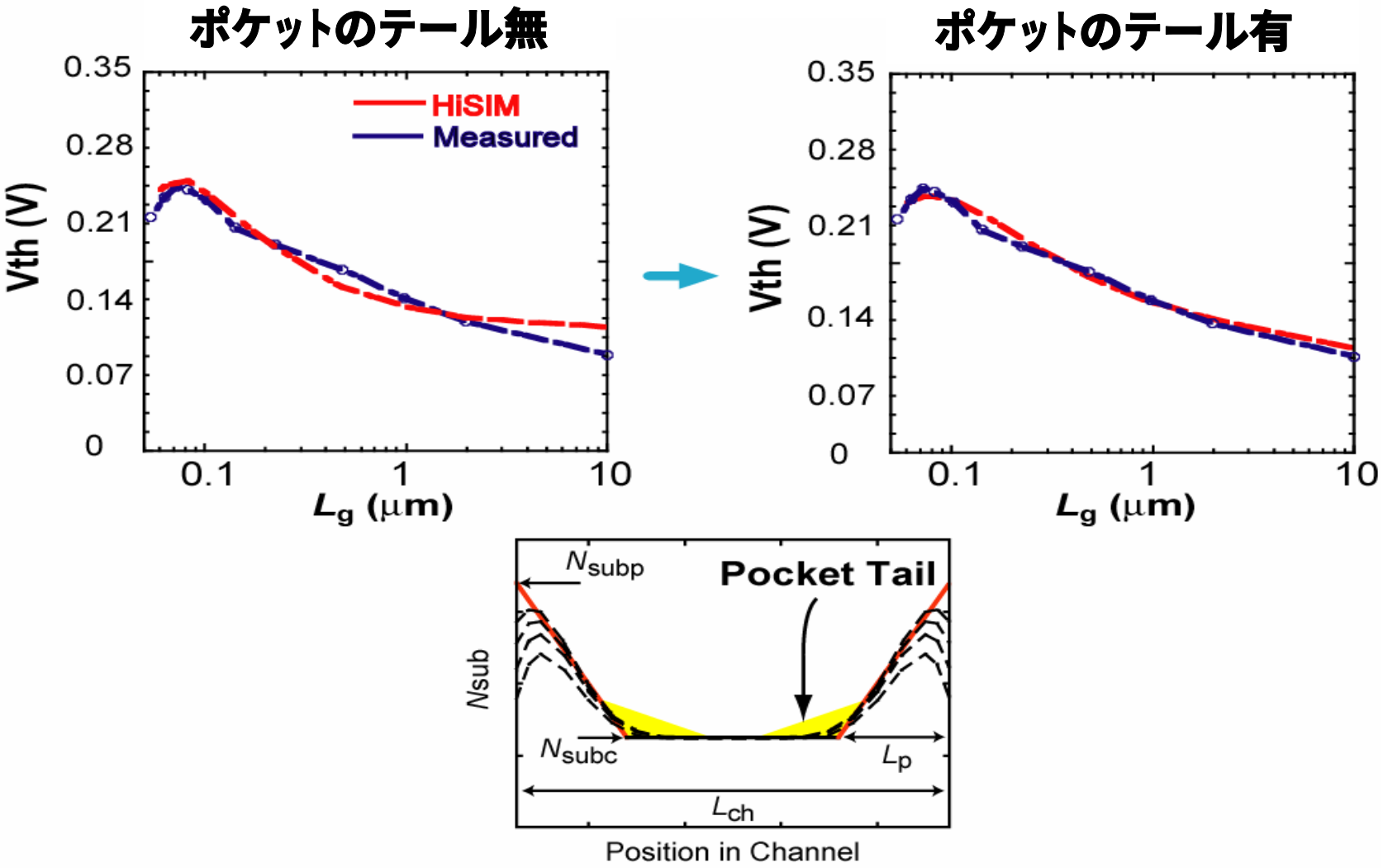




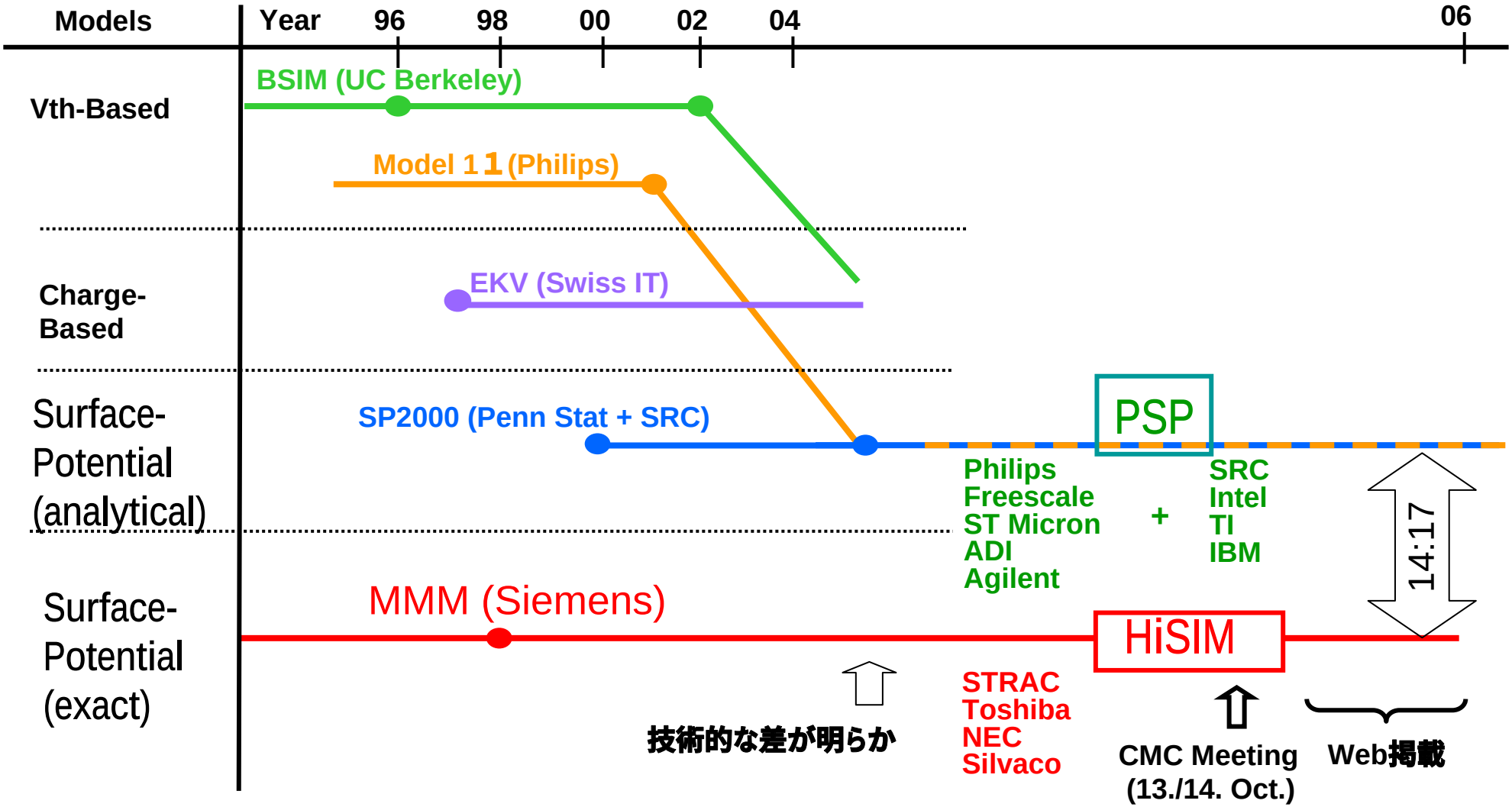
HiSIMは2Dデバイスシミュレーション結果と同じ

HiSIMがPSPより優位な点

(4) デバイス技術の微細化に対応した予測が可能



次世代ＭＯＳモデル国際標準化活動



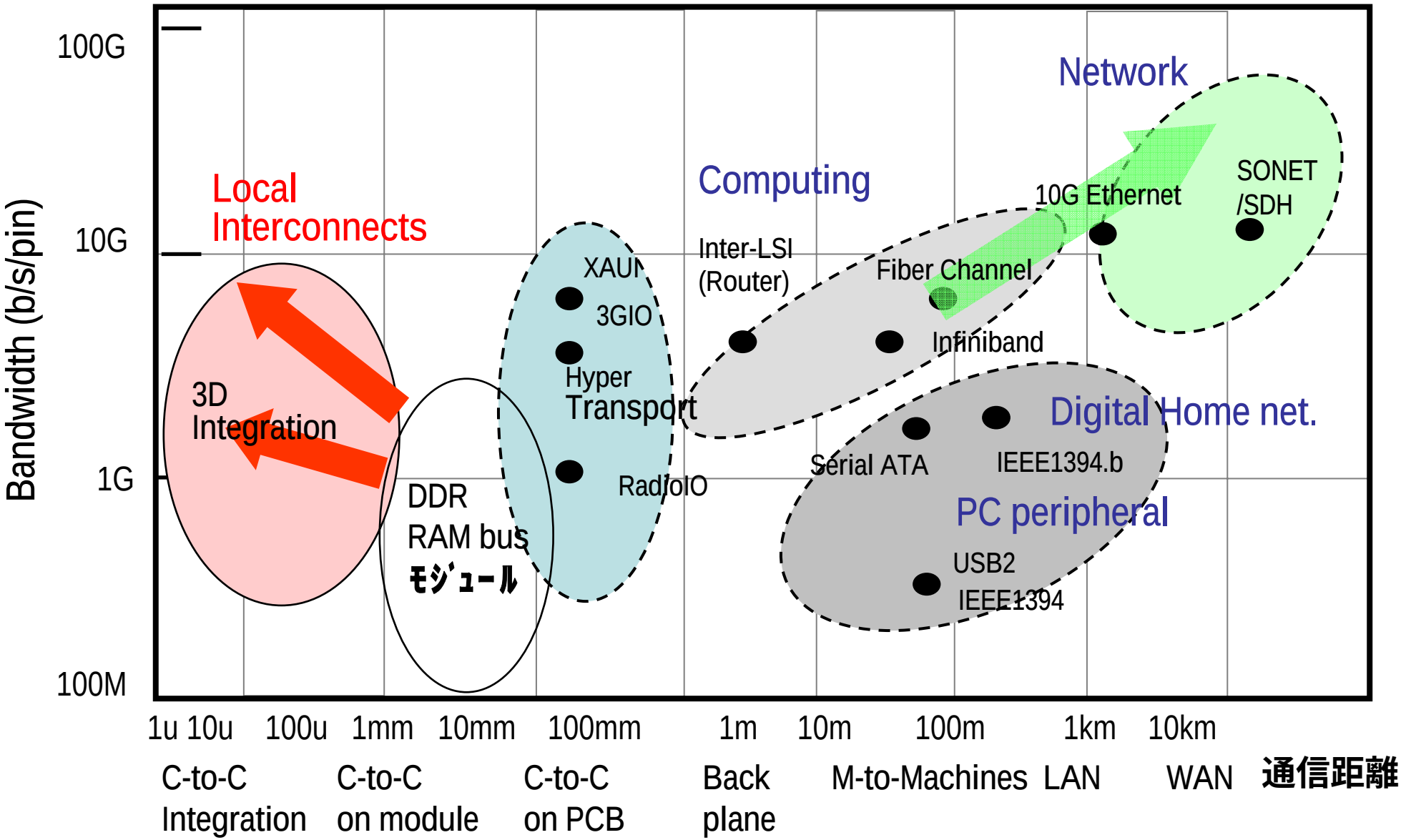
無線インタコネクト技術

通信と集積技術の融合

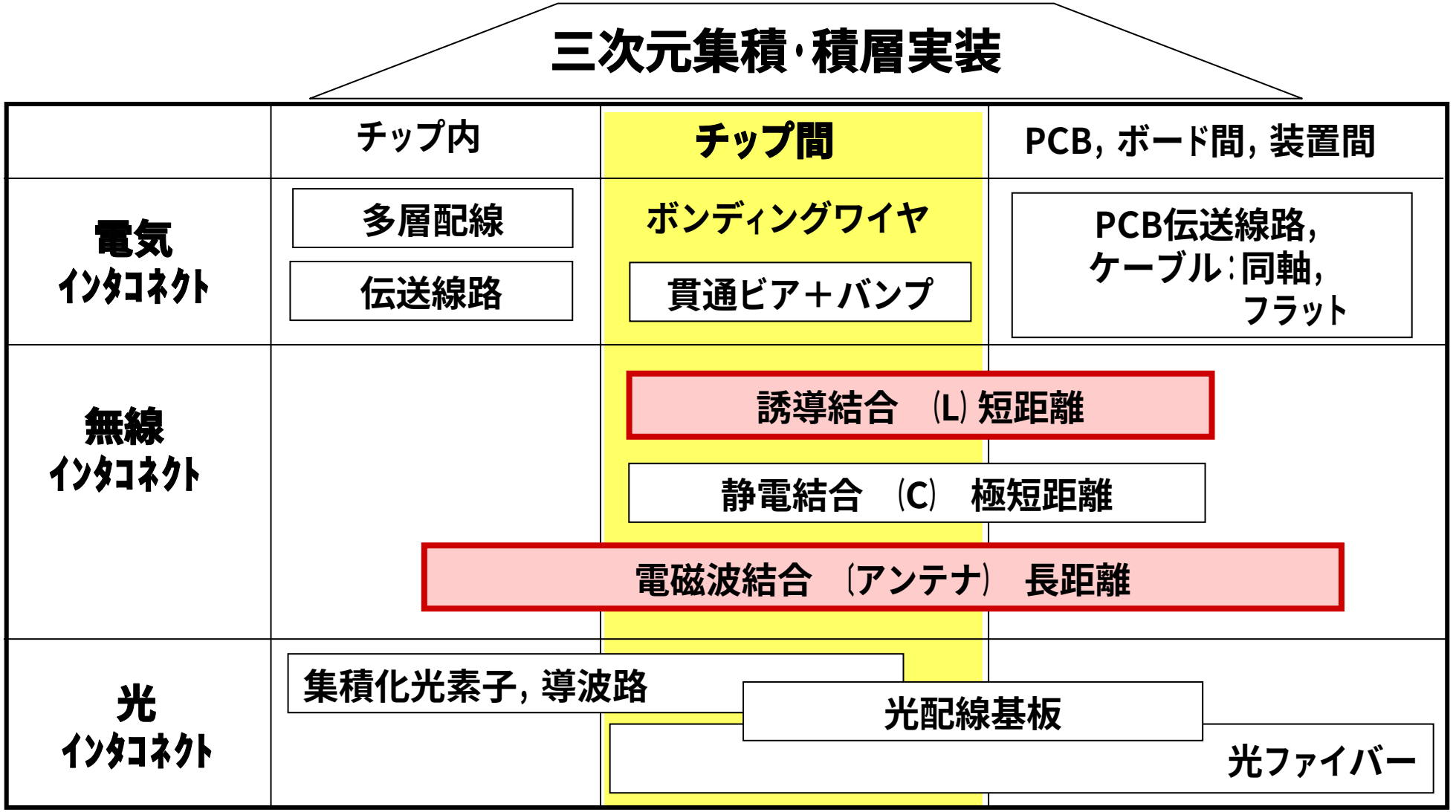
1. 集積化アンテナを用いたチップ間無線インタコネクト
   - 周波数20GHzの正弦波信号のSiチップ間送受信を実証
   - 周波数3GHzのガウシアンモノサイクルパルスで送受信を実証
   - UWB方式送受信回路を設計して，通信特性評価
   - 10チップにわたる*GWI*: *Global Wireless Interconnect*の実現見通し

2. 集積化インダクタを用いた隣接チップ間無線インタコネクト
   - インダクタ共振現象を利用した，高速・低電力通信回路を考案
   - テストチップ試作・評価により1Gbps (@0.84mW)の通信を実証.
   - 低電力化，小面積化により*LWI*: *Local Wireless Interconnect* の実現見通し

極短距離インタコネクションの位置づけ

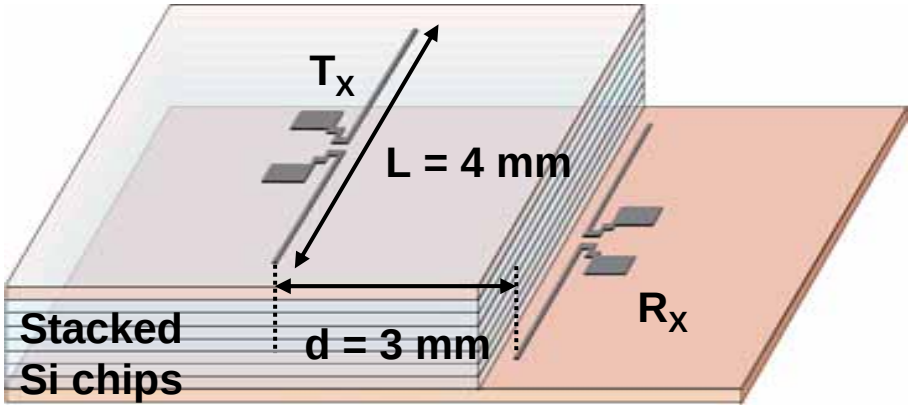


インタコネクト技術の適用領域



集積化アンテナによるUWB信号伝送

Si基板を通して20GHzのパルス電磁波が伝搬し、UWB通信ができることを実証。
無線三次元集積におけるグローバル無線インタコネクションの基礎データを取得。

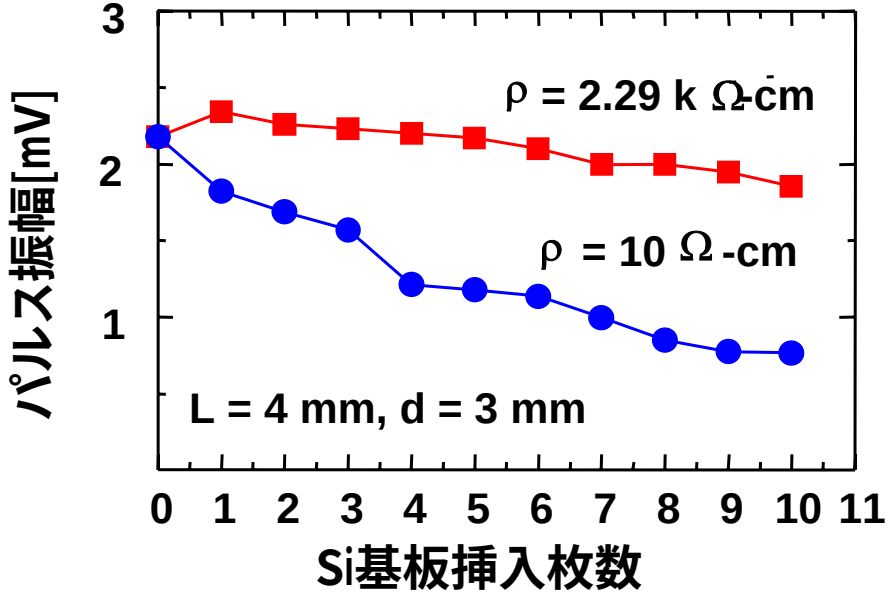


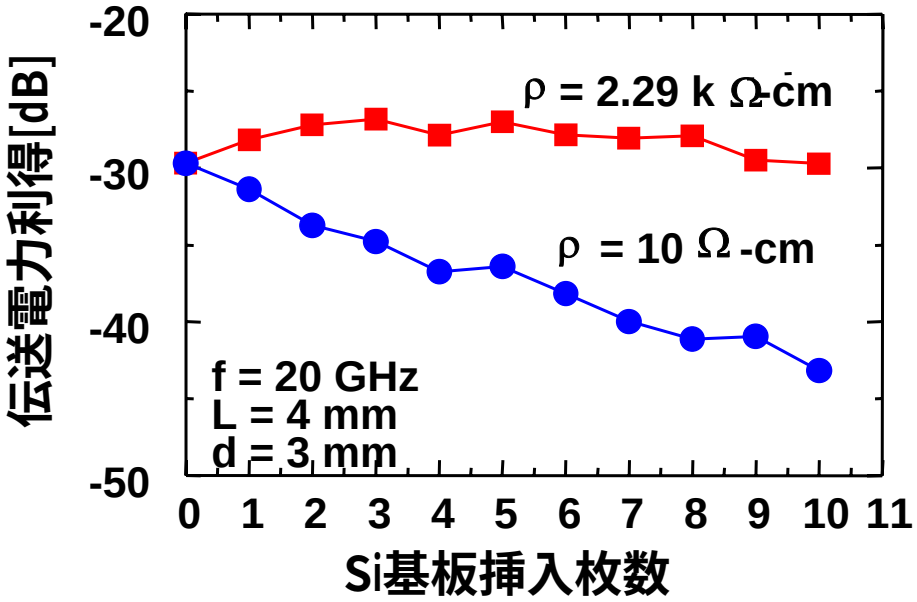
Siチップ積層構造

信号減衰率のSi 基板抵抗率依存性

- 4.9 dB/mm (ρ = 10 Ω·cm)
- 0.4 dB/mm (ρ = 2.29 kΩ·cm)

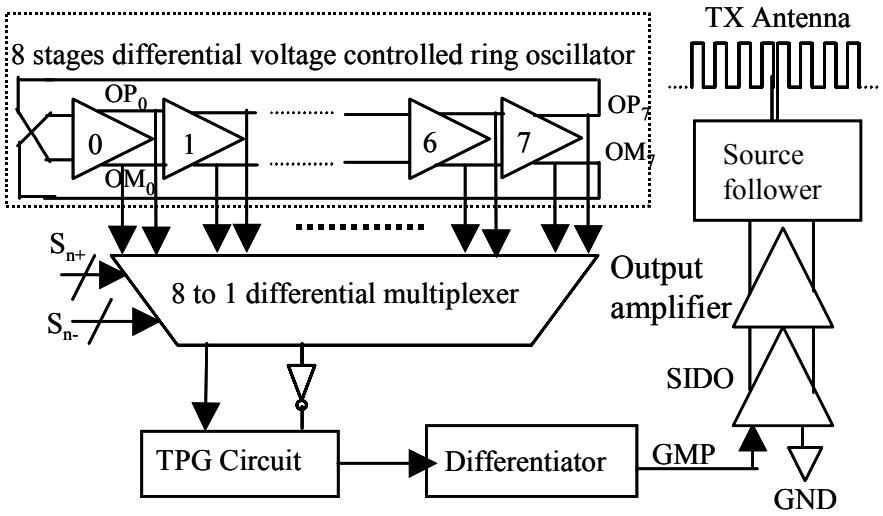
K. Kimoto et al.,, SSDM 2004



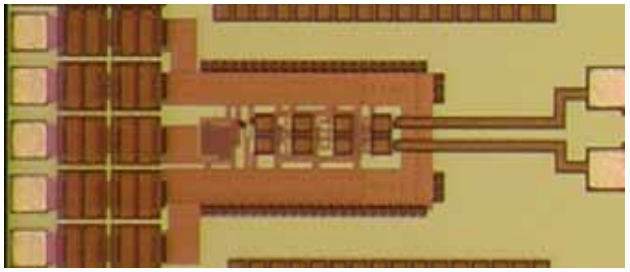


Siチップ間UWB送信回路／受信回路

ガウシアンモノサイクルパルス送信回路

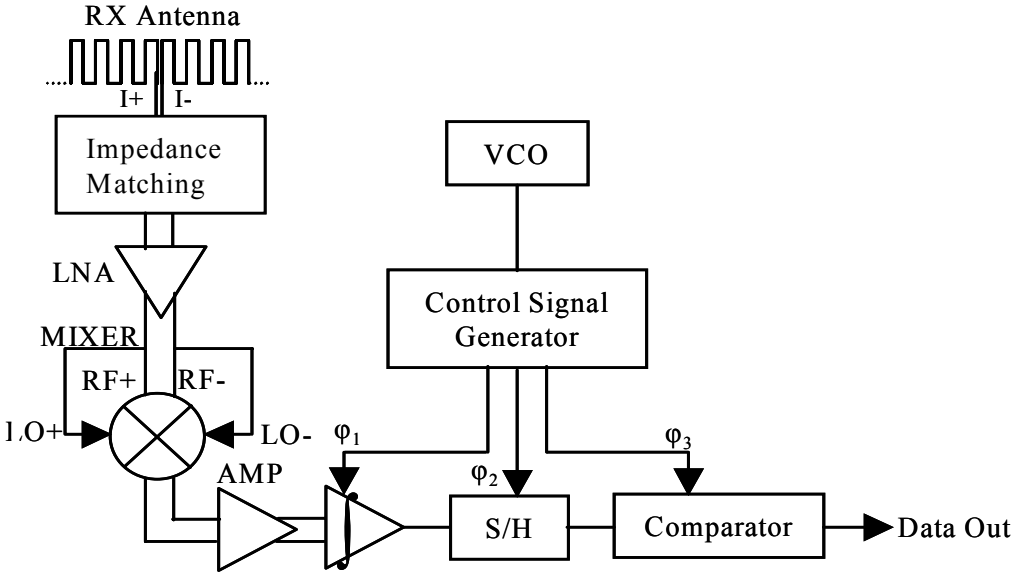


パルス幅	0.46ns (f_c=2.17GHz)
面積	0.03mm^2
消費電力	21.6mW
データレート	1.16Gbps

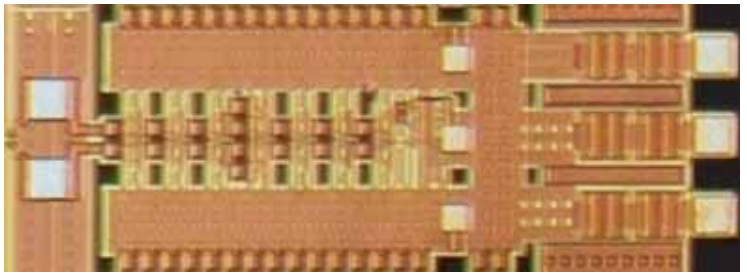


国際会議発表 Symposium on VLSI Circuits 2006

UWB信号の受信復調回路

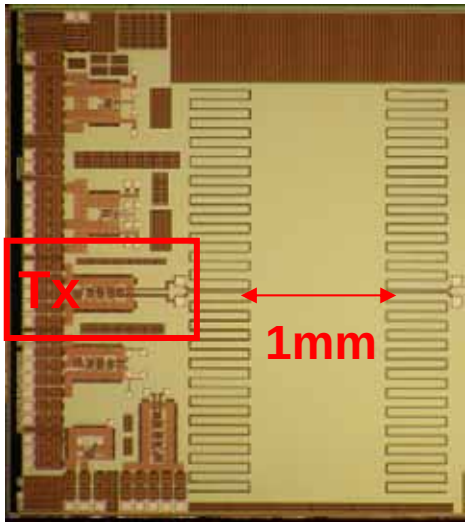


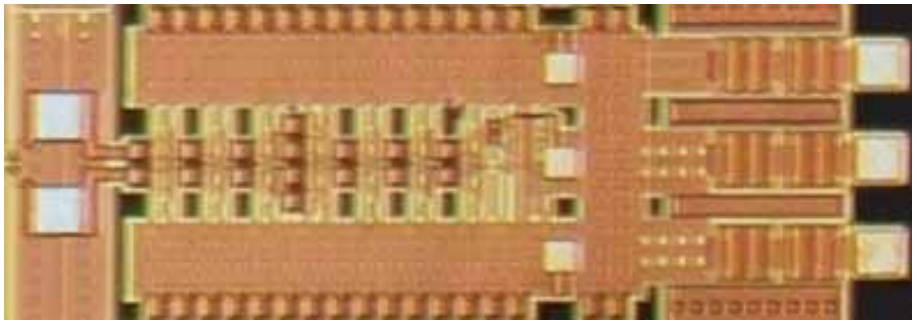
3dB 帯域幅	3GHz at f_c=3GHz
面積	0.61mm^2
消費電力	32mW
復調レート	250〜400Mbps



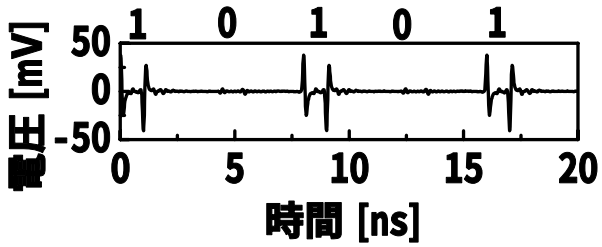
N. Sasaki, et al., IWUWBT 2005

Siチップ間UWB送信回路／受信回路

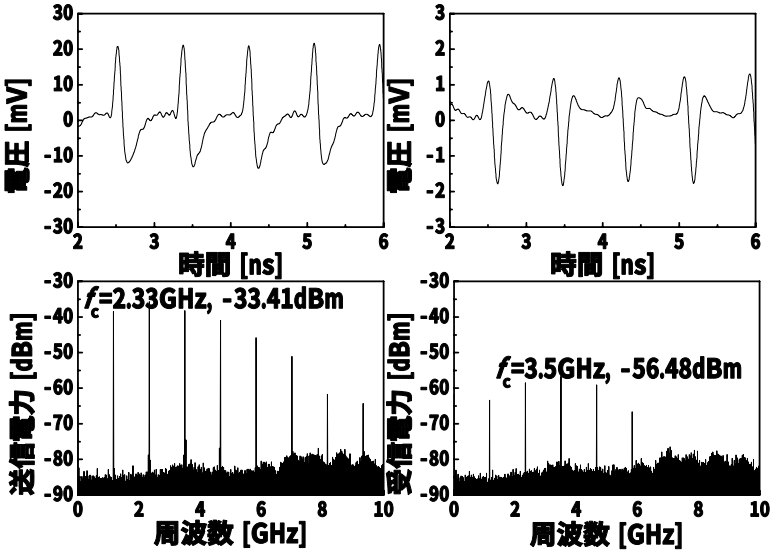




入力
(GMP)



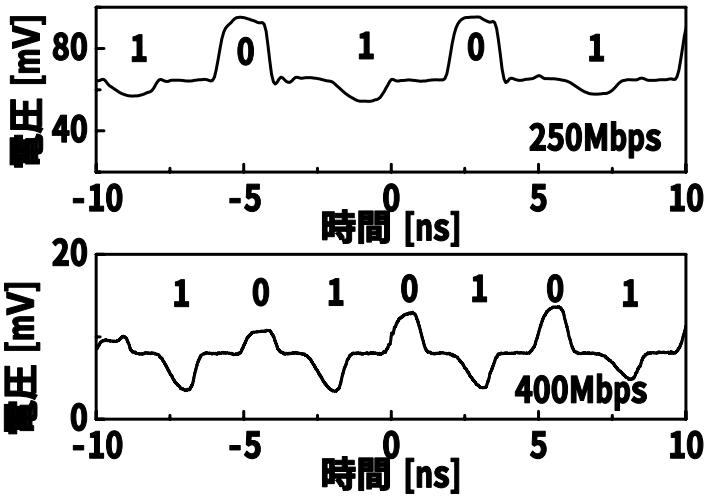
送信波形　　受信波形



GMPのオンチップ生成、送信に成功

OOK変調

出力復調
データ



V_{pp}=63mVのGMPを復調。データレート: 400Mbps

無線インタコネクト技術

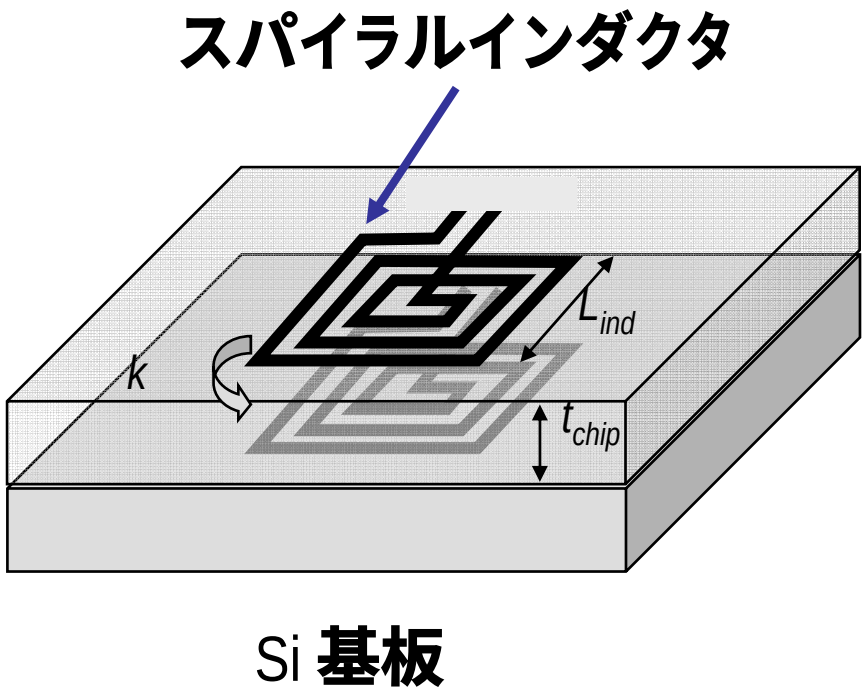
通信と集積技術の融合

1. 集積化アンテナを用いたチップ間無線インタコネクト
   ・周波数20GHzの正弦波信号のSiチップ間送受信を実証
   ・周波数3GHzのガウシアンモノサイクルパルスで送受信を実証
   ・UWB方式送受信回路を設計して，通信特性評価
   ・10チップにわたる*GWI：Global Wireless Interconnect*の実現見通し

2. 集積化インダクタを用いた隣接チップ間無線インタコネクト
   ・インダクタ共振現象を利用した，高速・低電力通信回路を考案
   ・テストチップ試作・評価により1Gbps (@0.84mW)の通信を実証.
   ・低電力化，小面積化により*LWI: Local Wireless Interconnect*
   の実現見通し

インダクタ共振による無線インタコネクト　LWI

- スパイラルインダクタでカップリング
- LC共振特性の利用



3Dカスタムスタックシステム

- 大規模なシステム
- 高機能なシステム

現在の3次元集積システム

- チップ間配線が複雑
- 高度な位置合わせが必要
- 内部チップの放熱が困難

オンチップ･スパイラル･インダクタ

CMOSプロセスの多層配線で実現可能

自己共振周波数 $f_{self} = \frac{1}{2\pi\sqrt{LC}}$

Q値（振幅の大きさ） $Q_{LC} \propto \sqrt{\frac{L}{C}}$

Qを下げずに共振周波数を下げる

↓

インダクタンスの増加

↓

多層配線を利用し，
スタック型インダクタを作成

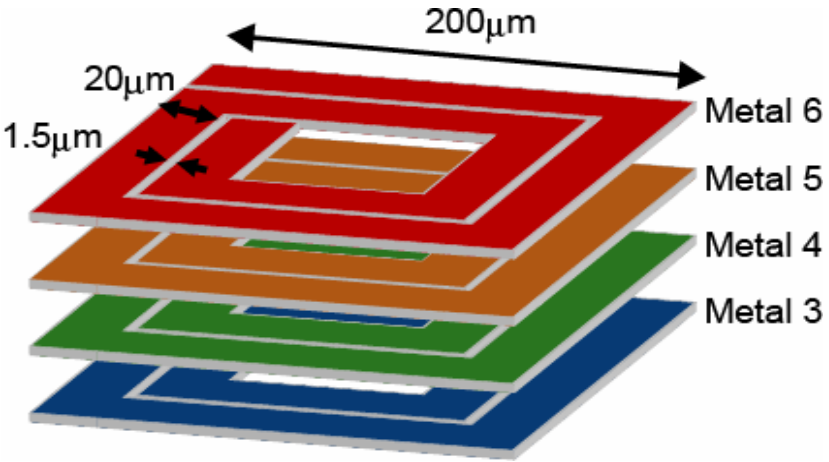


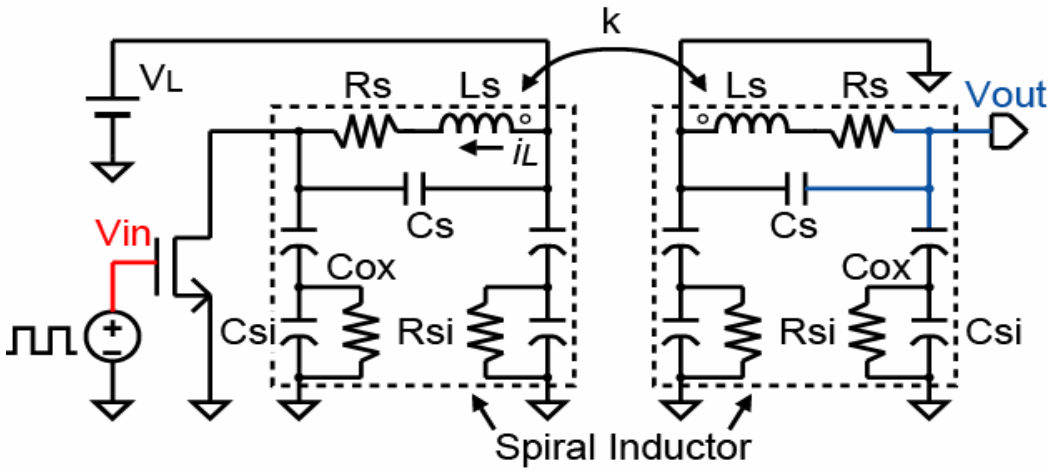
図　スタック型インダクタ

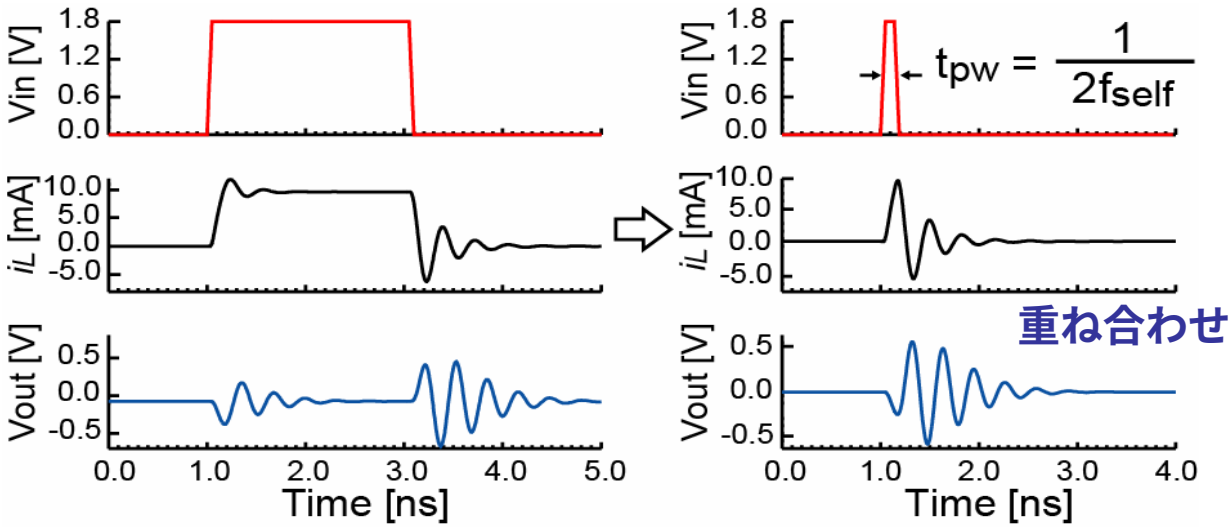
表　インダクタパラメータ

Ls	17nH	Csi	39fF
Cs	95fF	Rsi	920Ω
Rs	19Ω	k	0.11
Cox	180fF	—	—

低消電力データ転送の実現

共振現象を利用したインダクタ結合により低消費電力化



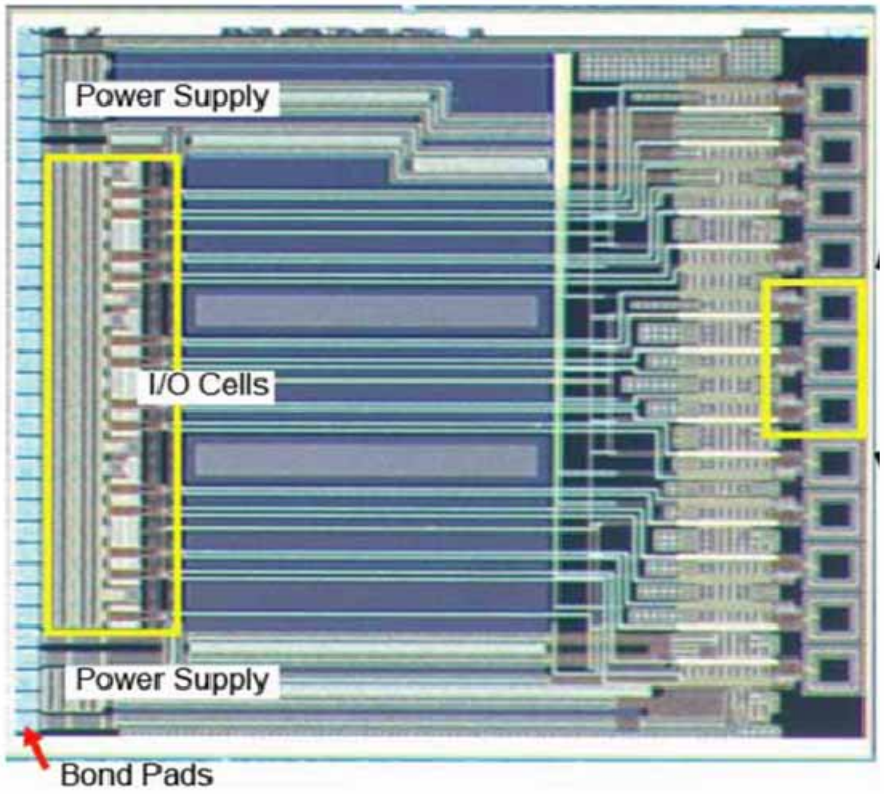


0.18um CMOS テクノロジ

パルス幅の下限：
100～150ps
自己共振周波数：
3.3～5.0GHz

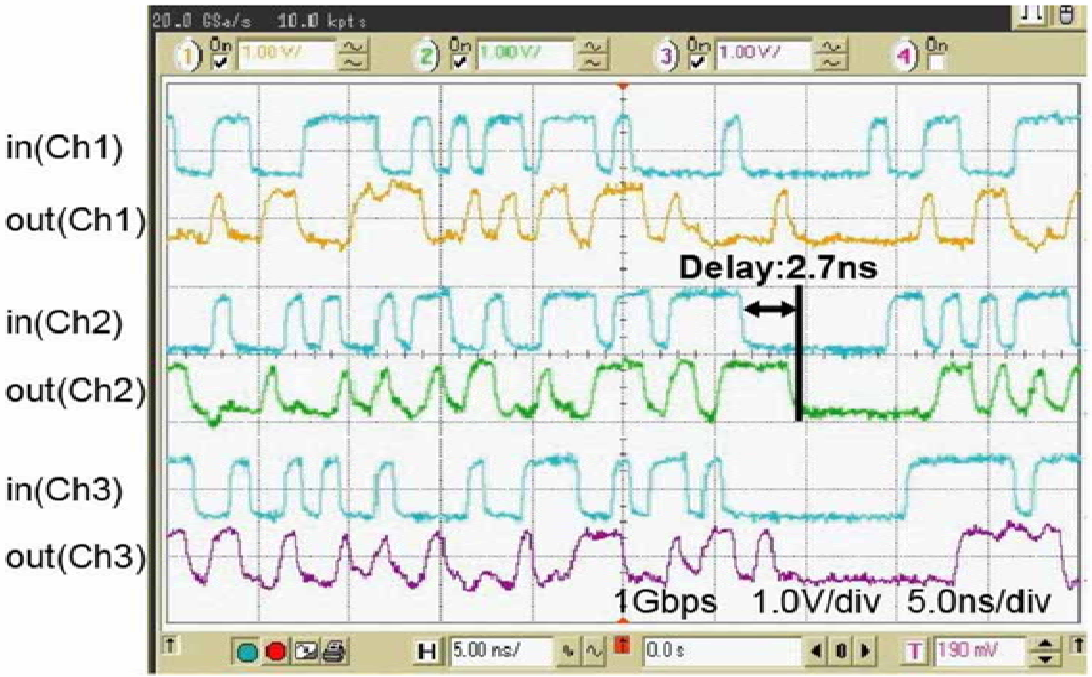
**自己共振周波数を
パルス幅に合わせる
そのため，共振周波数を
下げることが必要**

LWIテストチップ



ビットレート1Gbpsを0.84mWで実現

測定波形　誤り率10^{-10}



0.18um CMOS テクノロジ
MIM Cap　Metal : 6層
電源電圧 : 1.8V
インダクタサイズ :　200um x 200um
チップサイズ :　3.0mm × 3.0mm

国際会議発表:
Symposium on VLSI Circuits 2005

パッチアンテナを搭載した短距離無線回路

CMOS RF回路技術

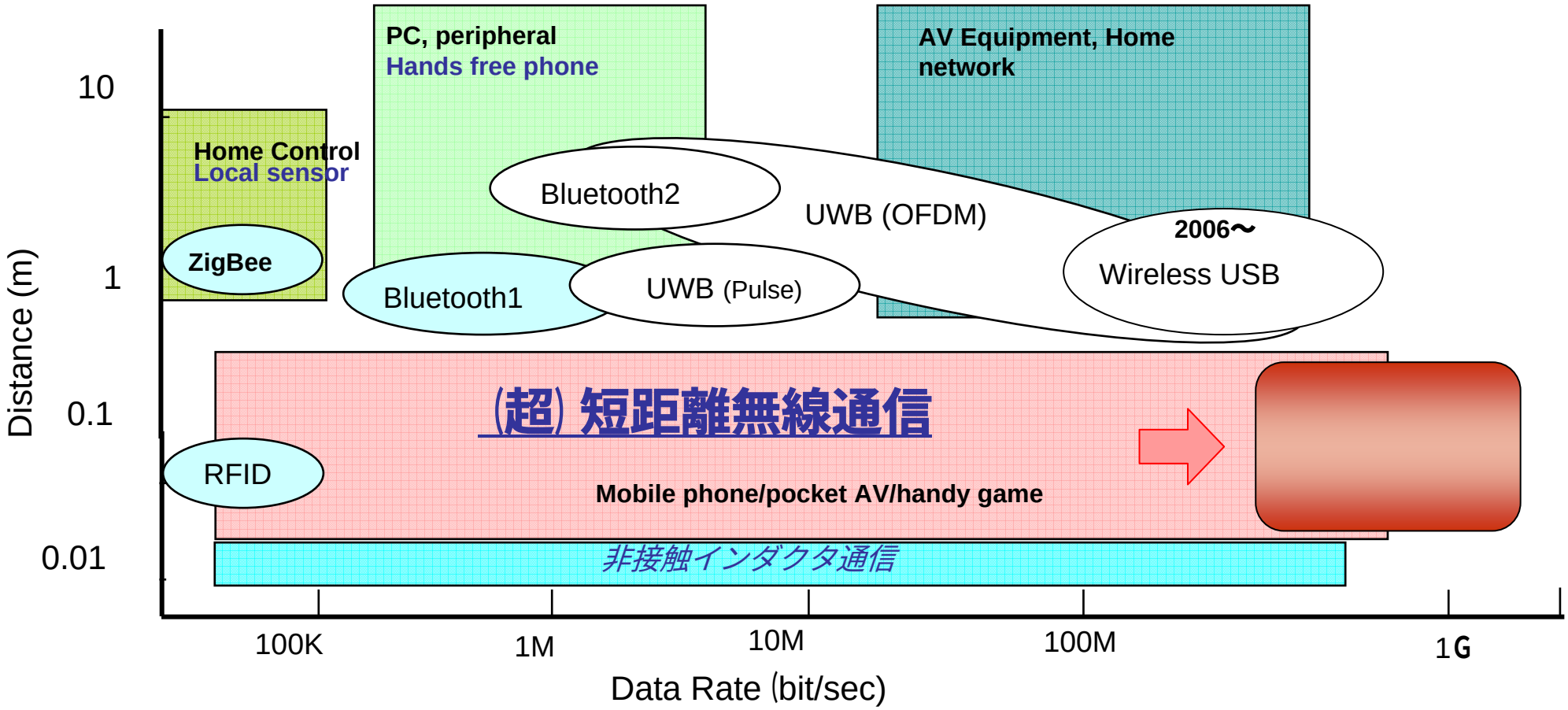
アーキテクチャの単純化

アンテナとICチップの一体化

微細CMOS ⇒ ミリ波帯

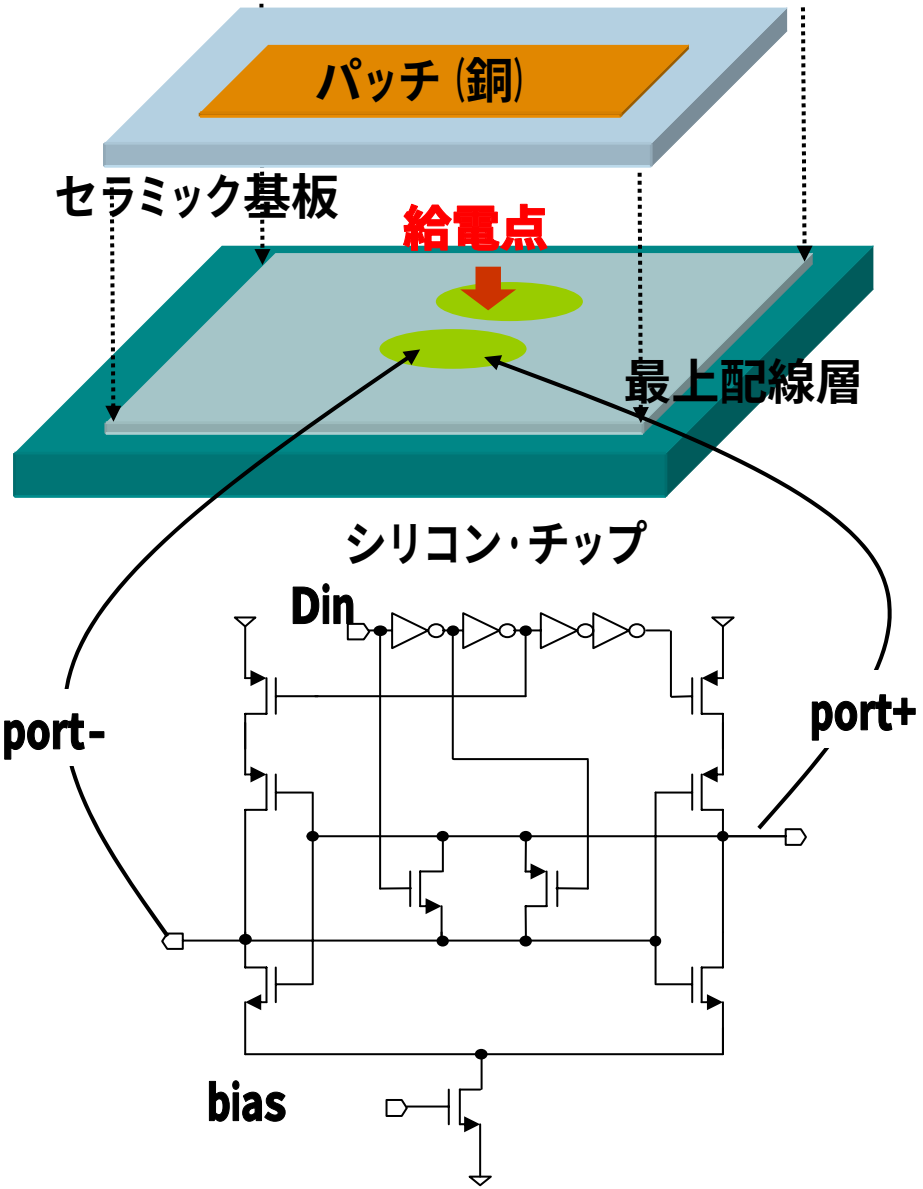
単一ブロックにRF機能の複合化

アンテナを積層化共振器として利用

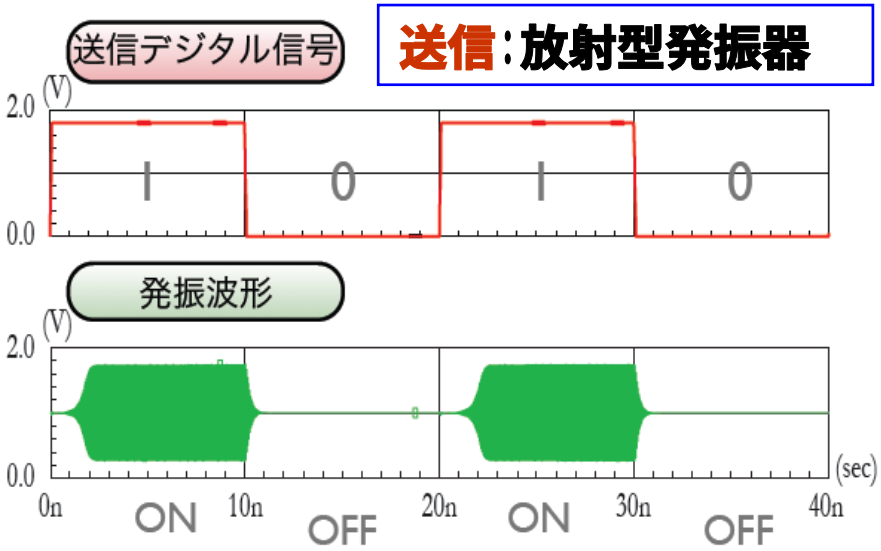


パッチアンテナを搭載した短距離無線回路

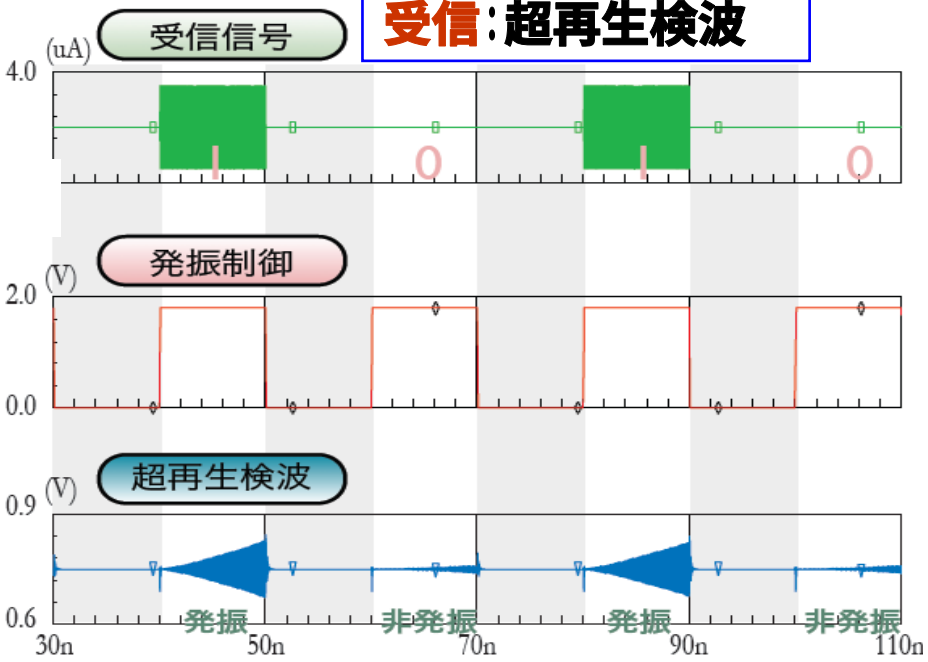
アンテナ＋発振器＋OOK



送信：放射型発振器

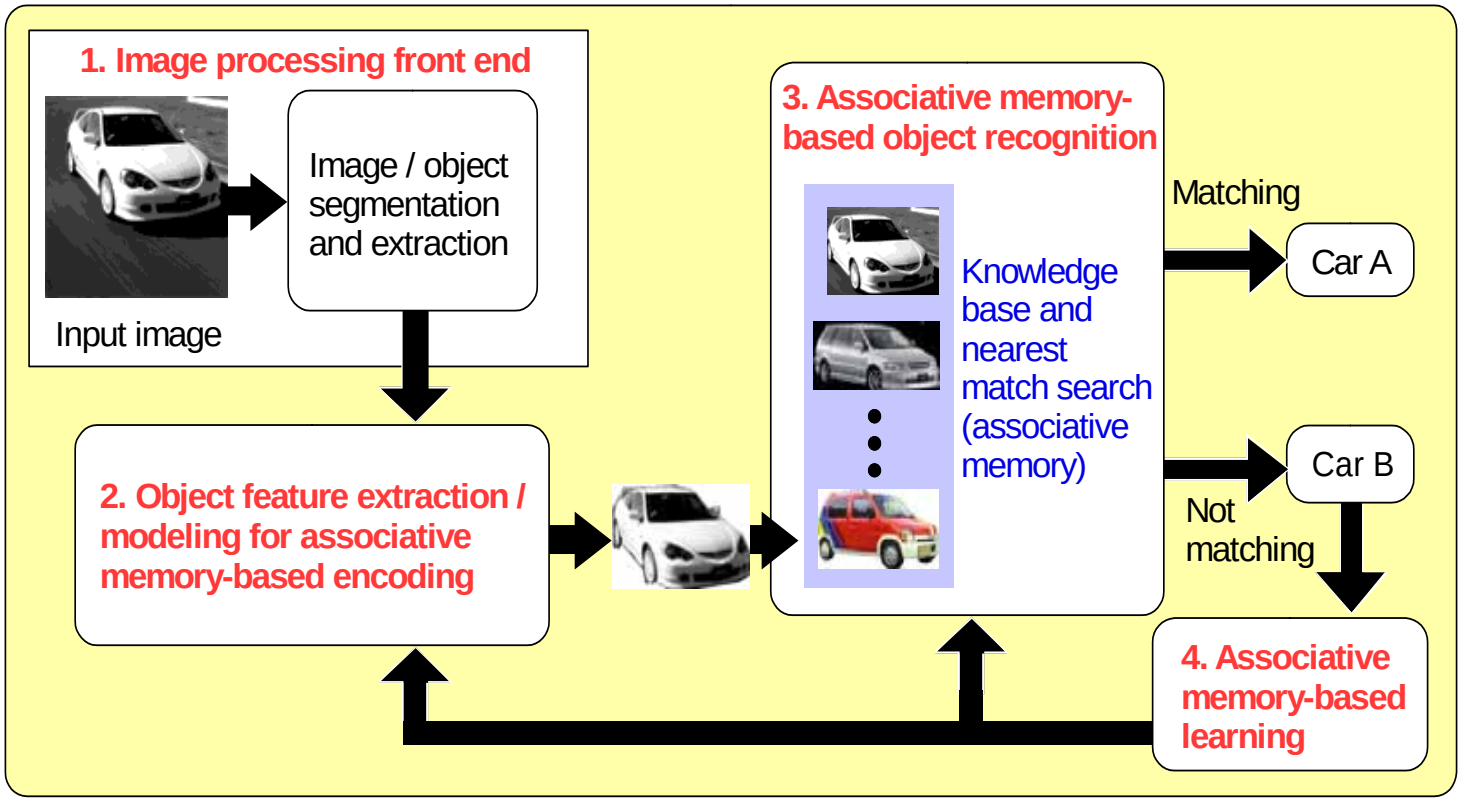


受信：超再生検波



連想メモリベース画像処理技術

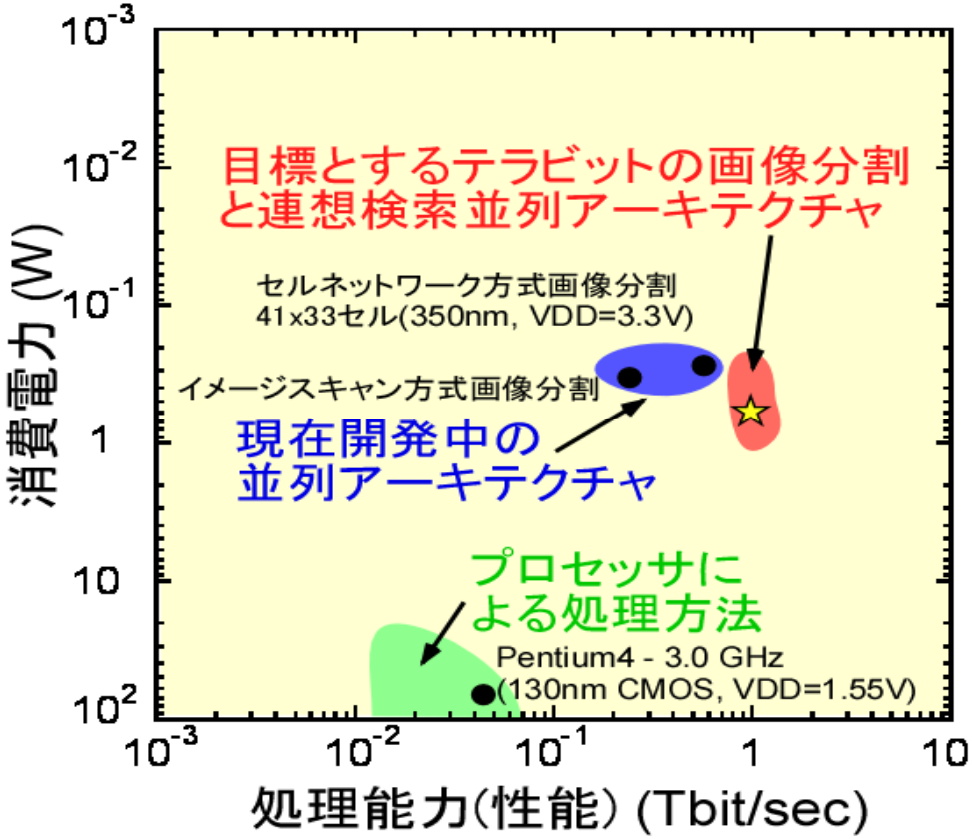
画像分割と連想検索に基づく
物体追跡チップアーキテクチャの開発



目標とする連想メモリベース画像処理システムの概念図

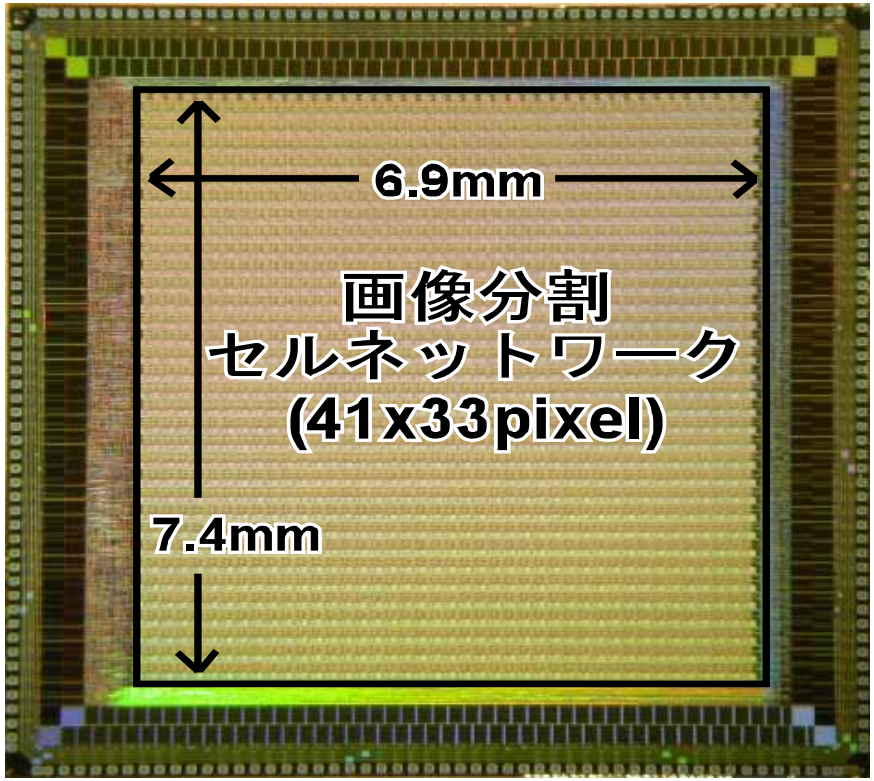
画像分割と連想検索の並列処理に基づく物体追跡チップアーキテクチャの開発

- チップ内テラビット処理（～1Tbit/sec)による リアルタイム画像分割処理チップアーキテクチャの開発
  （関連論文16件，特許登録/出願10件）
- 全並列最小距離検索連想メモリによるオブジェクトマッチング処理技術の開発
  （関連論文19件，特許登録/出願20件）
- 連想検索ベース複数物体追跡チップアーキテクチャの開発
  （国際会議発表予定1件，特許出願1件）
- 画像分割，特徴抽出，連想メモリベースオブジェクトマッチング等のFPGAによる原理検証とテストチップ試作（国際会議発表予定1件）

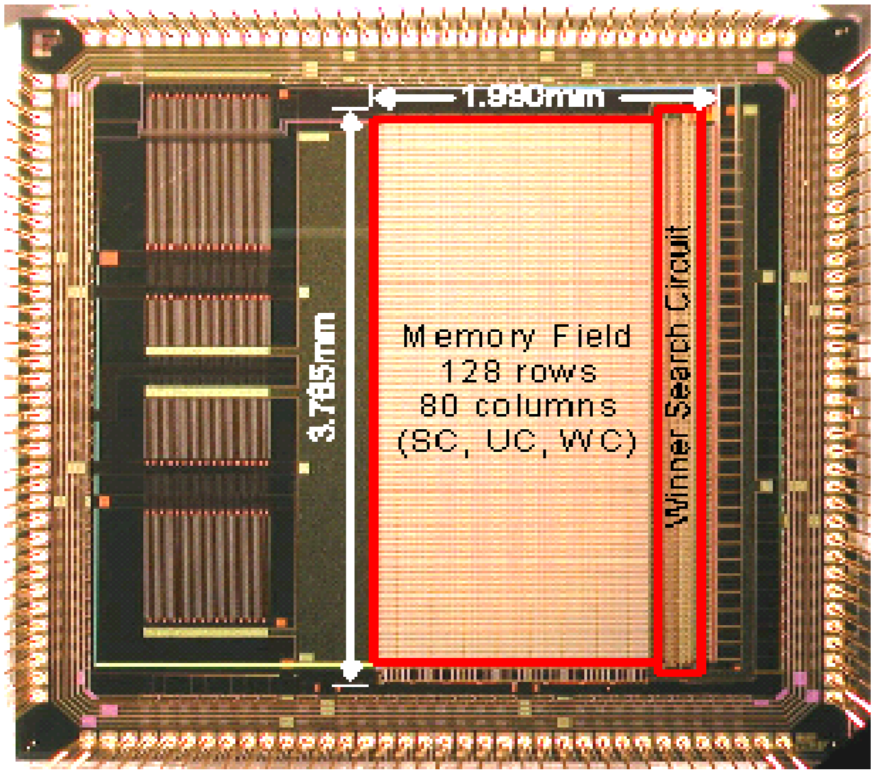


目標とするテラビットの画像処理性能

画像分割と連想メモリチップ

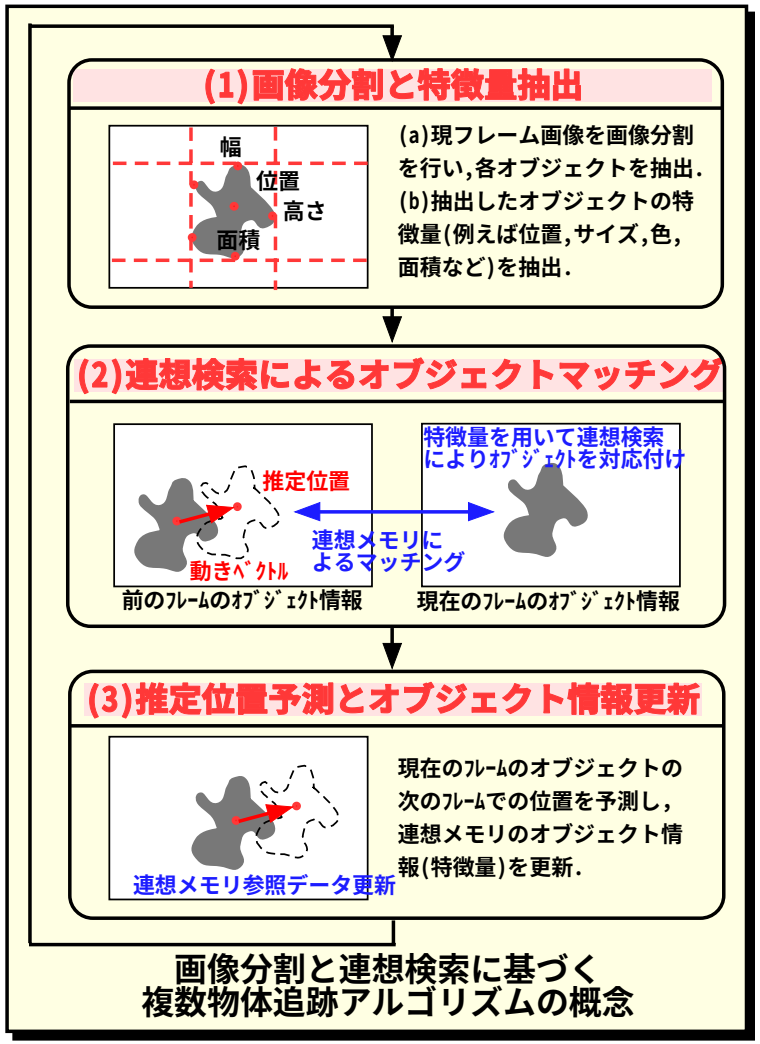


セルネットワークベース
画像分割チップ

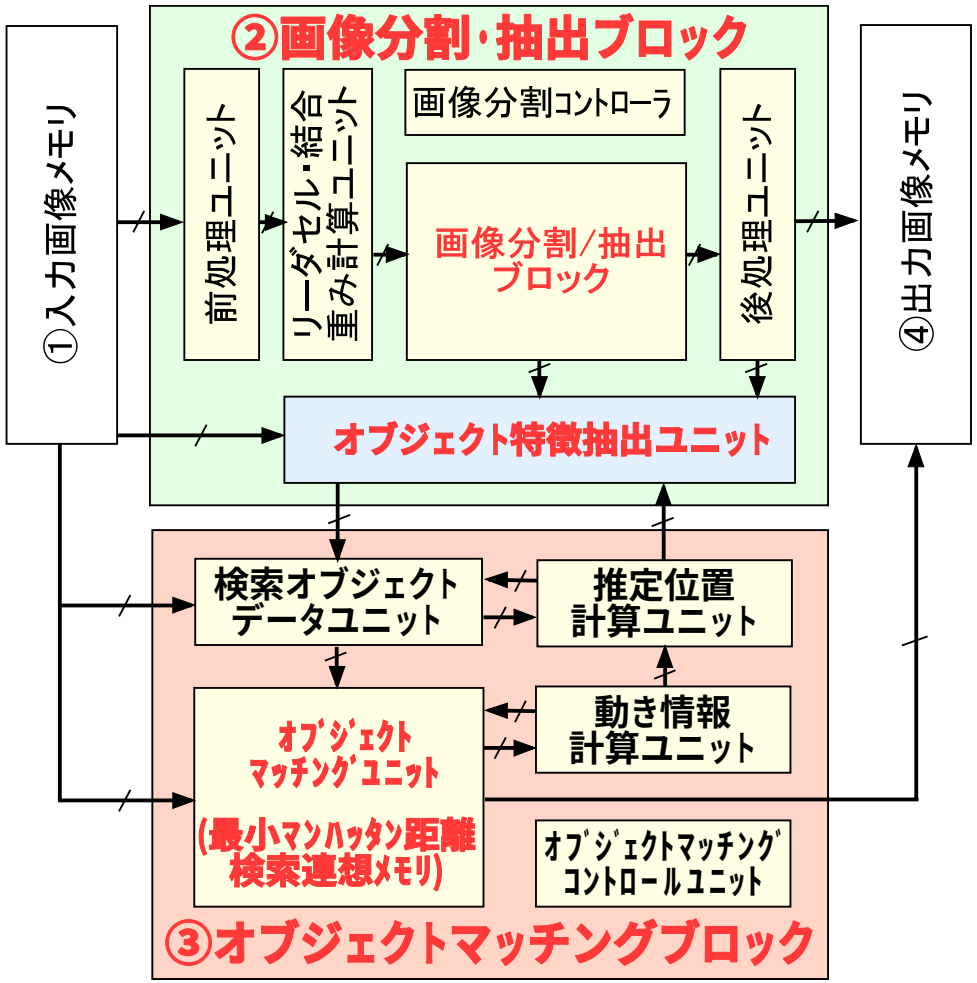


最小距離検索機能を有する
連想メモリチップ

画像分割と連想検索に基づくリアルタイム複数動物体追跡



画像分割と連想検索に基づく
複数物体追跡アルゴリズムの概念

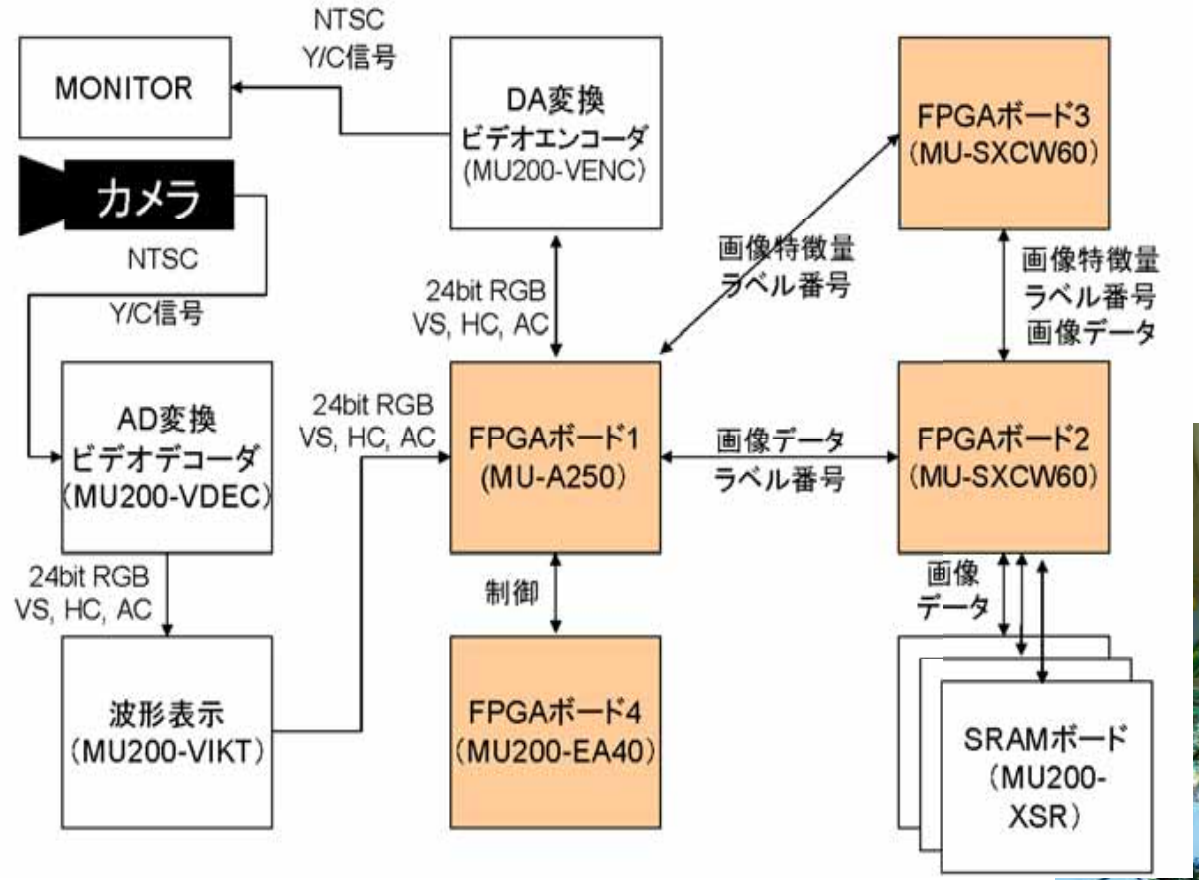


物体追跡アーキテクチャブロック図

特長
(ISCAS06, ASPDAC06 発表予定)

- 画像分割により**静止体，動体の両方**を同時に抽出
- 剛体のみでなく，**非剛体**，物体が重なる場合（**オクルージョン**）も追跡が可能
- 同時に**複数の物体**のリアルタイム追跡が可能
- 物体特徴量と最小距離検索を用いているため，画像認識への応用が可能

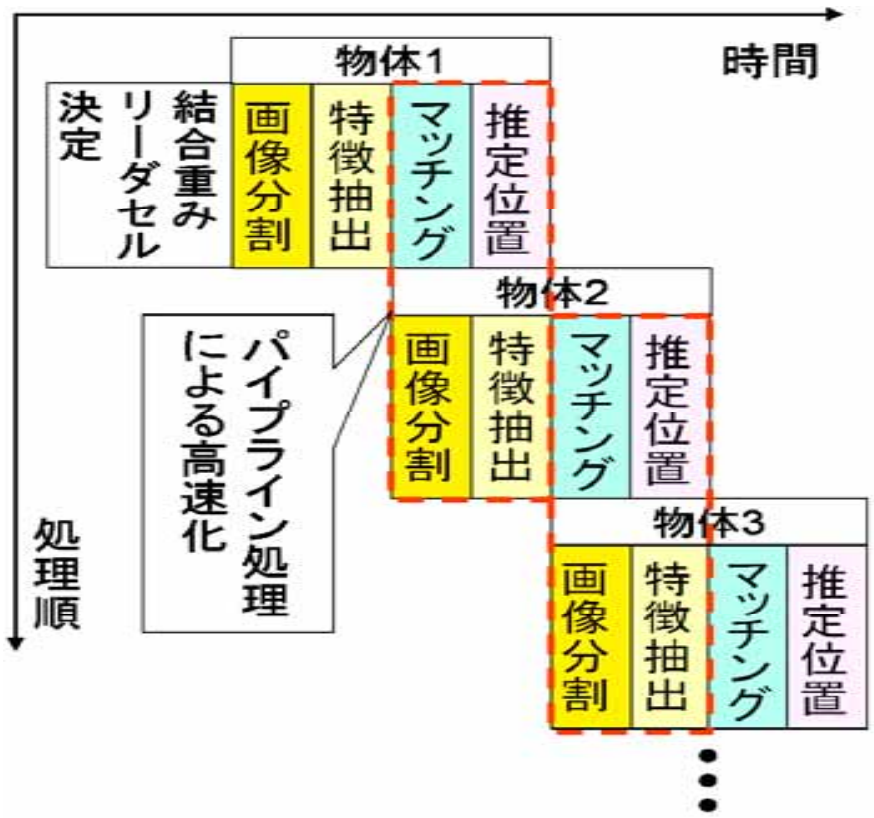
リアルタイム複数動物体追跡プロトタイプシステム

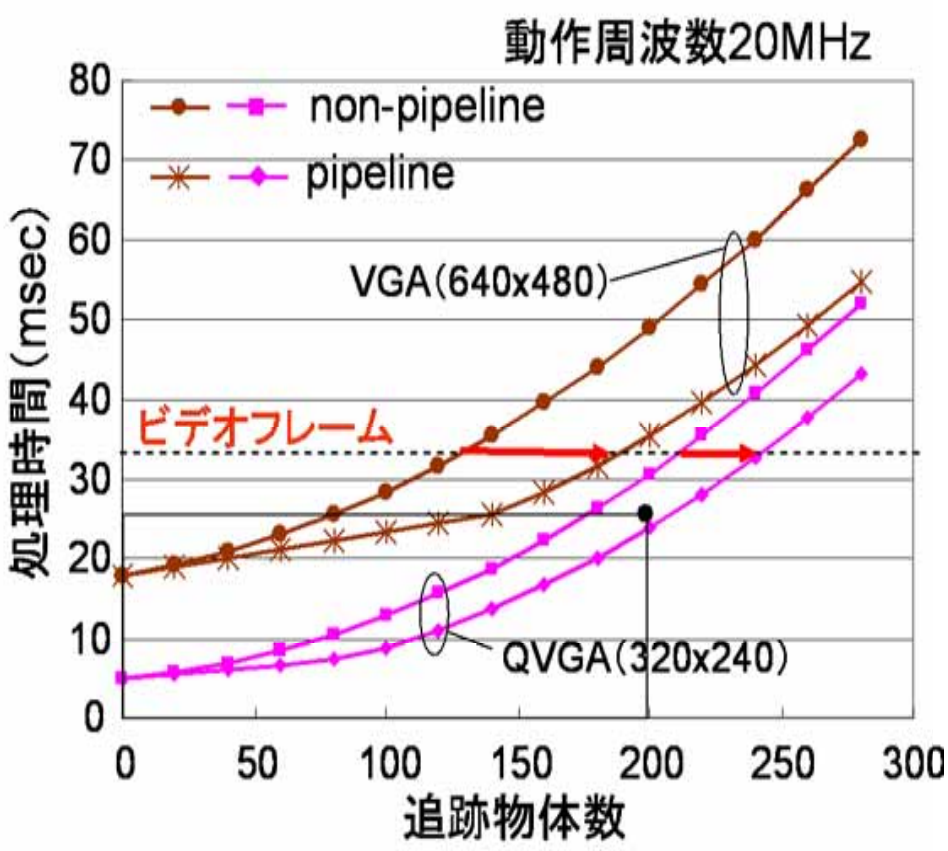


ブロック図

外観

複数動物体追跡システムの高速化





パイプライン処理による高速化

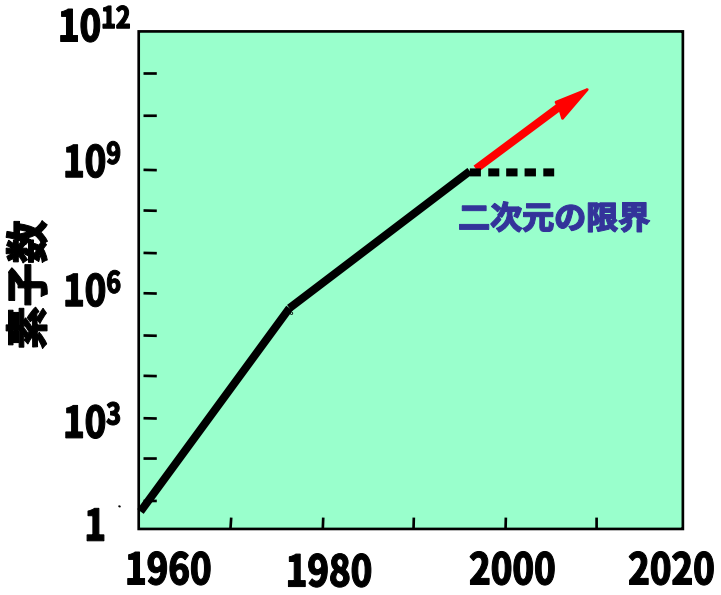
マッチング処理と画像分割処理を時間的にオーバーラップさせることで処理時間を削減可能

・25msec/frame
QVGA　：215物体

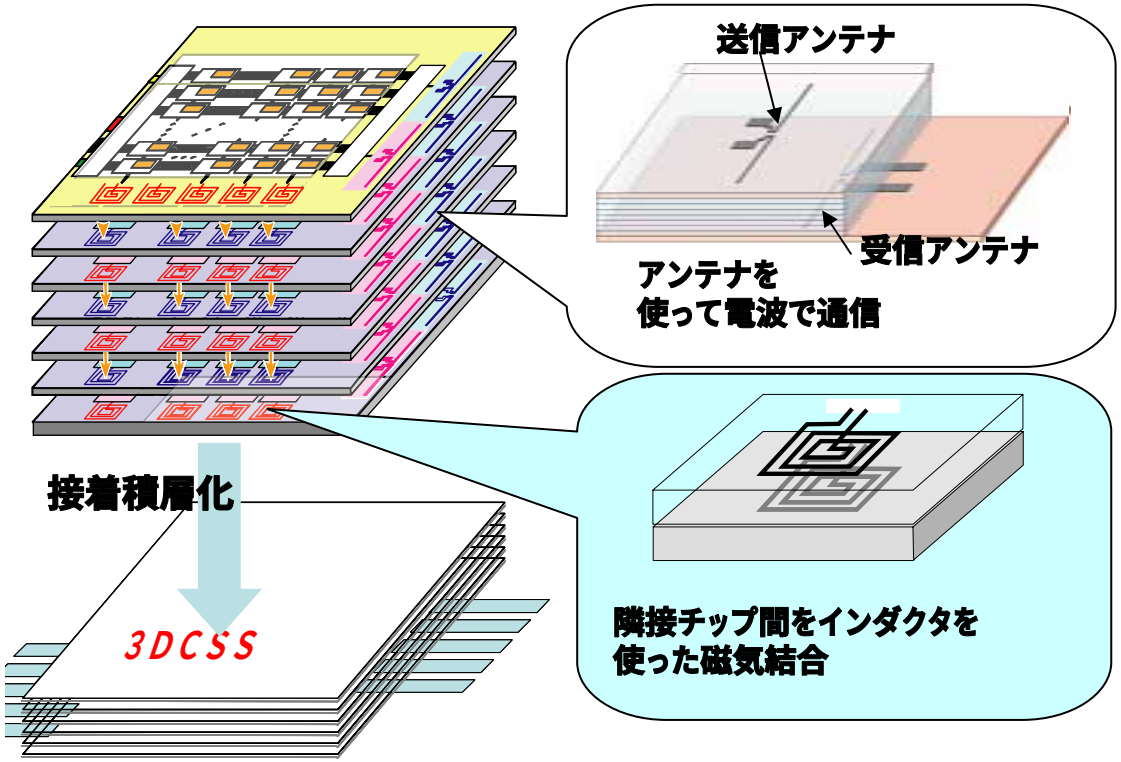
・33msec/frame (ﾋﾞﾃﾞｵﾌﾚｰﾑ)
QVGA　：240物体
VGA　：180物体

無線インタコネクト三次元集積技術

ムーアの法則を破る
三次元集積



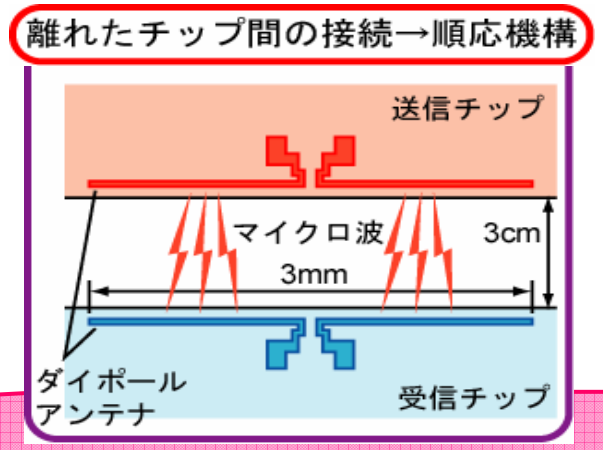
3DCSS：
三次元カスタムスタックシステム

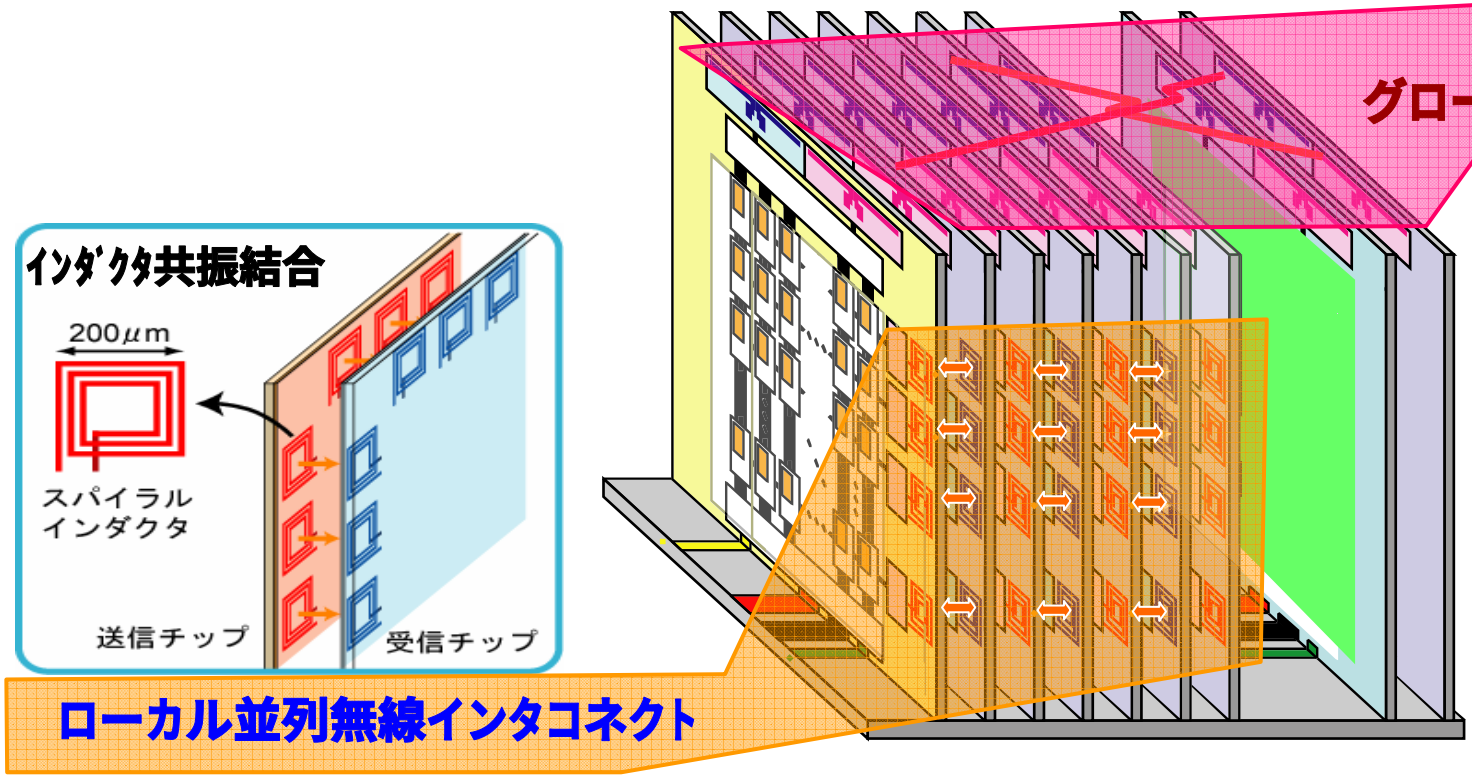


無線インタコネクト三次元集積システム

3DCSS：三次元ｶｽﾀﾑｽﾀｯｸｼｽﾃﾑ

異種機能のマルチチップ
チップ間の情報通信が最大の課題

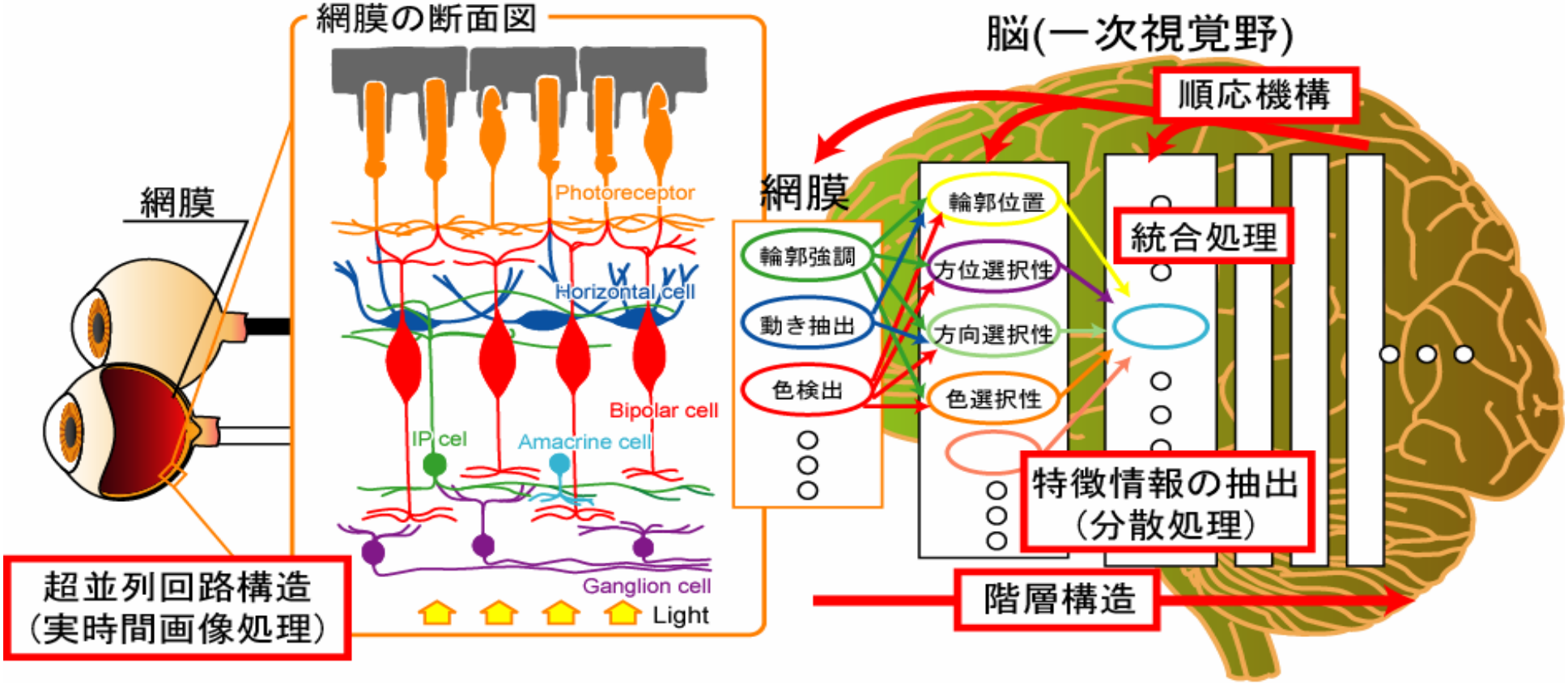




電磁波妨害の対処

電波吸収体の集積化

三次元集積で実現を目指す人間の視覚システム

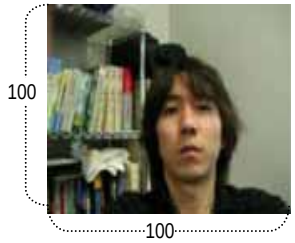


・超並列・階層構造により、特徴抽出や統合処理を実時間処理
・時々刻々変化する視覚環境に順応する

↓

生体視覚系の構造・機能を工学的に実現 → 3次元集積
人間より高速なハイパーブレインを実現

マルチオブジェクト認識3DCSSにおけるデータ転送

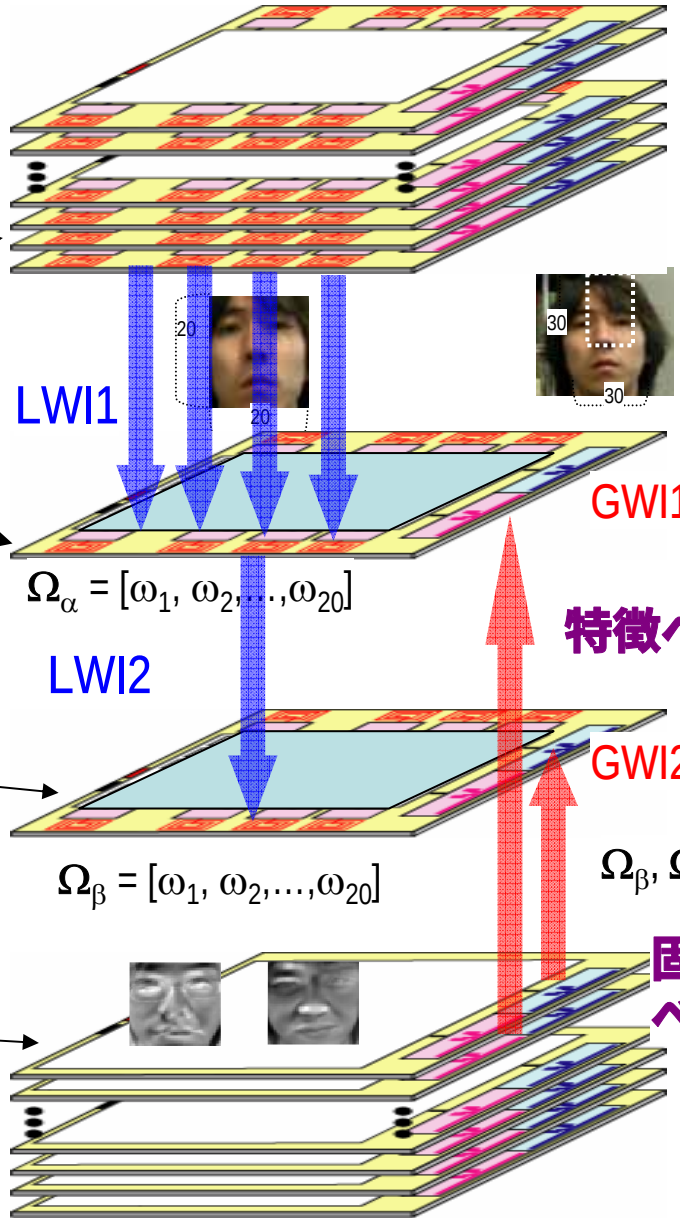


VP3D
初期視覚処理

OR3D
ｵﾌﾞｼﾞｪｸﾄ検出

OR3D
ｵﾌﾞｼﾞｪｸﾄ認識

DB 3D
参照メモリ



LWI： **アナログ情報並列転送**
GWI： **非隣接チップ間**
データバス転送
制御コマンド転送

DB参照数100，
入力物体100の場合

データ転送レート

LWI1	：6.4G bps
LWI2	：44M bps
GWI1	：1.12G bps
GWI2	：4.4G bps

三次元集積アーキテクチャ

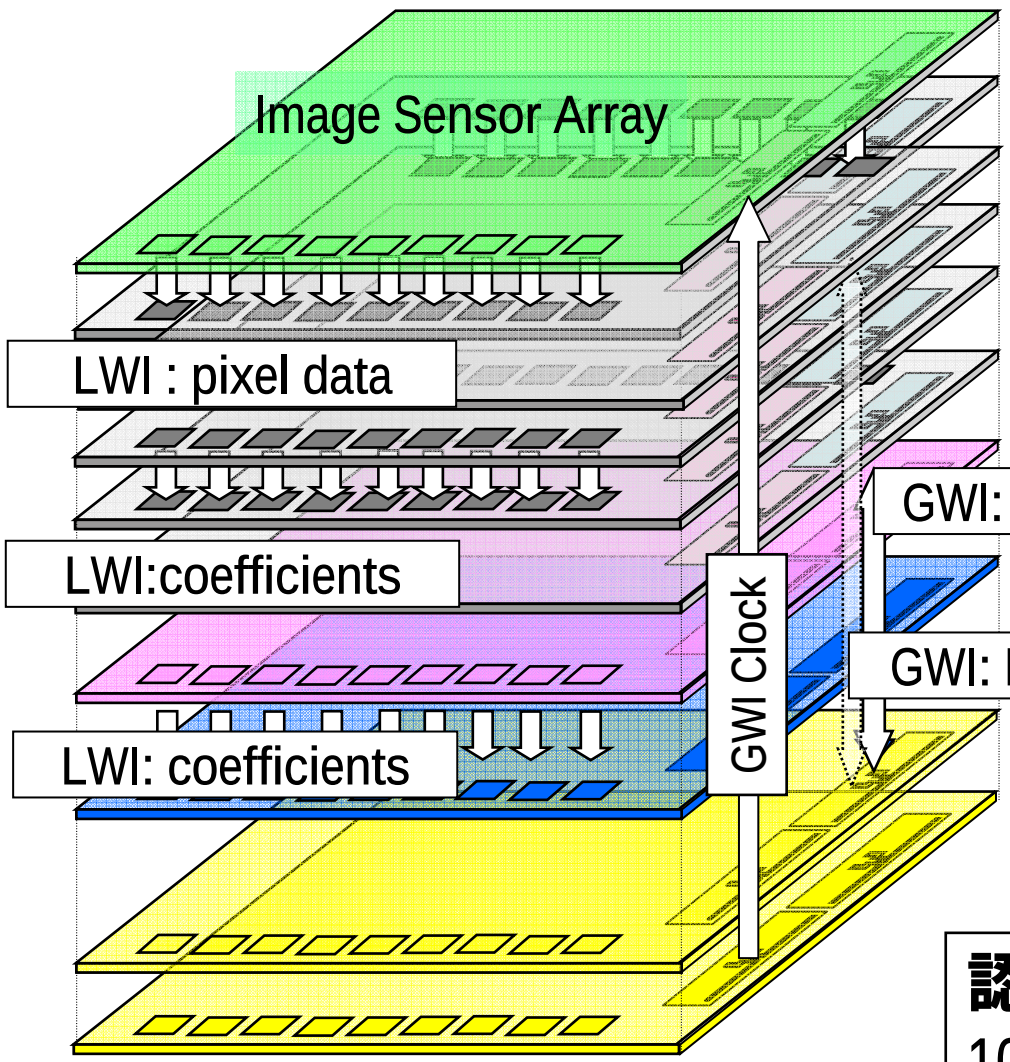


Image Sensing & Filtering
(Smoothing, LoG, etc)

Object Detection

Feature Analysis by PCA

GWI: Feature Vectors

Object Recognition

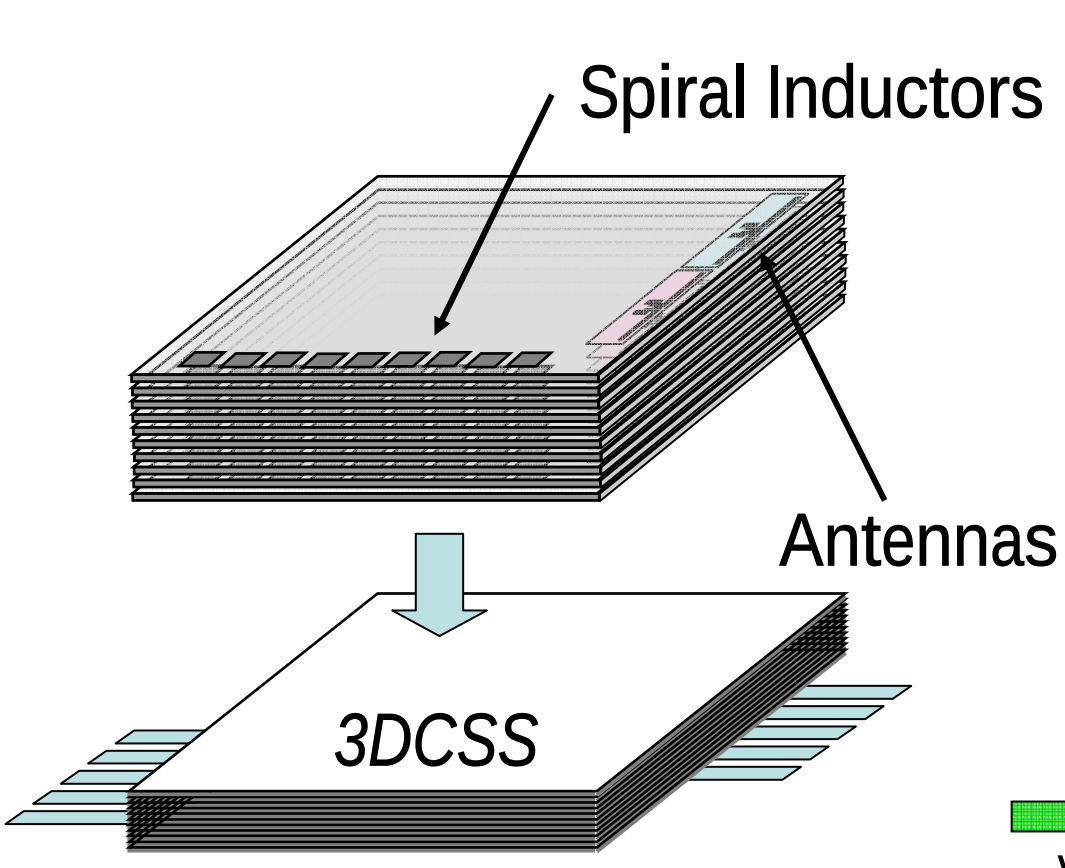
GWI: Reference Vectors

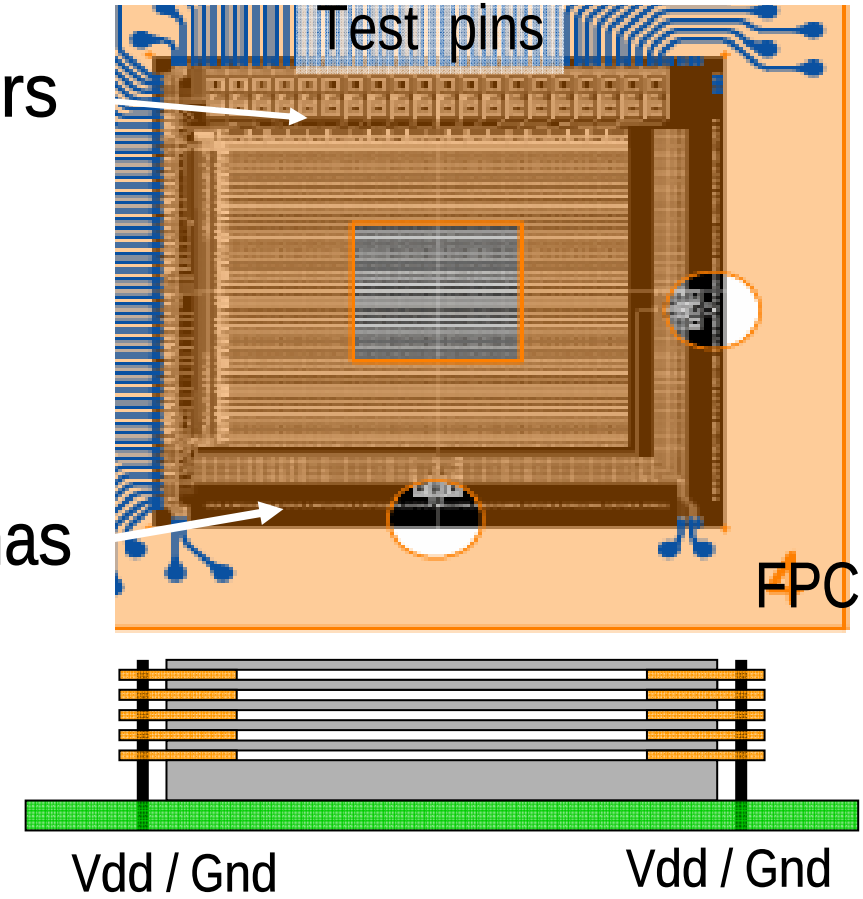
Reference Data Base
(Associative Memory)

認識性能 (simulation)
10 frames/s, 10 objects/ scene,
1000 individuals/object

国際会議発表　ISSCC2005

3DCSS Prototype with LWI and GWI





Features

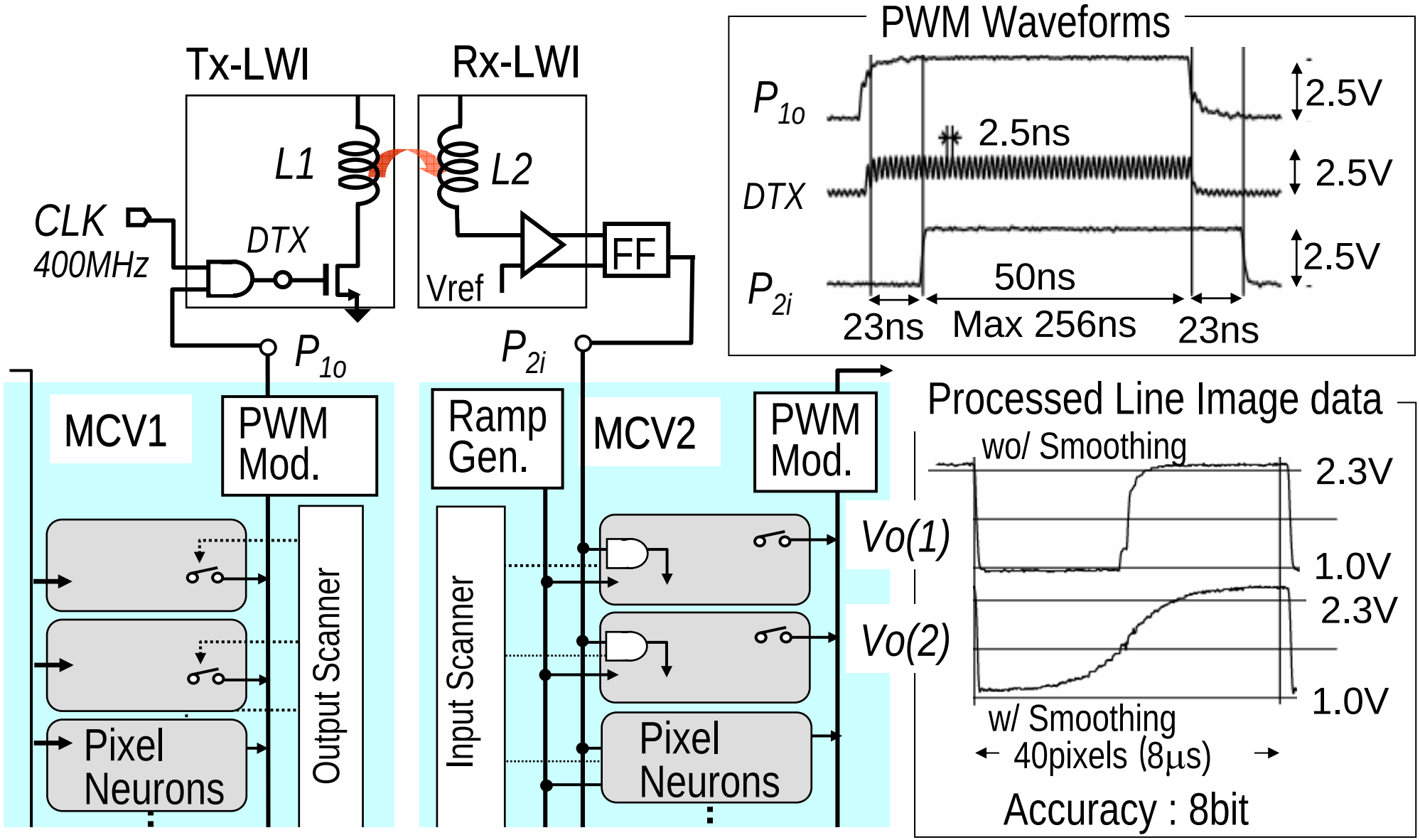
1. Improve Reliability and Yield
2. Resolve problems in KGD and heat radiation

Parameters

L_{ant}= 2-4 mm, L_{ind}= 50 - 200μm
No. of Chips= 10-100
t_{chip}= 50 -100μm

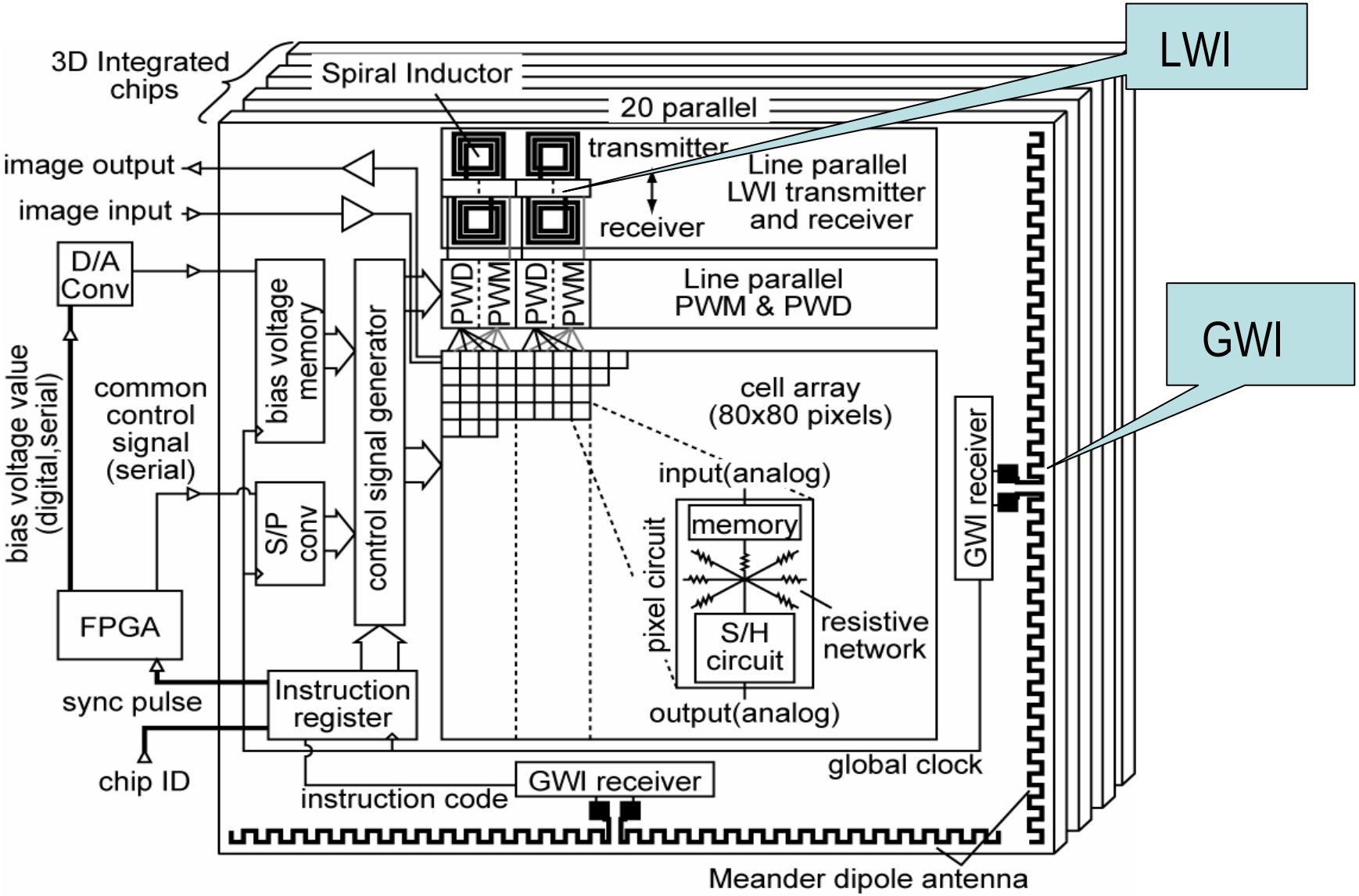
三次元集積プロトタイプの試作評価

LWIを用いたマルチチップビジョンの実験



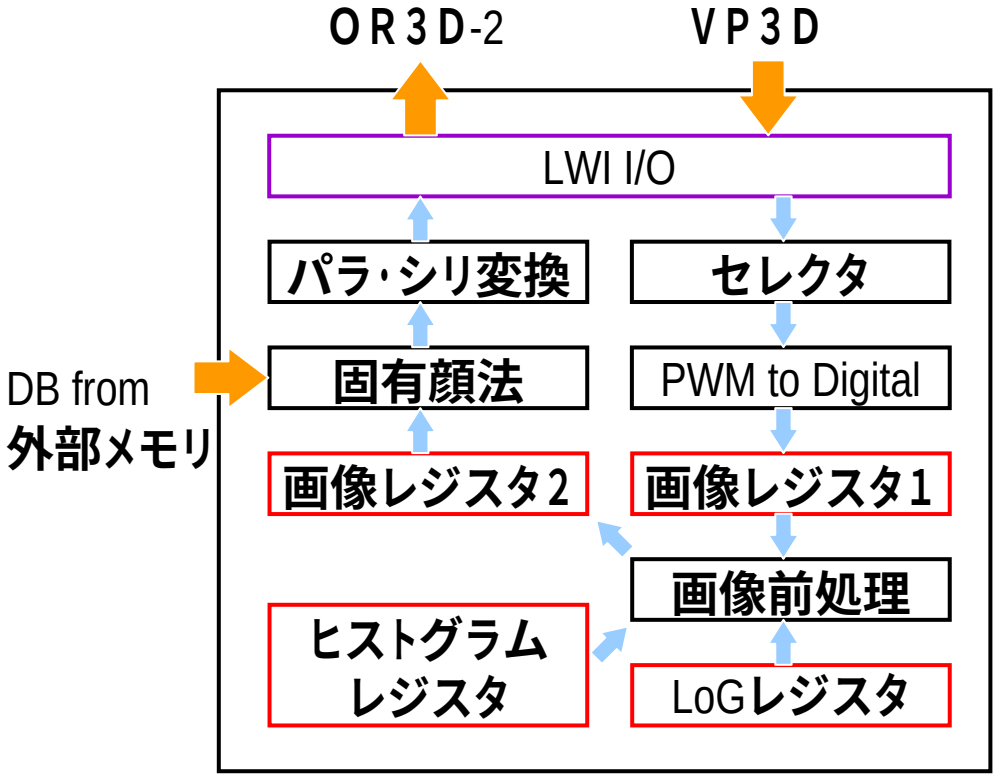
国際会議発表　ISSCC2005

三次元集積による画像処理チップ（ＶＰ３Ｄ）



三次元集積による画像処理チップ (OR3D)

オブジェクト検出，認識チップ OR3D



仕様

画素サイズ	32x32
画素データ	8bit グレイスケール
画像データ入力	LWIもしくはカメラ
画像前処理	ヒストグラム平坦化
	LoG (5x5)
	ヒストグラム調整
認識アルゴリズム	固有顔法
処理速度	100ms以下
	1:100認証で
データベース	オフチップ

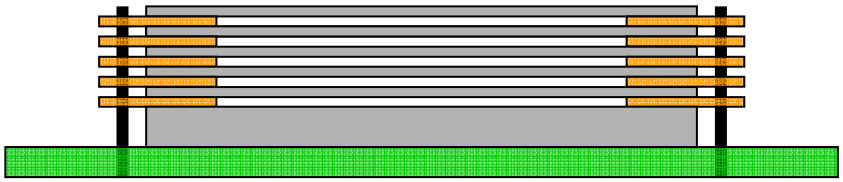
基本処理

①画像データ入力
②PWM to Digital変換(PDC)
③画像前処理
④固有顔法
⑤認識結果出力

メモリサイズ

画像レジスタ1 & 2	: 8bit, 32x32 words
ヒストグラムレジスタ	: 6bit, 256 words
LoGレジスタ	: 12bit, 5x5 words

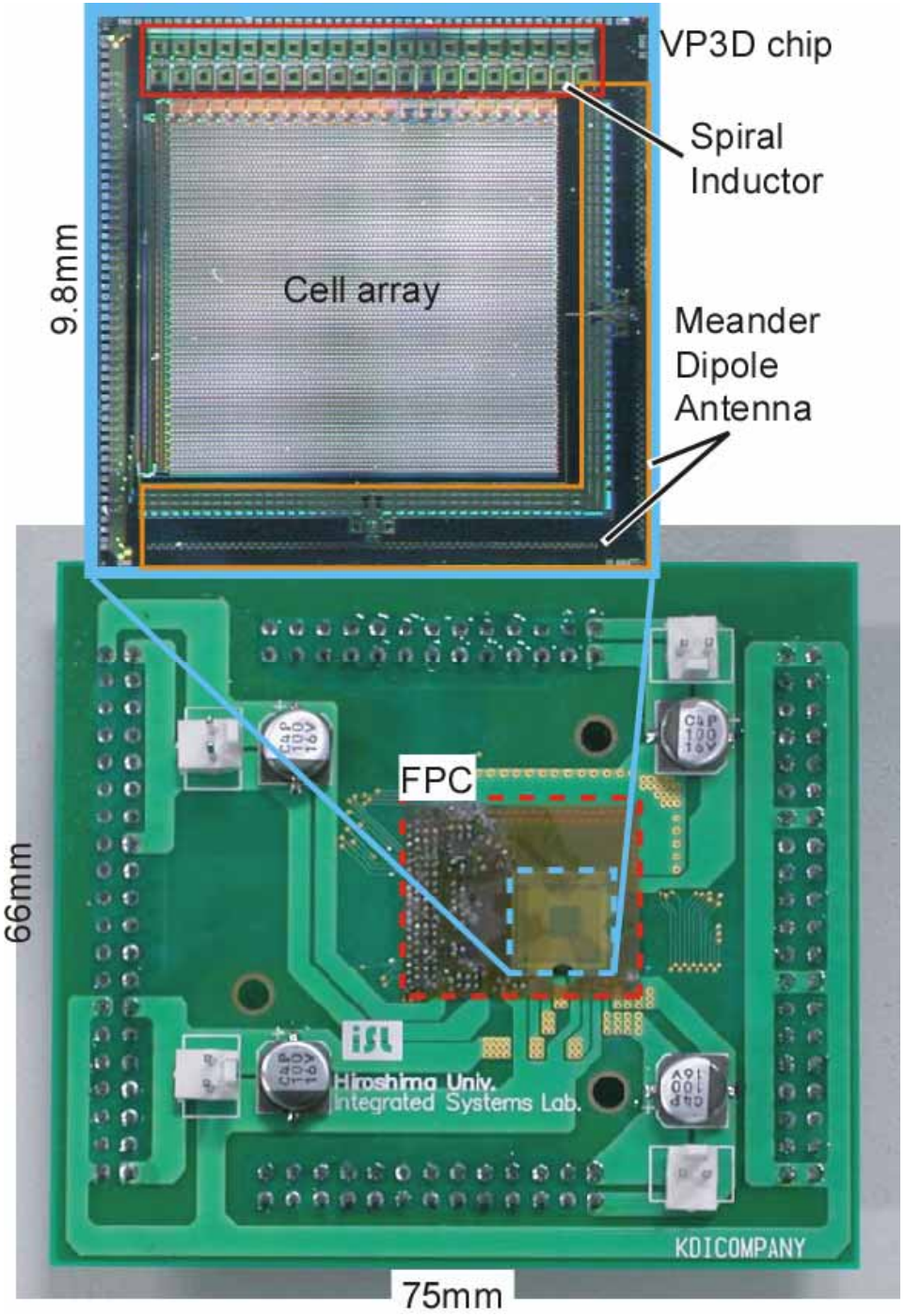
3DCSSプロトタイプ
画像処理システム



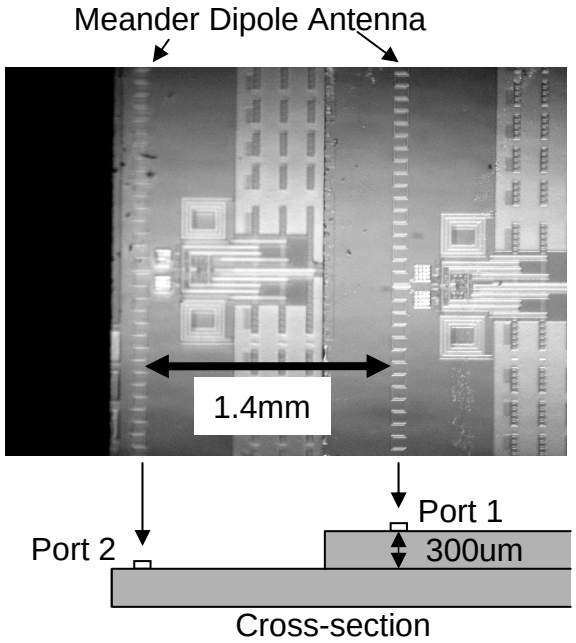
Parameters

Lant= 2-4 mm, Lind= 50 - 200μm
No. of Chips= 10-100
tchip= 50 -100μm

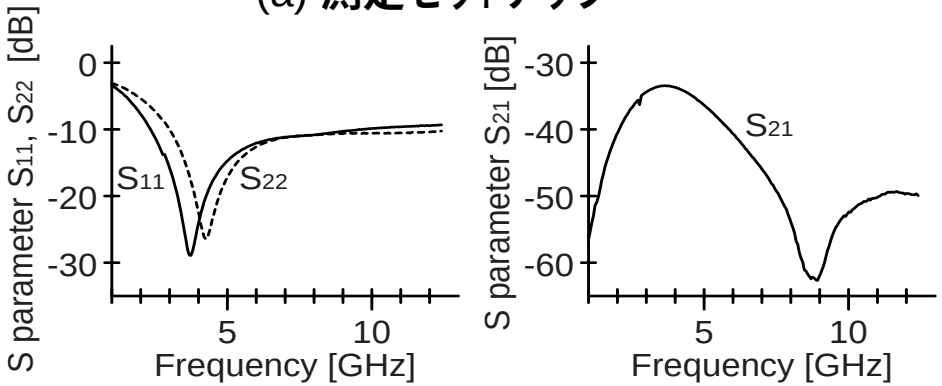
国際会議投稿予定



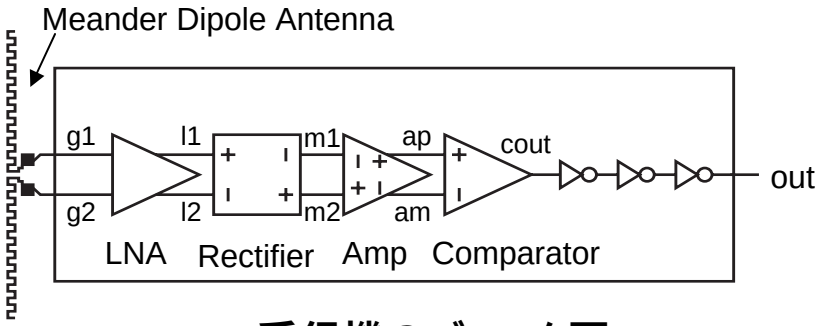
グローバル無線インタコネクト (GWI)テストチップ



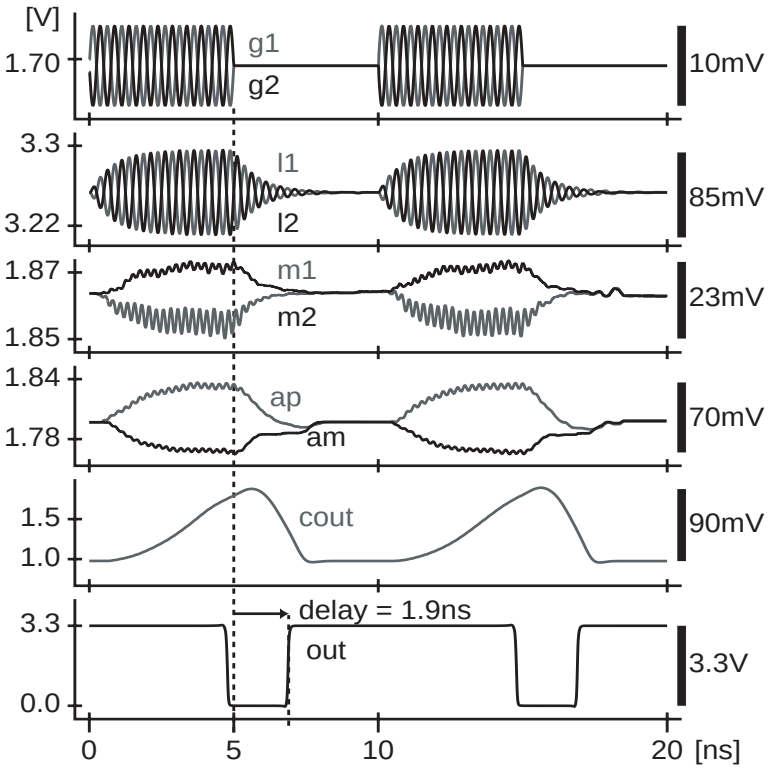
(a) **測定セットアップ**



(b) **ダイポールアンテナの実測特性**



(c) GWI **受信機のブロック図**



(d) GWI **受信波形**

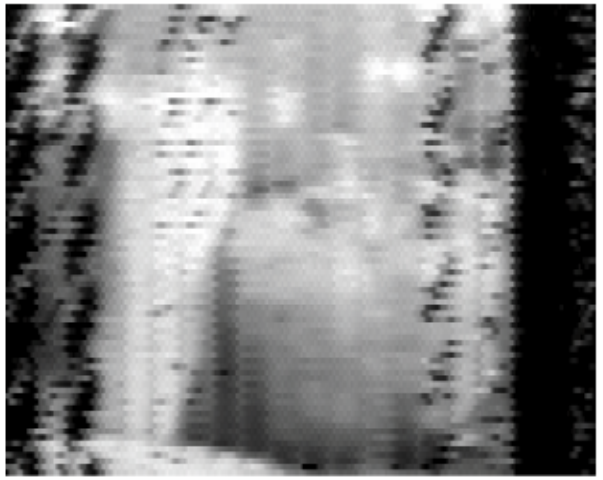
三次元集積技術 (3DCSS) で画像処理に成功

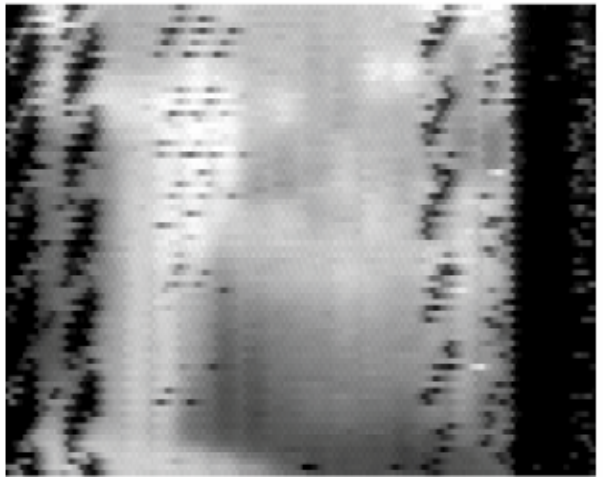
入力画像

80 x 80 pixels
Hexagonal grid

送信側画像

受信側画像





スムージングなし

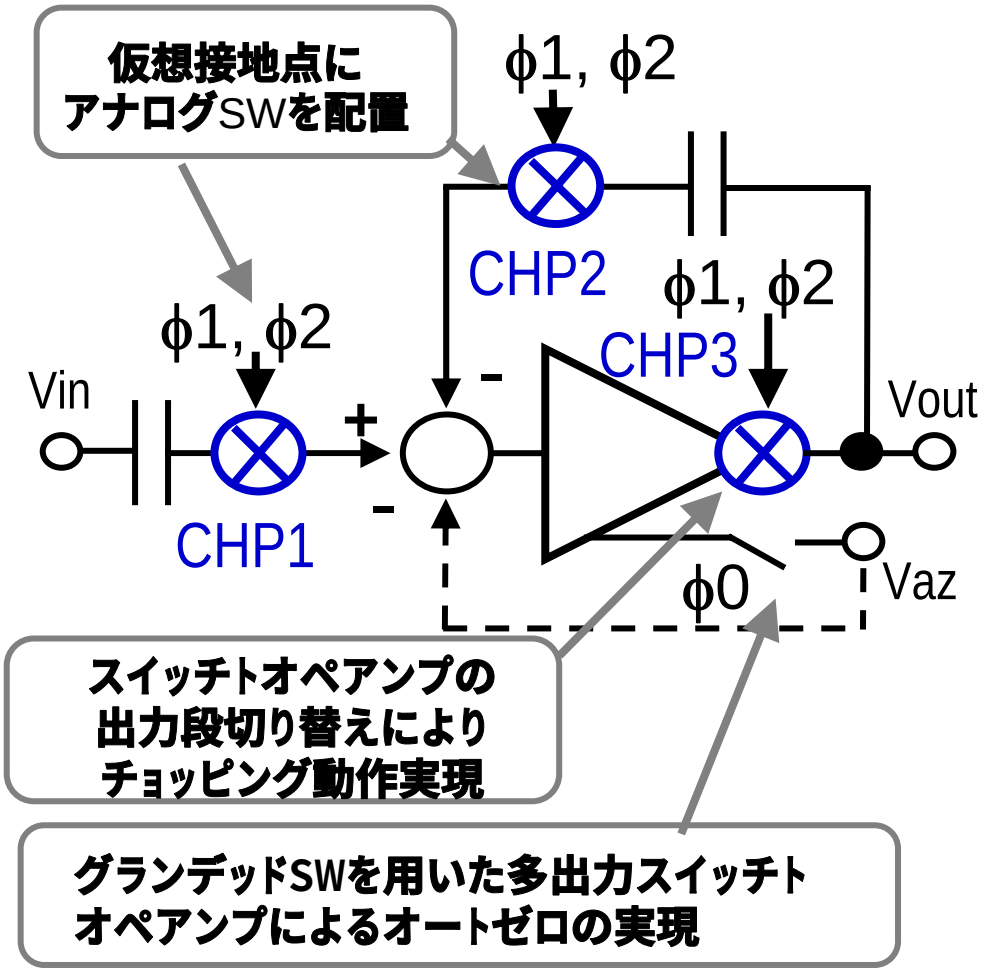
スムージングあり

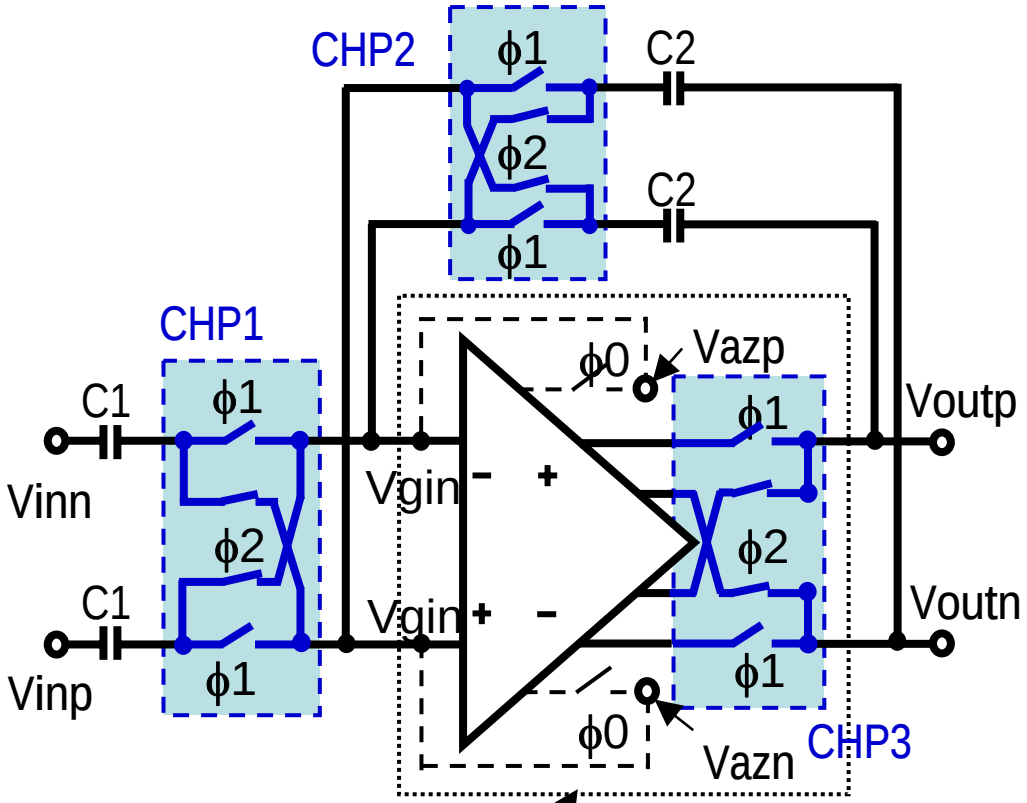
国際会議投稿予定

低電圧動作・低雑音増幅回路

特性：　1V電源動作・50nV低雑音特性

考案技術：グランデッドスイッチによるチョッパ，オートゼロの考案





全差動4出力スイッチトオペアンプ

国際会議発表：Symposium on VLSI Circuits 2005

新構造トランジスタと集積化技術

処理能力向上: デバイスの高速化

→ 周波数特性向上

→ 面積当たりの駆動電流, I_{drive} 増大

多様化する高速･低消費電力デバイス

→ 微細プロセスコア技術

テラ情報処理のための新構造トランジスタ

(1)集積デバイス基盤技術

・デュアルメタルゲート
　仕事関数制御
・極浅ソース･ドレインによる
　短チャネル効果抑制

・原子層成長high-k絶縁膜と
　原子層成長Si窒化膜の
　スタック構造のゲート絶縁膜

(2)三次元立体ＭＯＳデバイス

・小面積でゲート幅Wを拡大て，
　面積当たりの電流増大
　電力制御回路に適用

しきい値制御

減小抑制

$$I_{drive} \propto \frac{\varepsilon \quad \mu \quad W}{t \quad L}$$

増大

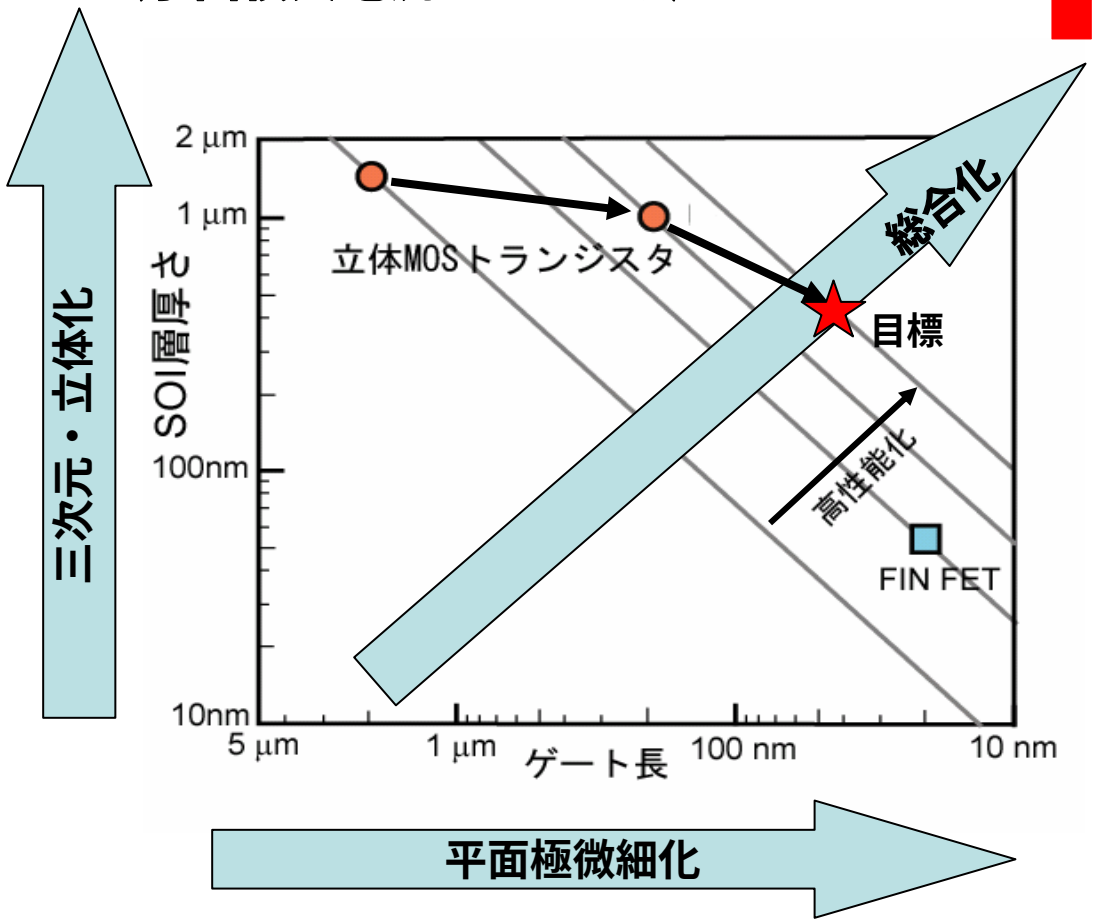
増大：10倍以上

μ ： キャリヤ易動度
ε ： ゲート絶縁膜厚誘電率
W ： ゲート幅
L ： ゲート長
t ： ゲート絶縁膜厚

デバイス･プロセス研究課題の相互関連

■立体ＭＯＳトランジスタ
(小面積大電流トランジスタ)

■無線あるいは光による三次元配線
■モデリングによる性能予測
■量子ドット立体集積構造
(多値不揮発性メモリ
超高感度光検出器など)



■ ALD high-kゲート絶縁膜
■ ALD窒化ゲート絶縁膜
■デュアルメタルゲート
■極浅ソース・ドレイン
■直接パターニングLow-k膜

新構造デバイス・微細化基盤技術

1.三次元　ビームチャネルトランジスタ (Beam Channel Transistor)
- with high current driving capability

aiming at applications to power control with small chip area.

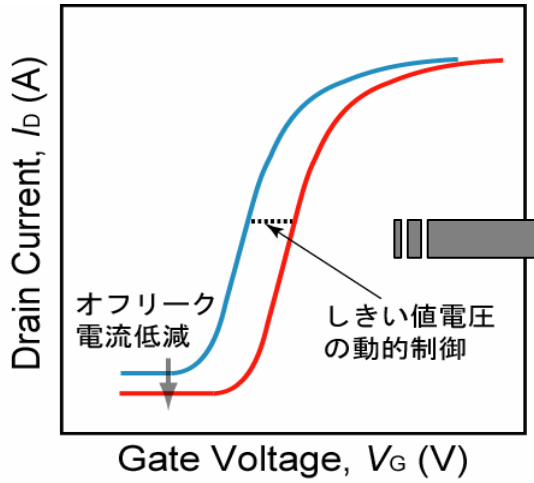
2. 仕事関数制御 NiSi ゲート MOSデバイス
- NiSi workfunction tuning method by Sb pre-doping to poly-Si before silicidation

3. High-k 絶縁膜形成 原子層成長(ＡＬＤ)技術
- Si-nitride/SiO2 stack gate dielectrics for future scaled DRAMs.
- Enhanced reliability in NBTI was achieved.

立体3並列ゲートトランジスタの提案

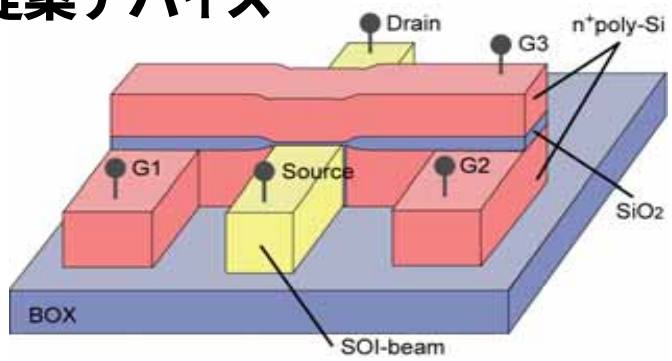
VLSI回路における
消費電力の問題

個々のデバイス特性制御
による最適化の重要性



しきい値電圧の動的
制御による待機電力
低減効果

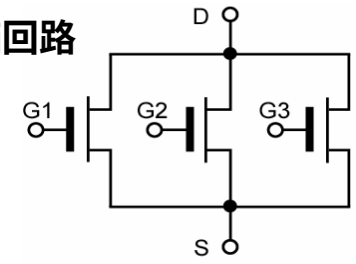
提案デバイス



SOIビームに独立した三つ
のゲート電極を形成

各ゲートに独立に電圧を印可

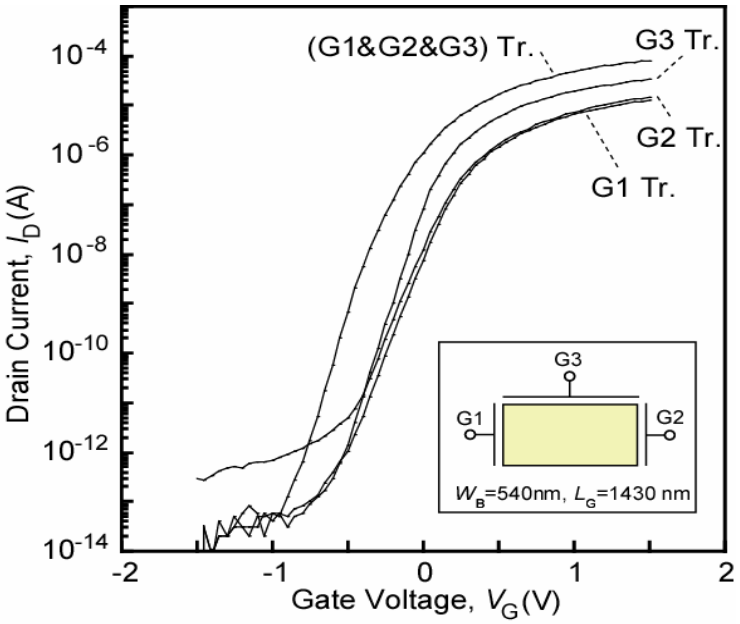
等価回路



○ 単一MOSFET → 基板バイアスによる
デバイス特性の動的制御

○三並列MOSFET → 回路面積の縮小

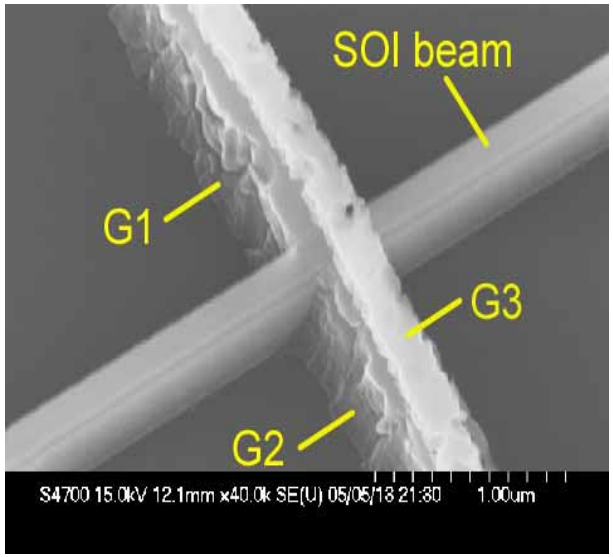
立体3並列ゲートトランジスタの試作に成功



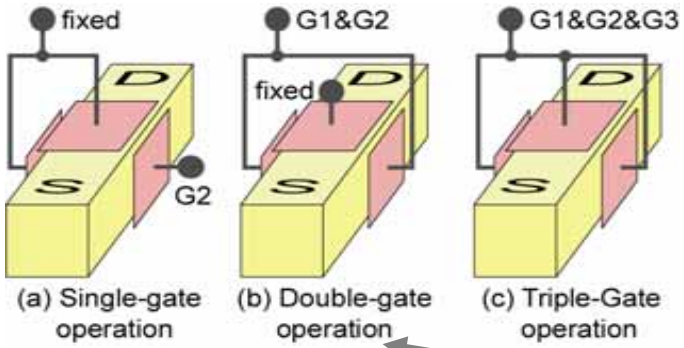
各ゲートによる電流制御動作を確認

(※非動作ゲートの印可電圧を-1Vに固定)

試作デバイスのSEM像



独立ゲートにより実現される三つの動作モード

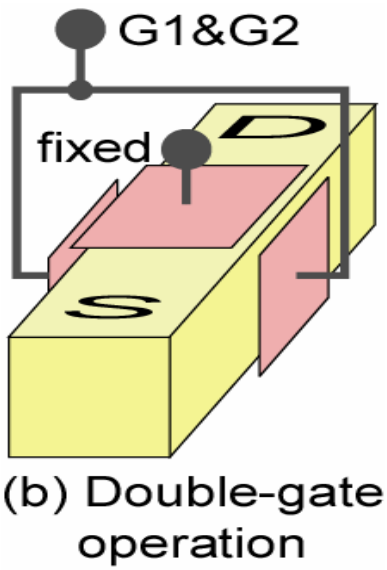


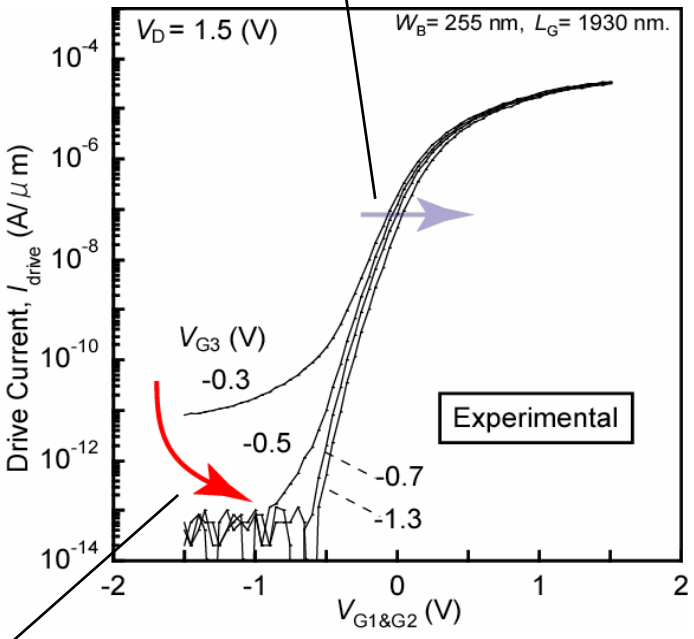
固定値の印可電圧を変えることによるデバイス特性の制御

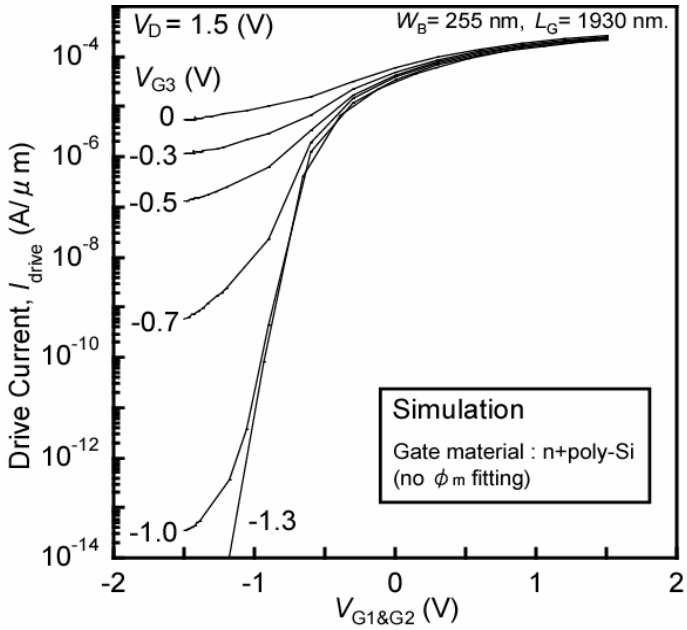
ダブルゲート動作におけるデバイス特性制御

固定値(V_{G3})を変化

しきい値電圧変化







オフリーク電流低減

デバイスシミュレーション*より期待される
オフリーク電流低減効果，しきい値電圧変動を確認

*DESSIS, ISE TCAD, release 9.5, Synopsys Co.,Ltd

新構造デバイス･微細化基盤技術

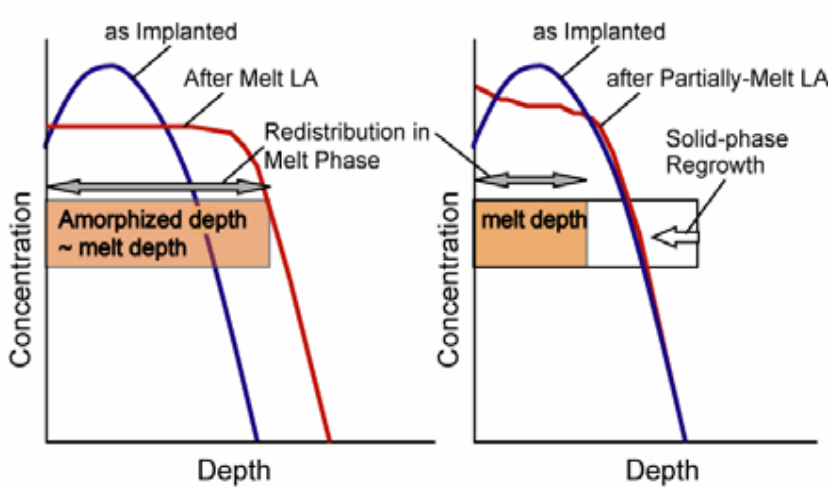
1.三次元　ビームチャネルトランジスタ (Beam Channel Transistor)
- with high current driving capability

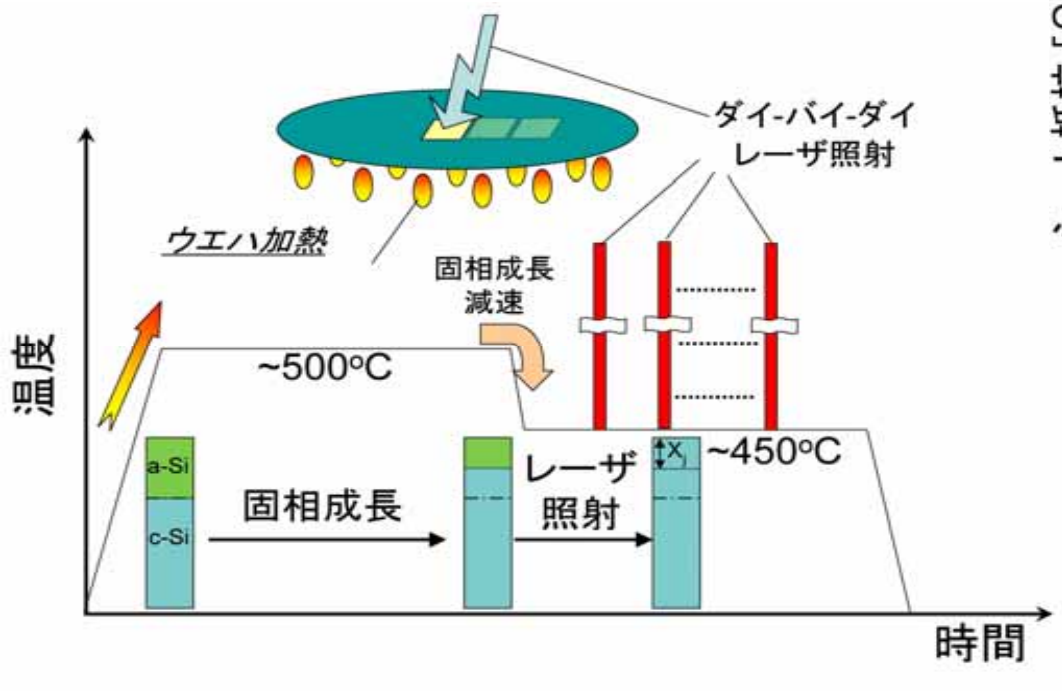
aiming at applications to power control with small chip area.

2. **仕事関数制御** NiSi **ゲート** MOS**デバイス**
- NiSi workfunction tuning method by Sb pre-doping to poly-Si before silicidation

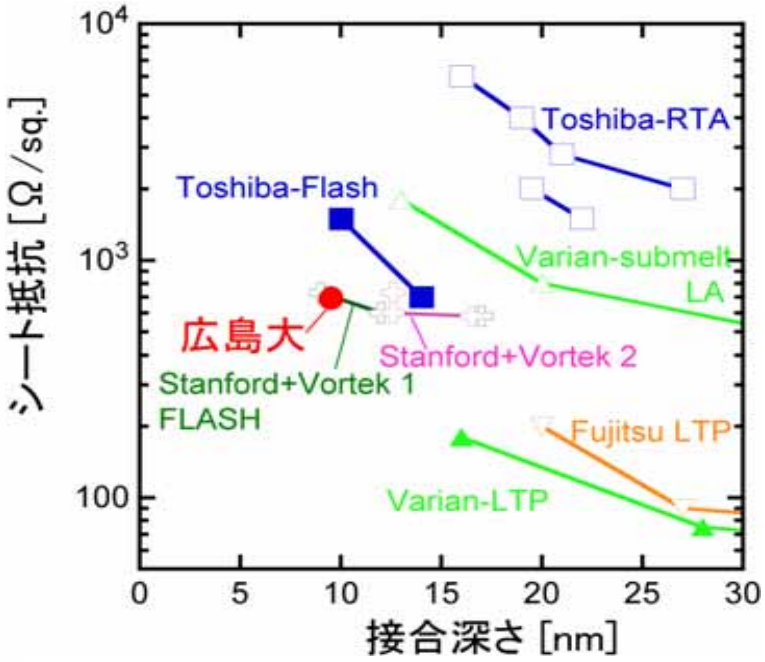
3. High-k **絶縁膜形成 原子層成長(ＡＬＤ)技術**
- Si-nitride/SiO2 stack gate dielectrics for future scaled DRAMs.
- Enhanced reliability in NBTI was achieved.

部分溶融レーザアニール(PMLA)法の提案





極浅低抵抗接合形成に適した新しいレーザアニール法、部分溶融レーザアニール法(Partial Melt Laser Anneal) を提案。低温固相成長を組み合わせることで、Siの極く浅い表面付近のみを溶融させることが特徴。

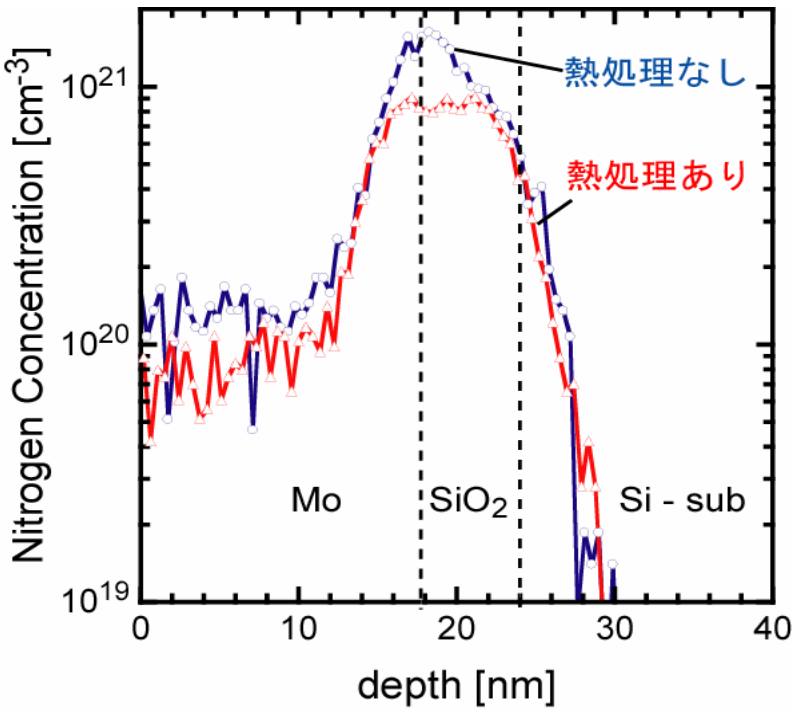


シート抵抗と接合深さのベンチマークで世界最高水準を達成。

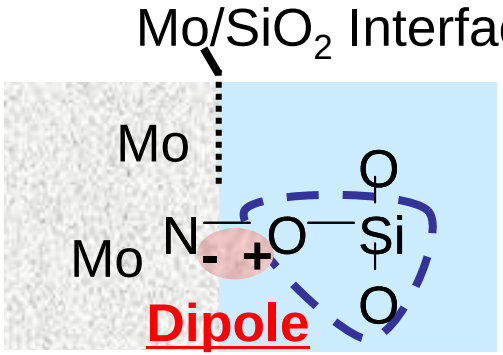
国際会議招待講演2回([10,18])

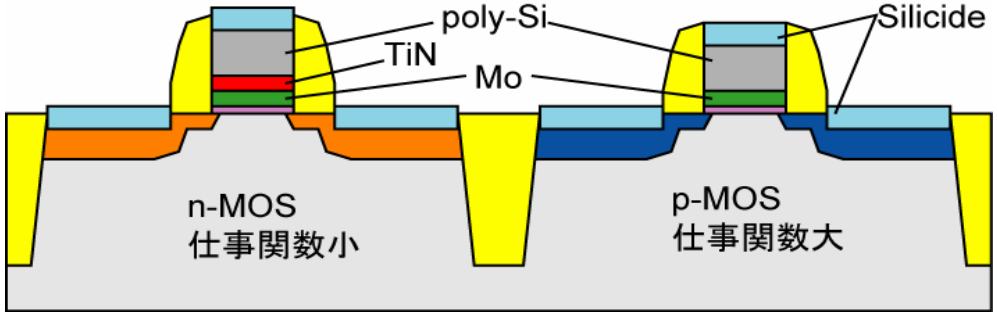
CMOSデバイスのためのMoゲート仕事関数変調の研究

Mo上に堆積させたTiNからNを固相拡散させMoの仕事関数変調 させる手法を初めてデバイスに適用。



仕事関数変調が界面にパイルアップしたNによることを明らかに(左上図青線)。→ 電気陰性度差に基づく双極子形成モデルを提案。国際会議[8]で発表





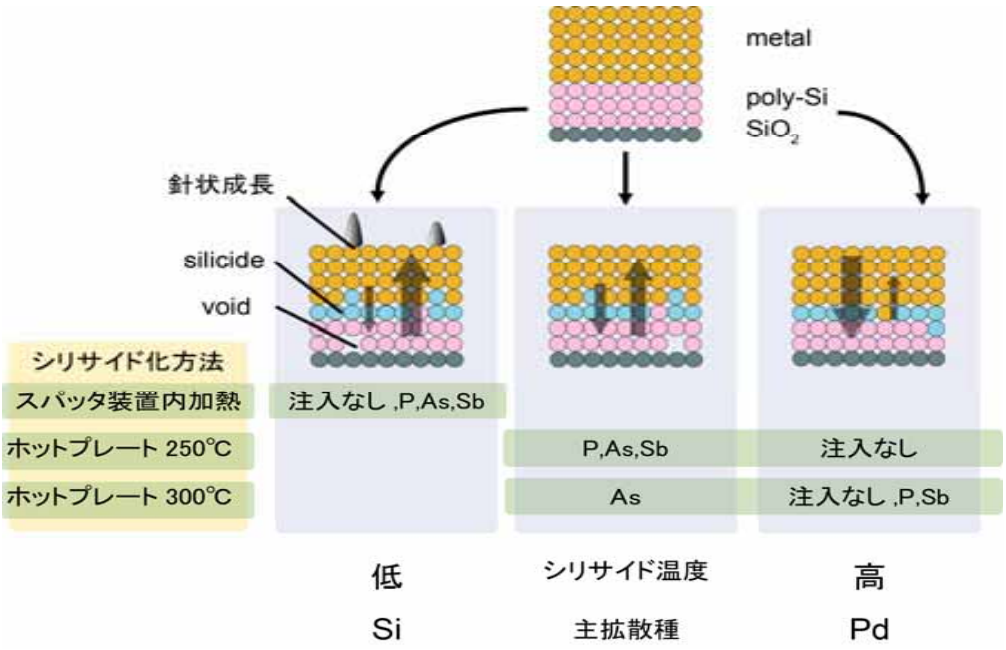
しかし、Nのパイルアップがデバイス製作時の熱処理中に減少する問題を発見(左上図赤線)

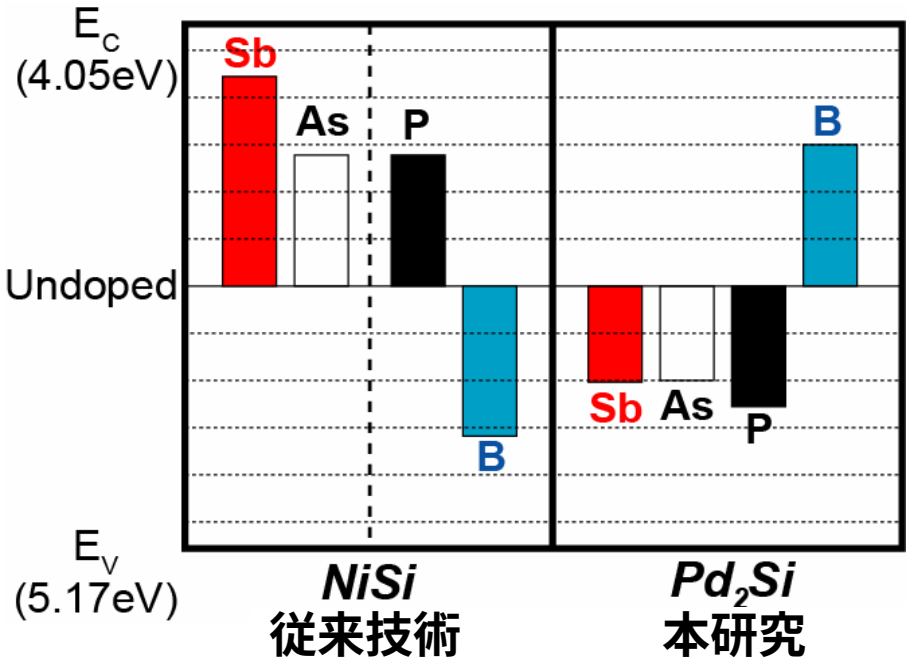
→ 対策プロセス･デバイス構造を提案

(日･米 特許出願済、国際会議[16]で発表、2006年4月国際会議招待講演予定)

新しいメタルゲート材料Pd_2Siの研究

次世代のMOSデバイスへの採用が期待されているフルシリサイドゲート構造(現在のポリシコンをシリサイドで置き換える構造)のための新しい材料を研究。Pd2Siは従来のNiSiに比べ、低温で形成可能であり、且つ低ストレスという特長を有す。





良質のPd2Si膜を得るためには、シリサイド化時のSiの拡散を抑えることが重要であることを解明。国際会議[22]で発表。

不純物導入による仕事関数変調が従来のNiSiと同等程度可能であることを実証。(国際会議投稿中)

21世紀COE最終年度はMOSFETへ適用し素子性能を評価予定。

新構造デバイス・微細化基盤技術

1.三次元　ビームチャネルトランジスタ (Beam Channel Transistor)
- with high current driving capability

aiming at applications to power control with small chip area.

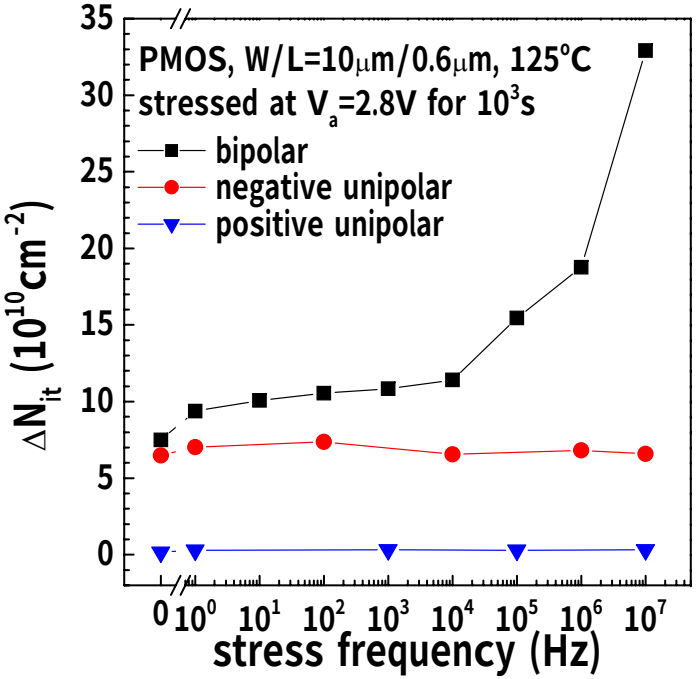
2. 仕事関数制御 NiSi ゲート MOSデバイス
- NiSi workfunction tuning method by Sb pre-doping to poly-Si before silicidation

3. High-k 絶縁膜形成 原子層成長(ＡＬＤ)技術
- Si-nitride/SiO2 stack gate dielectrics for future scaled DRAMs.
- Enhanced reliability in NBTI was achieved.

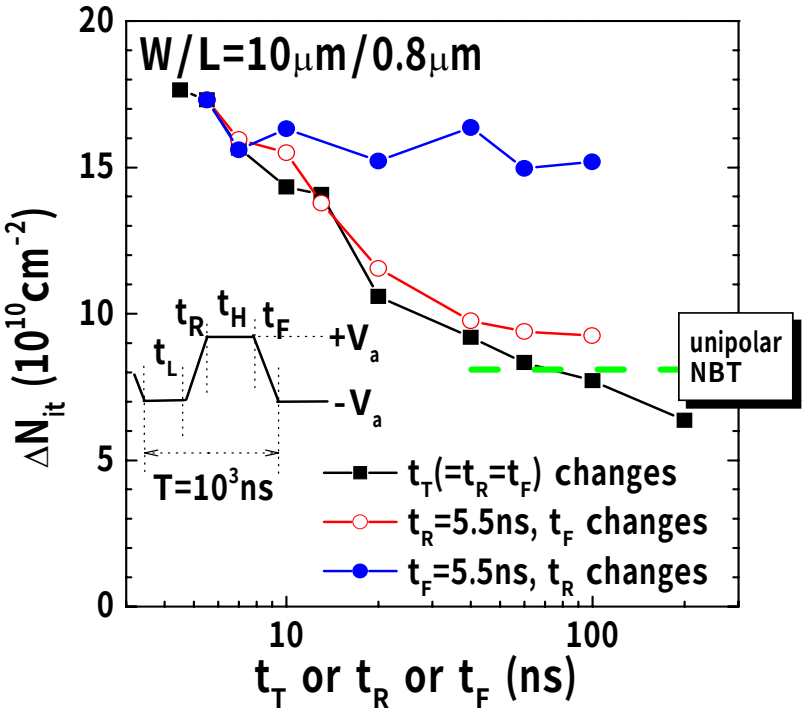
微細MOSのための高信頼性ゲート絶縁膜の開発

ダイナミックバイポーラパルスストレスによる窒化酸化膜ゲート絶縁膜における界面トラップ生成

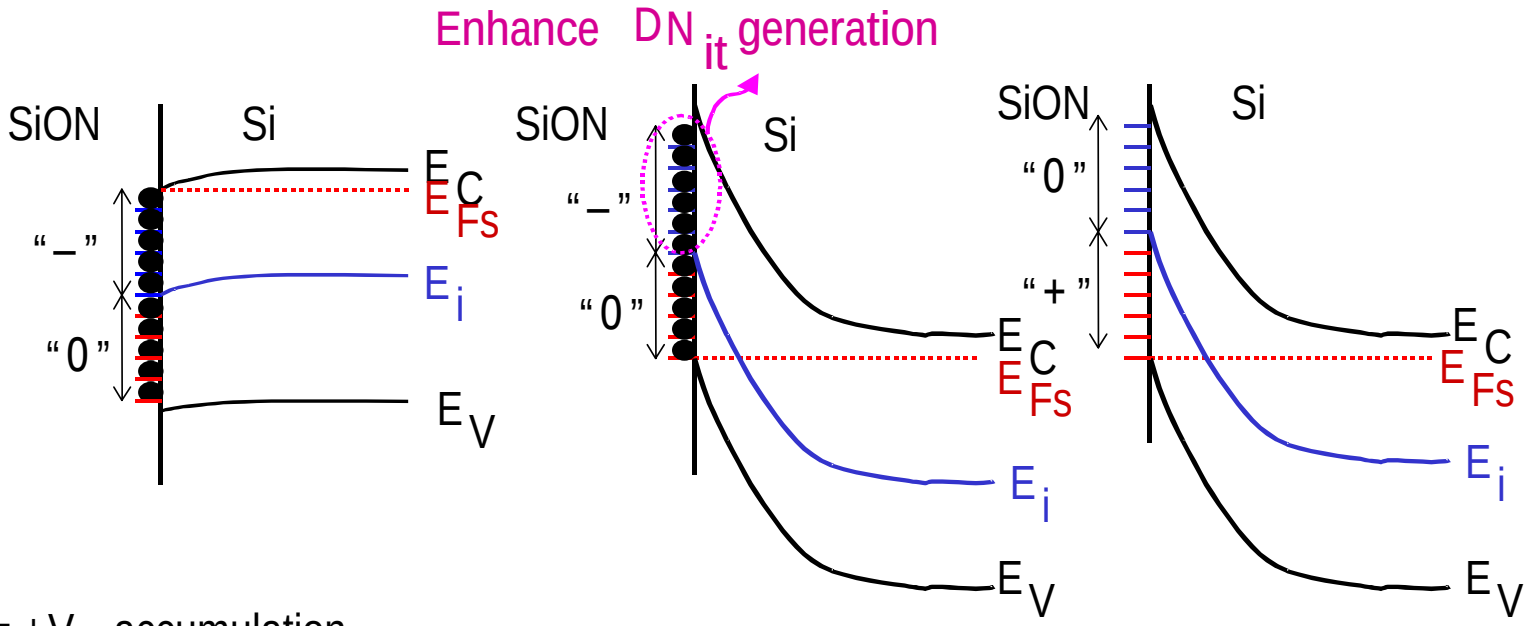
微細MOSFET適用のために、SiONゲート絶縁膜の信頼性を調べ、新知見を得た。



プラズマ窒化酸化膜ゲート絶縁膜を用いたpMOSFETのダイナミック電圧ストレス下界面トラップ生成量。
10^4 Hz以上の周波数領域において、周波数の増加に伴う界面トラップの急激な増加 が観測



界面トラップ生成量に対するバイポーラパルス電圧ストレスの立ち上がり･立下り時間依存性。　界面トラップ生成量は、立下り時間にのみ依存



$V_g = +V_a$ accumulation
$D N_{it}$ recovery

stage A

On the V_g reversal from+ V_a to $-V_a$
$D N_{it}$ enhancement occurs

stage B

$V_g = -V_a$ inversion
$D N_{it}$ generation

stage C

- 高周波バイポーラストレスにおける著しい界面トラップの増加は、界面におけるトラップ電子がゲート電圧V_gの急激な正から負への変化に追随できない事により生じる。
- 追随できない電子は過渡的にゲート電界と同じ向きの内蔵電界を作りSi-Hボンドの解離を促す。

IEEE Electron Device Letters, Vol. 26, No.3, pp. 216-218 (2005)

IEEE Electron Device Letters, Vol. 26, No.6, pp. 387-389 (2005)

IEEE Electron Device Letters, Vol. 26, No.9, pp. 658-660 (2005)

光電融合デバイスと量子デバイス技術

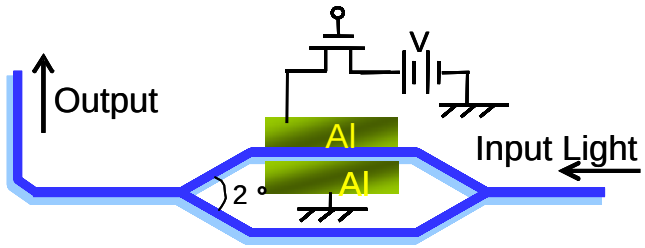
集積化光インタコネクションのための光機能素子　(横山G)
- 屈折率電界変調型リング共振器光スイッチで速度リミットを解決
- 電気光学(EO) 材料, 磁気光学 (MO) 材料を用いてSiに集積化
- 光電融合プロトタイプの試作, 実証

量子ドットを有する浮遊ゲート機能デバイス
- 超高感度光センサー (小数フォトンの検出と小数電子の輸送)
- 光入力多値メモリ、スイッチの室温動作
- 量子ドットのサイズ制御性, ドットの電子状態の制御

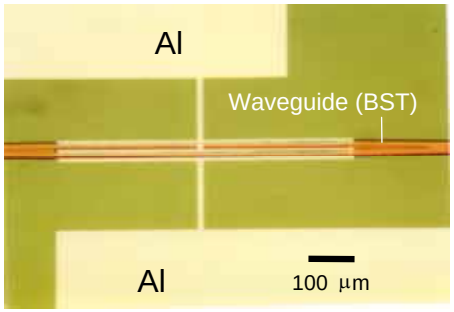
光応答によるスイッチ・メモリ動作の基礎研究
- C-V 特性の測定 光照射による変位電流の測定
- 電子注入および放出による電圧電流特性のヒステリシス

初めて電気光学材料$(Ba,Sr)TiO_3$を用いた モノリシックマッハツェンダー光スイッチの動作に成功

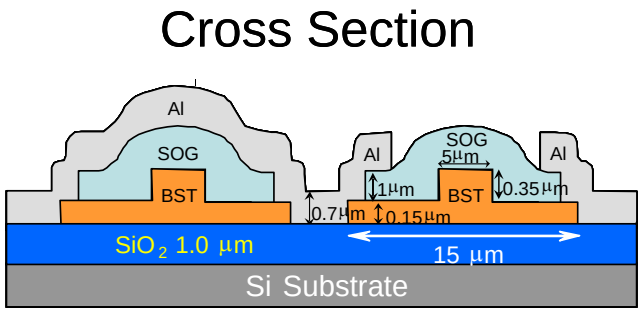
(a)

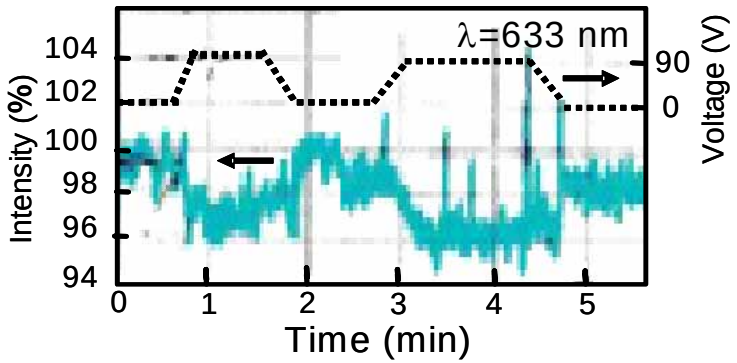


(b)



(c)





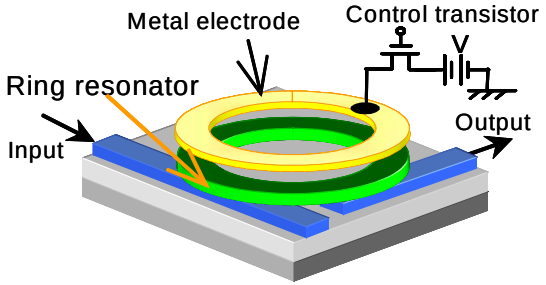
- 従来の電気光学材料(主に$LiNbO_3$が使用される)光スイッチは、引き上げ単結晶材料を用いたものが主流で、非常に高価で、集積化も困難であった。
- 今回開発した光スイッチは、メモリデバイス用に研究されていた$(Ba,Sr)TiO_3$を用いて、Si基板上に形成したもので、Si基板上に高集積化できる技術である。
- 変調特性は、現状では4%と低いが、今後、膜の結晶性を向上させ、小型のリング共振器型の光スイッチを形成して実用化にもっていきたい.

国際会議発表2005SSDM、投稿中Appl. Phys. Lett.

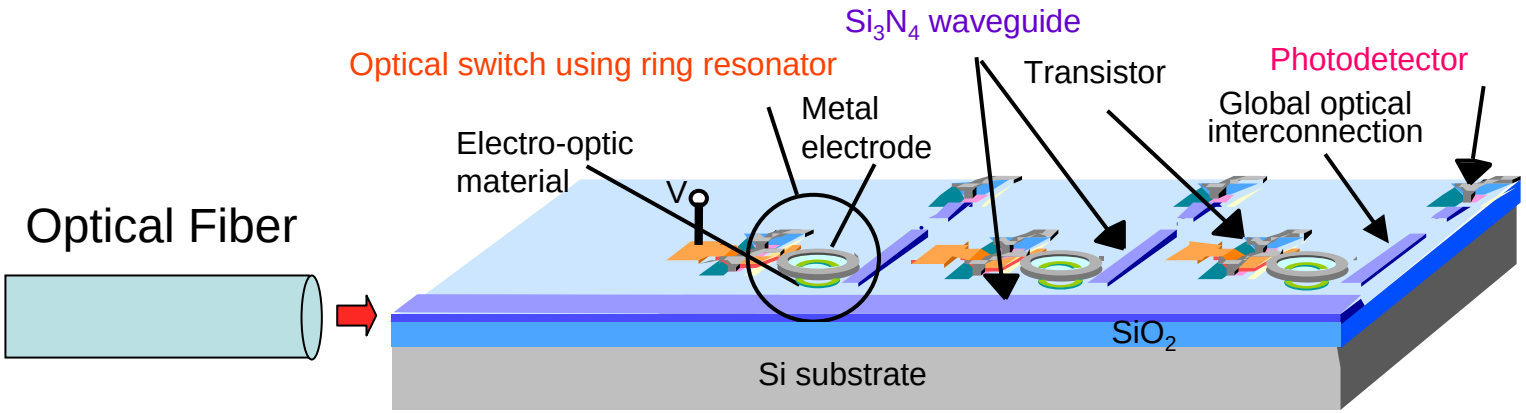
今後1年間の計画

1．$(Ba,Sr)TiO_3$を膜の結晶性を向上させ、実用的な光変調効率を得る。ーバッファ層(MgO等) の挿入により結晶性を改善

2．リング共振器型光スイッチを試作･動作確認



3. 光変調素子、フォトディテクタ、光導波路を集積した光配線集積回路プロトタイプの試作と動作実証



光電融合デバイスと量子デバイス技術

集積化光インタコネクションのための光機能素子　(横山G)
・屈折率電界変調型リング共振器光スイッチで速度リミットを解決
・電気光学(EO) 材料，磁気光学 (MO) 材料を用いてSiに集積化
・光電融合プロトタイプの試作，実証

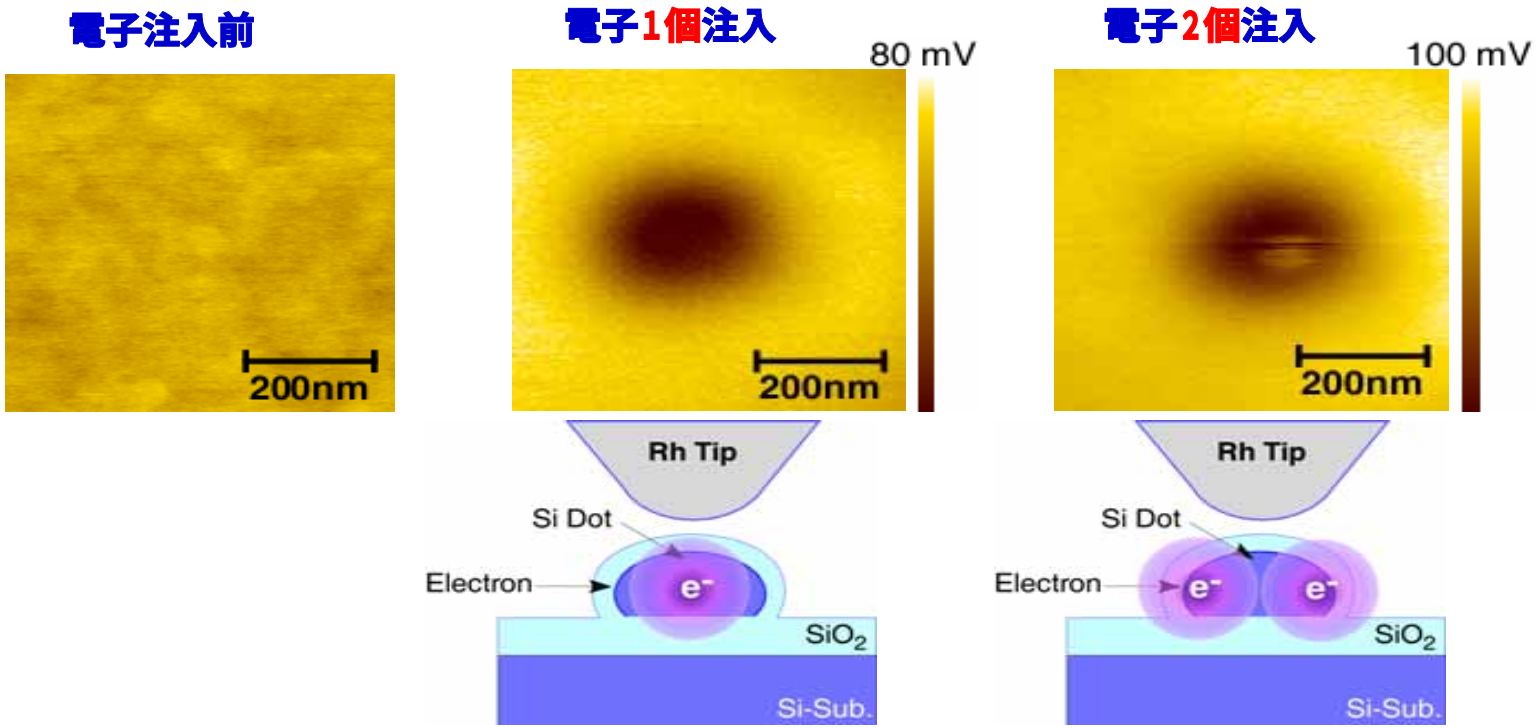
量子ドットを有する浮遊ゲート機能デバイス
・超高感度光センサー (小数フォトンの検出と小数電子の輸送)
・光入力多値メモリ、スイッチの室温動作
・量子ドットのサイズ制御性，ドットの電子状態の制御

光応答によるスイッチ・メモリ動作の基礎研究
・C-V 特性の測定 光照射による変位電流の測定
・電子注入および放出による電圧電流特性のヒステリシス

量子ドットへの電荷注入と帯電状態評価

1つの量子ドットに注入された2個の電子間のクーロン反発によって生じるドーナツ状の特徴的表面電位の測定に成功した⇒電子1個の注入・放出による量子ドットの帯電状態変化の直接観察技術を確立

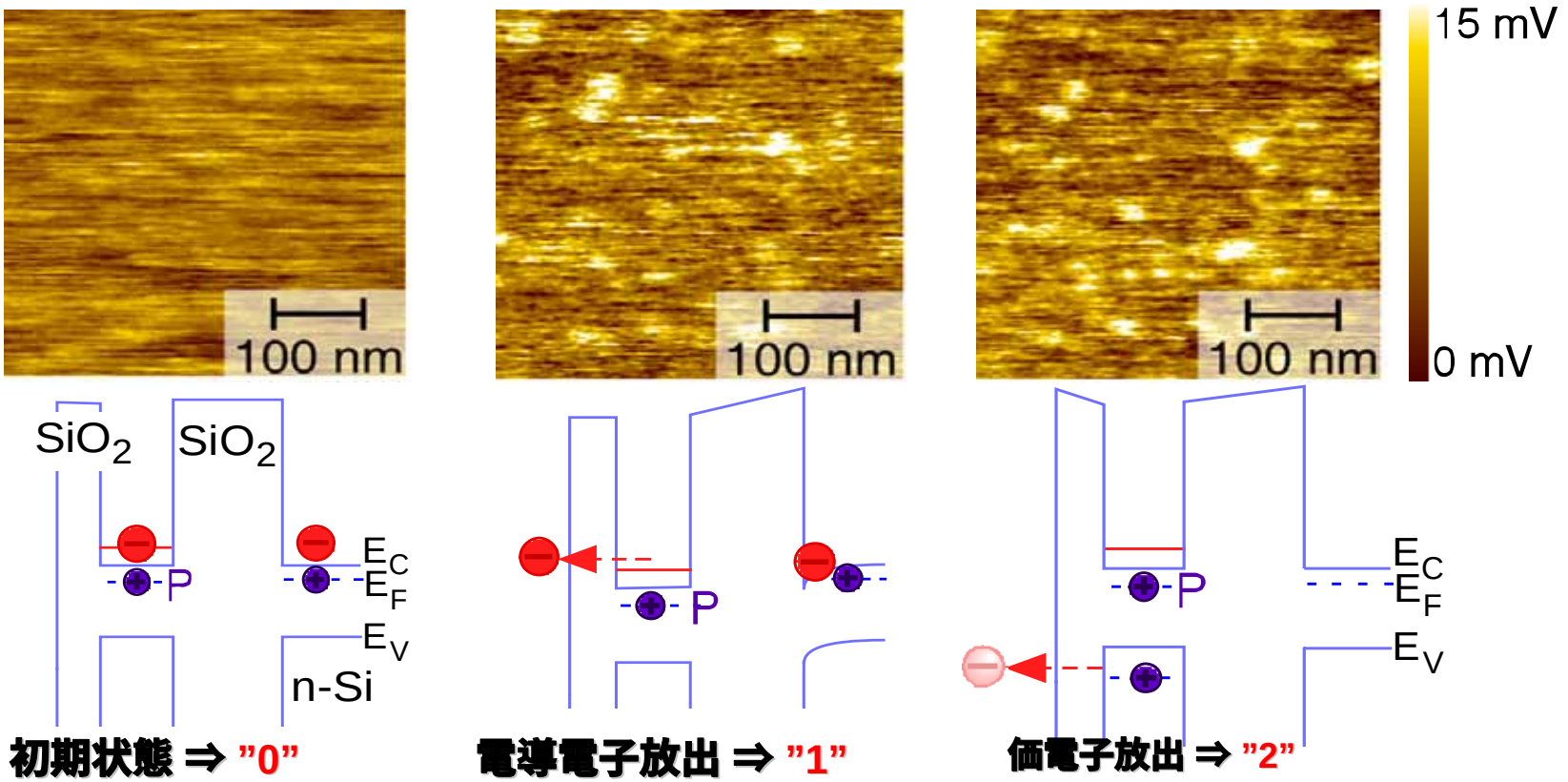
・導電性AFM/KFMにより評価したSi量子ドットの表面電位像



ドーピングによるSi量子ドットの価電子制御

Si量子ドットへのPおよびBドープにより低電圧多段階電子注入・放出動作を確認した⇒低電圧動作多値メモリに必要な価電子制御技術を確立

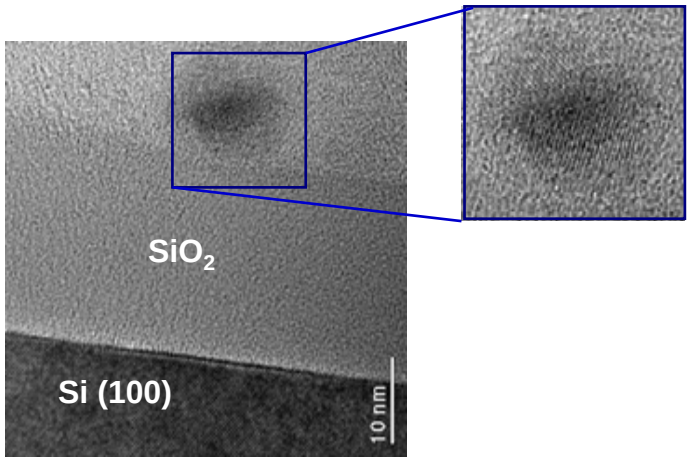
・導電性AFM/KFMにより評価したSi量子ドットの表面電位像

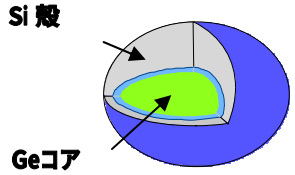


Geコアを有するSi量子ドット(擬似スーパーアトム構造)の帯電状態評価

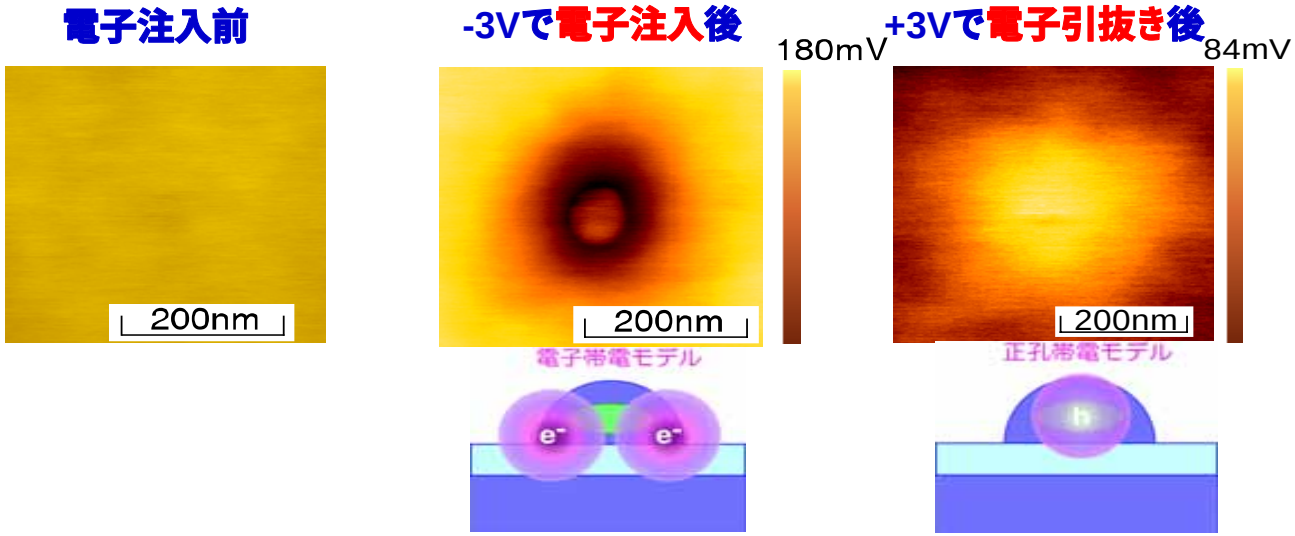
Geコアを有するSi量子ドット表面電位の測定から、正孔はGeコアに、電子はSi殻に閉じ込められることがわかった　⇒擬似スーパーアトム構造による受発光デバイス実現の可能性を検証できた

・Geコアを有するSi量子ドットの断面TEM像





・Geコアを有するSi量子ドットの表面電位像

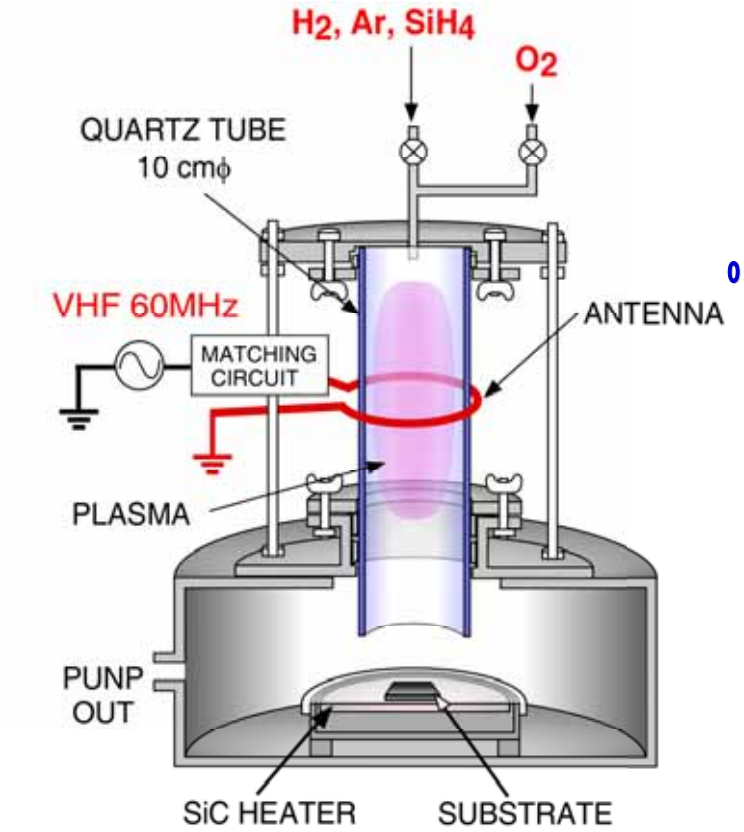


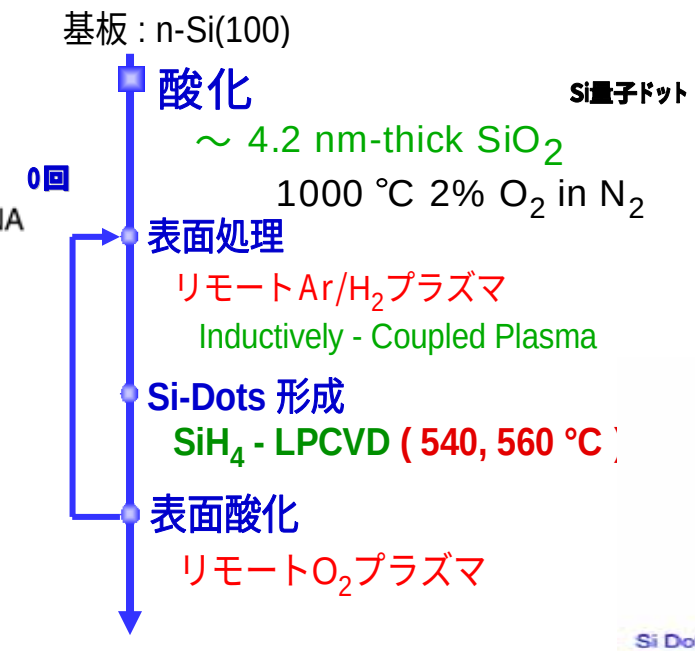
Si量子ドット積層構造の作製と帯電状態評価

ドライプロセスによるSi量子ドット積層構造の作製

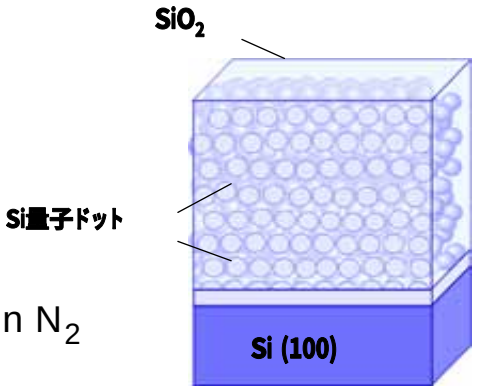
リモートプラズマおよびLPCVD法の組み合わせにより、真空一貫プロセスでSi量子ドット積層構造の作製に成功 ⇒ 光入力メモリや、高感度光センサ、発光デバイス実現の礎となるSi量子ドット積層構造作製技術を確立

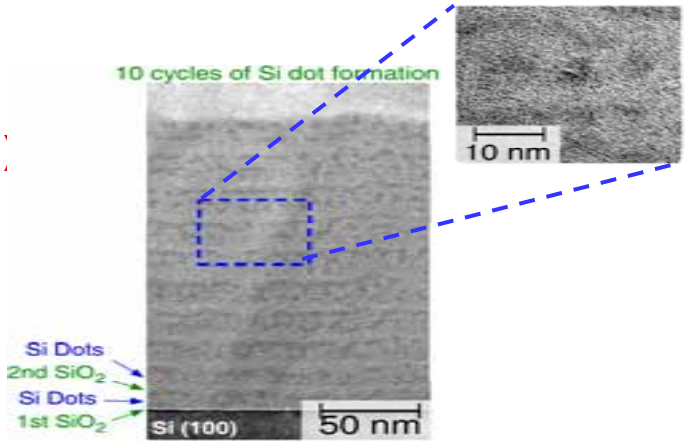
・Si量子ドット積層構造作製装置とプロセスフロー





・Si量子ドット積層構造の概略図と作製した積層構造の断面TEM像



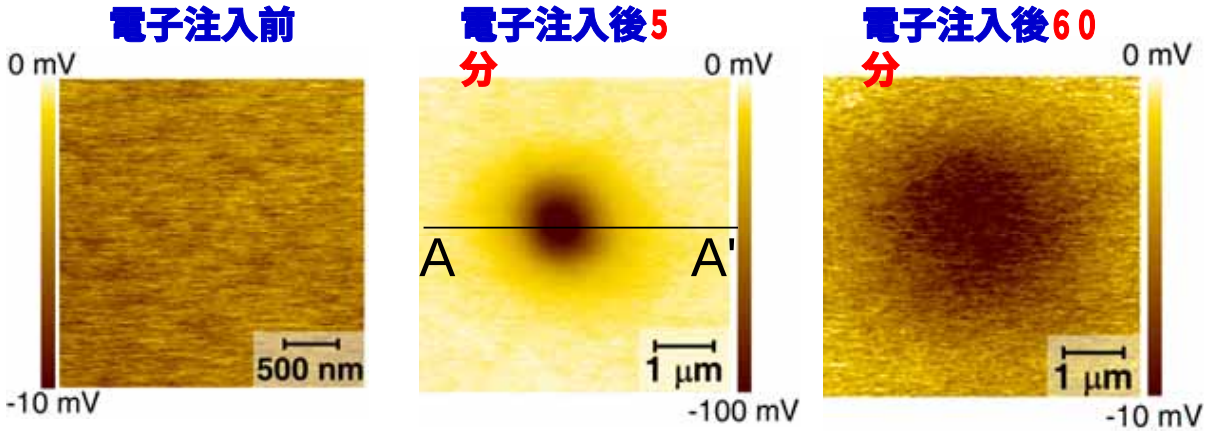


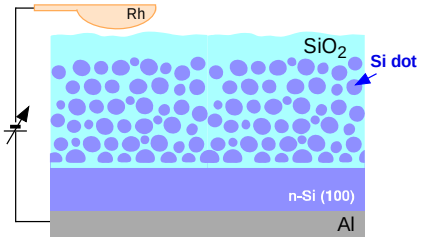
Si量子ドット積層構造の帯電状態評価

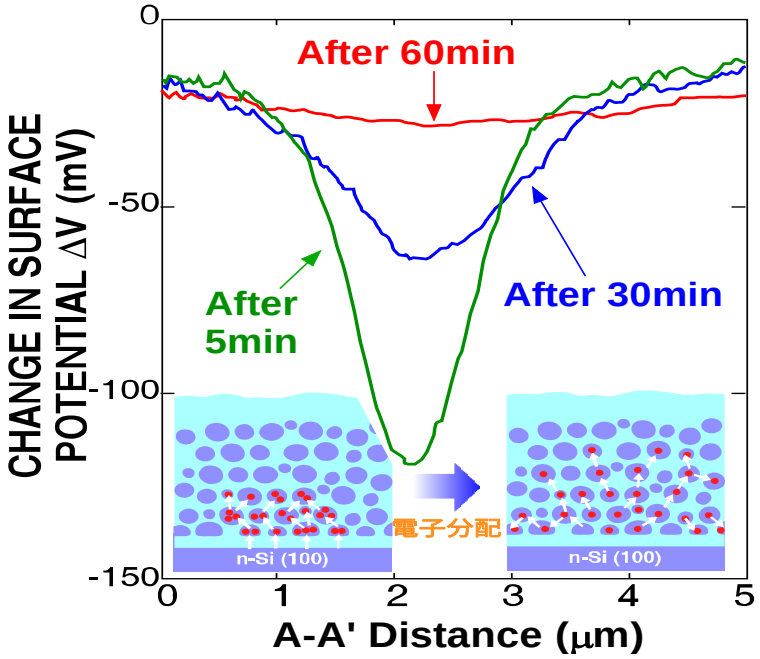
Si量子ドット積層構造における隣接ドット間の電荷移動の直接観察に成功⇒量子ドット間の電荷移動を利用した光入力メモリや、高感度光センサ、発光デバイス実現の可能性を実証

・Si量子ドット積層構造における電荷移動と表面電位経時変化

・Si量子ドット積層構造への電荷注入後の表面電位像の経時変化

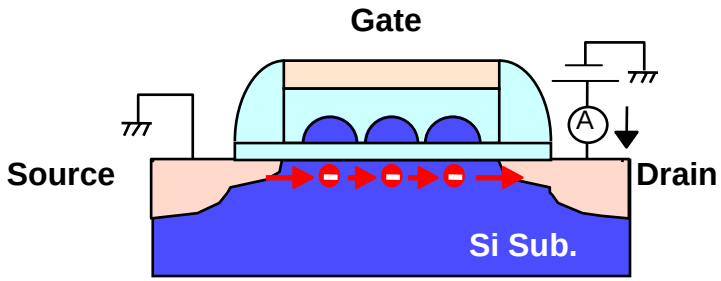




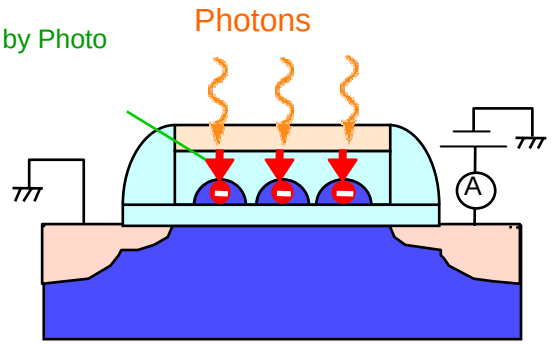


Si量子ドットを用いた高機能デバイスの実現

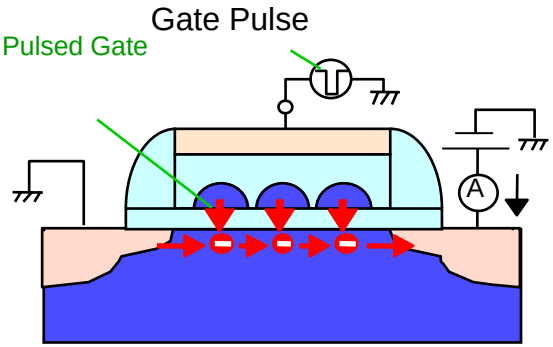
光書き込みメモリ



Electron injection by Photo Excitation

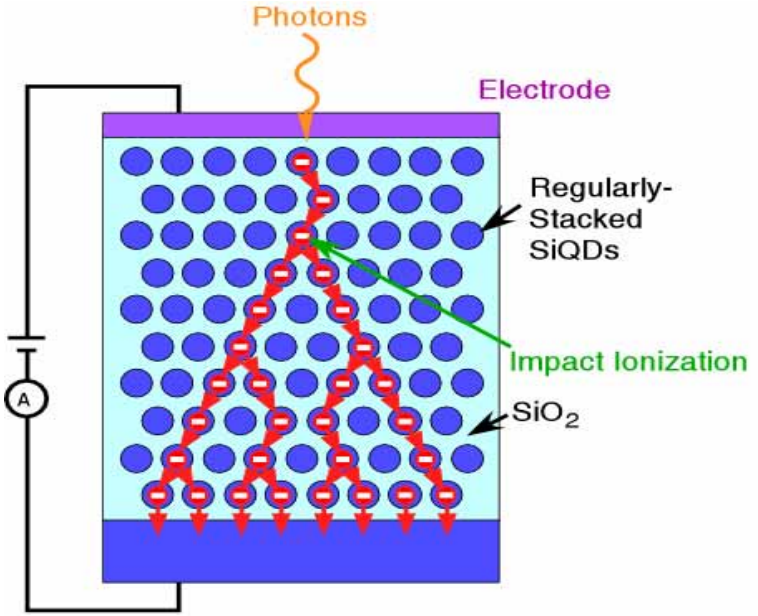


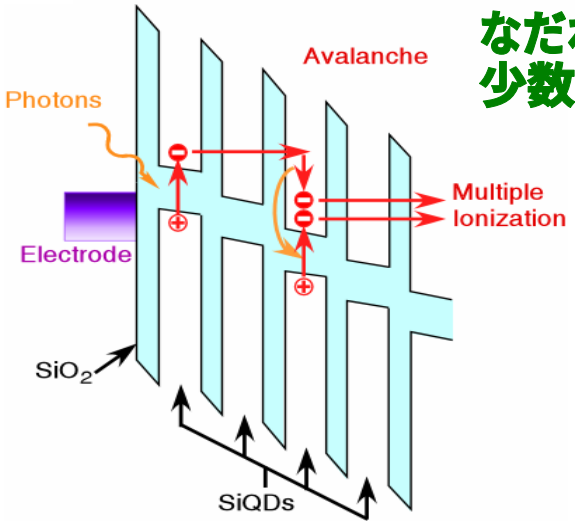
Electron Emission by Pulsed Gate Bias



光集積に不可欠なSiベースの受発光デバイスの実現

高感度光センサー





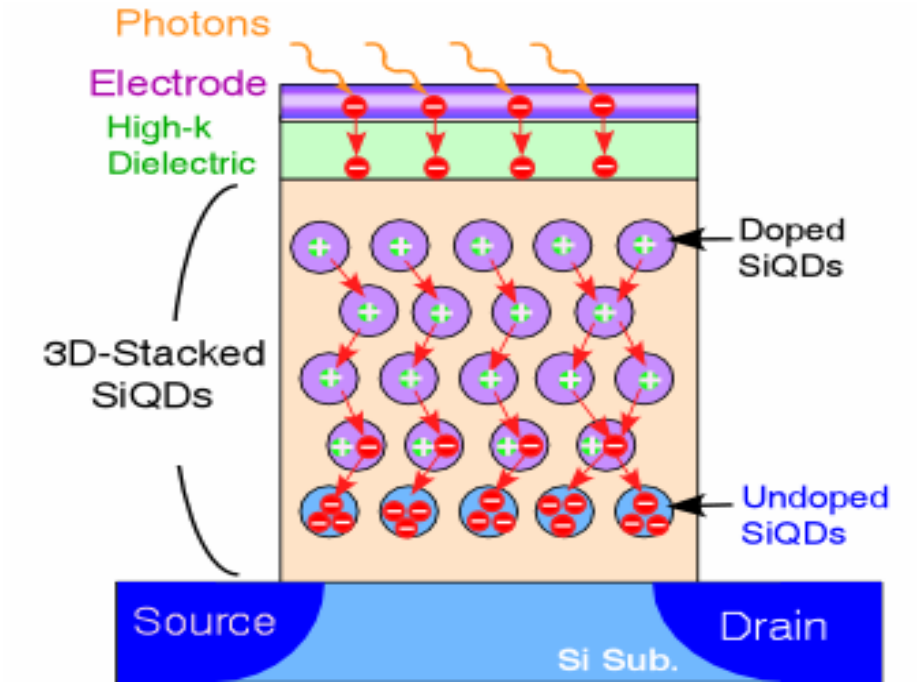
なだれ増倍による少数フォトンセンサー

Si量子ドットを用いた高機能デバイスの実現

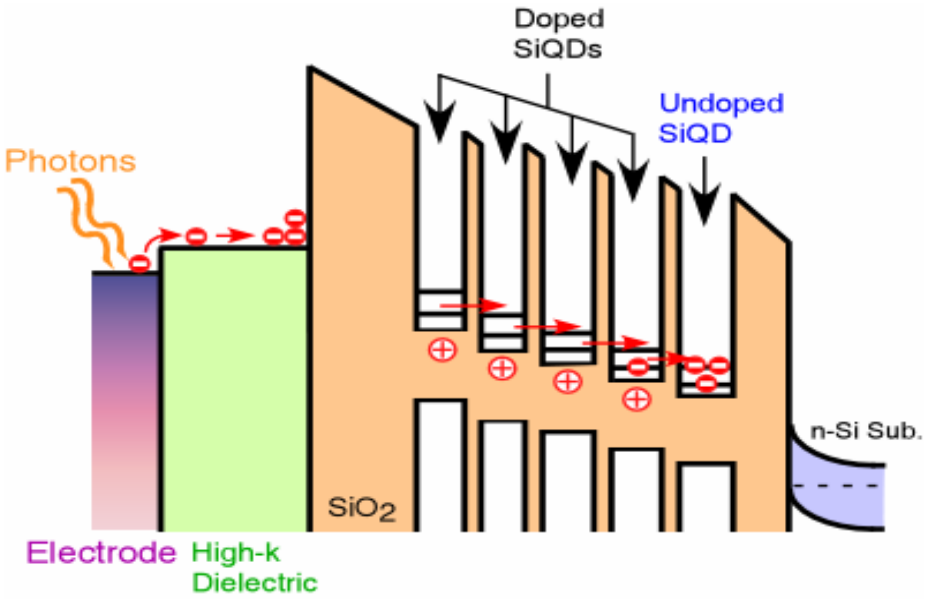
高機能MOSFET

発光デバイス

超高感度光スイッチMOSFET



量子ドットLED



光集積に不可欠なSiベースの受発光デバイスの実現

教育システム

広島大学大学院先端物質科学研究科
半導体集積科学専攻

高度情報社会におけるネットワーク，モバイル通信，コンピュータ，デジタル家電，ロボットなどの頭脳は半導体集積回路（ＬＳＩ）で実現されている。
将来，ナノスケールのトランジスタの原理，構造，製造法を開拓して，新しいモデリングによる回路･アーキテクチャの設計方法を研究して，未踏の高度な認識能力を持ったブレインを，極限的な低エネルギーと小型，軽量で実現することを目指している。

本専攻は**広島大学21世紀COE「テラビット情報ナノエレクトロニクス」**を推進する教育組織です．**ナノデバイス･システム研究センター**と協力して，半導体集積回路の革新的なアイディアと先端研究設備を活用した実践的な研究をとおして設計から製造プロセス技術までを一貫して捉えられる視野の広い先端研究者と専門技術者の育成を目的としている．

半導体集積科学専攻の研究室と教員

研　究　室	教　育　研　究　内　容	担当教官　(他機関経験)
量子半導体工学	半導体量子構造を利用した新機能デバイスの開発および次世代･超微細トランジスタ実現の為の材料･プロセスインテグレーション	宮崎　誠一 東　清一郎　(ｾｲｺｰｴﾌﾟｿﾝ)
極微細デバイス工学	極限デバイスにおける基本動作原理の解明とこれに基づく電気応答シミュレーション手法の確立，及び高精度電流制御を実現する次世代デバイスの開発。	三浦　道子　(シーメンス) 江崎達也　(NEC)
機能集積ｼｽﾃﾑ工学	極限的性能の通信情報処理アナログ回路･アナデジ混載回路の設計技術，無線インタコネクトを導入した三次元集積システムの方式･設計技術，および生命体処理原理に基づくロボットのビジョンやブレインの高度認識･知能化技術	岩田　　穆　(NTT) 佐々木　守　(熊本大)
ナノデバイス工学	LSIの高密度集積化に伴って生じた問題を解決するための極限微細デバイス技術の開発およびワイヤレス伝送技術	吉川　公麿　(NEC) 芝原 健太郎　(NEC)
ナノプロセス工学	極限デバイス及びフォトニックデバイスに必用な原子スケール加工技術･ナノプロセス技術	横山　　新　(筑波大) 中島　安理　(富士通)
ナノ集積工学	極微細デバイスおよびナノ要素プロセスを有機的に組み合わせ、極限立体集積回路実現の集積技術	角南　英夫　(日立)
知能集積回路工学	高速かつ低消費電力なデータアクセスとパターンマッチング機能などを有するメモリベースの柔軟な知能情報処理システム，アーキテクチャ，及びLSI回路技術	マタウシュ H．J． (シーメンス) 小出　哲士　(東大VDEC)

ナノデバイス･システム研究センター

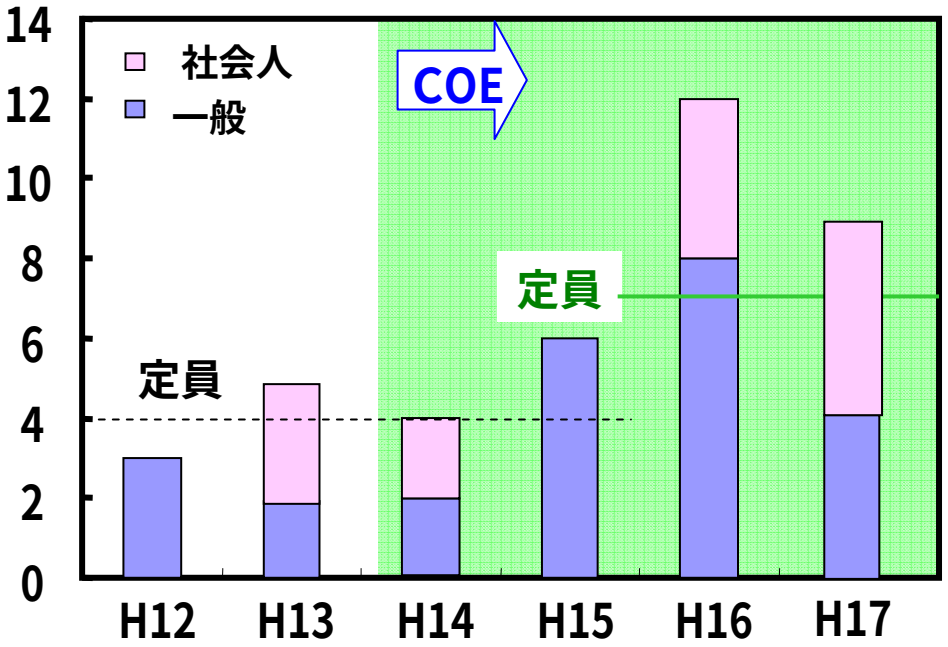
半導体集積科学専攻授業科目

必修科目		先端物質科学講究 先端物質科学特別講義 科学技術英語表現法	10単位 2単位 2単位
選択必修科目	概論科目	基礎物理概論 バイオテクノロジー概論 エレクトロニクス概論※2	1科目2単位
	実習、演習	集積回路･プロセス演習 インターン（企業派遣研修）	1科目2単位
選択科目	1. 材料･デバイス科目	半導体物性工学 電子デバイス物理 半導体シミュレーション工学 化合物半導体デバイス	1-4分類の 3分類以上から 6科目 12単位を取得
	2. 集積化技術科目	LSI集積化工学 半導体メモリ 集積化情報伝送工学	
	3. システム･ 回路設計科目	システムLSI設計 アナログ集積回路 知能集積回路 マイクロコンピュータ設計	
	4. 横断科目	集積システム信頼性 光電融合システム 分子･バイオデバイス	

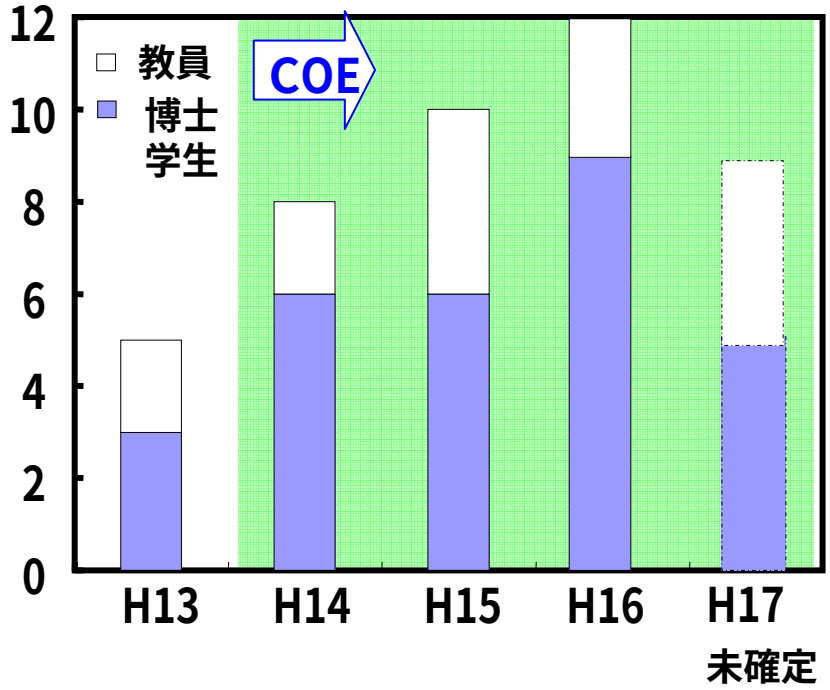
博士課程教育の充実

1．博士課程後期学生の数と質の向上

入学学生数



被表彰数



2．進路の見通し

実績：　半導体企業：40%，ポスドク研究員40%，公的研究機関１０%

見通し：　半導体企業への就職は伸びることは確実と思われる
大学のポストの確保が課題．組織再編による確保を目指す．

研究業績リスト

論文リスト (岩田, 佐々木グループ)

[IS-1] H. Ando, T. Morie, M. Miyake, M. Nagata and A. Iwata, “Image Segmentation/Extraction Using Nonlinear Cellular Networks and their VLSI Implementation Using Pulse-Modulation Techniques”, IEICE Trans. Fundamentals, Vol. E85-A, No. 2, pp. 381-388, (2002).

[IS-2] T. Morie and T. Matsuura and M. Nagata and A. Iwata, “A Multi-Nano-Dot Circuit and Structure Using Thermal-Noise Assisted Tunneling for Stochastic Associative Processing”, J. Nanosci. Nanotech., Vol. 2, No. 3, pp. 343-349, (2002).

[IS-3] K. Katayama, M. Nagata, T. Morie and A. Iwata, “An Hadamard Transform Chip Using the PWM Circuit Technique and Its Application to Image Processing”, IEICE Trans. Electron., Vol. E85-C, No. 8, pp. 1596-1603, (2002).

[IS-4] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models ”, IEEE Trans. Nanotechnology, Vol. 2, No. 3, pp. 158-164, (2003).

[IS-5] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, “A Design of Neural Signal Sensing LSI with Multi-Input Channels”, IEICE Trans. Fundamentals, vol.E87-A, pp.376-pp.383, (2004).

[IS-6] T. Morie, K. Murakoshi, M. Nagata and A. Iwata, “Pulse Modulation Techniques for Nonlinear Dynamical Systems and a CMOS Chaos Circuit with Arbitrary 1-D Maps”, IEICE Trans. Electron., Vol. E87-C, No. 11, pp. 1856-1862, 2004

[IS-7] T. Yoshida, M. Akagi, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu, “A Design of Wireless Neural-Sensing LSI ”, IEICE Trans. Electronics, Vol.E87-C, pp.996-1002. (2004).

[IS-8] T. Yoshimura and A. Iwata“, An analysis of interference in synchronous systems”, IEICE Electronics, Express, Vol.1, No.15, pp.465-471, (2004).

[IS-9] M. Shiozaki, T. Mukai, M. Ono, M. Sasaki, A. Iwata, “A 2.7 Gcps and 7-Multiplexing CDMA Serial Communication Chip Using Two-Step Synchronization Technique”, IEICE Trans. Electron., vol.E88-C, No.6, pp.1233-1240, (2005).

[IS-10] M. Shiozaki, T. Mukai, M. Ono, M. Sasaki, A. Iwata, “A 2.7 Gcps and 7-Multiplexing CDMA Serial Communication Chip for Real-Time Robot Control with Multiprocessors”, Journal of Robotics and Mechatronics ”,vol.17, No.4, pp.463-468, (2005).

[IS-11] M. Shiozaki, M. Sasaki, A. Mori, A. Iwata and H. Ikeda, “20GHz uniform-phase uniform-amplitude standing-wave colck disrtribution”, IEICE Electronics Express, Vol. No. 3, No.12, pp11-16, (2006).

国際会議リスト (岩田, 佐々木グループ)

[IS-C-1] M. Nagata, Y. Murasaka, Y. Nishimori, T. Morie, and A. Iwata, “Substrate Noise Analysis with Compact Digital Noise Injection and Substrate Models”, Proc. 7th Asia and South Pacific Design Automation Conf, pp. 71-76, Bangalore, Jan, (2002).

[IS-C-2] T. Morie, J. Umezawa, T. Nakano, H. Ando, M. Nagata, and A. Iwata, “A Biologically-Inspired Object Recognition System Using Pixel-Parallel Feature Extraction VLSIs”, International Invitational Workshop on Intelligent Interface Devices, pp. 35-37, Kitakyushu, March 14, (2002).

[IS-C-3] M. Nagata, T. Morie, and A. Iwata, “Modeling Substrate Noise Generation in CMOS Digital Integrated Circuits”, IEEE 2002 Custom Integrated Circuit Conf, Orlando, May, (2002).

[IS-C-4] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “A Multi-Nanodot Floating-Gate MOSFET Circuit for Spiking Neuron Models”, 2002 IEEE Silicon Nanoelectronics Workshop, pp.53-54, Honolulu, June 9, (2002).

[IS-C-5] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, “An Efficient Clustering Algorithm Using Stochastic Association Model and Its Implementation Using Nanostructures”, Advances in Neural Information Processing Systems 14, Ed. T. G. Dietterich, S. Becker and Z. Ghahramani, MIT Press, Cambridge, MA, (2002).

[IS-C-6] K. Katayama and A. Iwata, “A High-Resolution Hadamard Transform Chip”, International Conference on Solid State Devices and Materials (SSDM), pp. 372-373, Nagoya, September17-19, (2002)

[IS-C-7] T. Maeda, A. Iwata, M. Kawabata, and S. Orisaka, “A 10-GHz Bipolar VCO with Reduced Phase Noise”, International Conference on Solid State Devices and Materials (SSDM), pp. 370-371, Nagoya,

September17-19, (2002).
[IS-C-8] H. Ando, T. Morie, M. Nagata, and A. Iwata, "An Image Region Extraction LSI Based on a Merged/Mixed-Signal Nonlinear Oscillator Network Circuit", 28th European Solid-State Circuits Conference (ESSCIRC 2002), CP.11, pp. 703-706, Florence, Italy, Sept. 26, (2002).
[IS-C-9] K. Katayama and A. Iwata, "Pulse Coupled Neural Network using Coupled Phase Locked Loop", International Symposium on Nonlinear Theory and its Applications (NOLTA), pp. 853-856, Xi'an, October 7-11, (2002).
[IS-C-10] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, "An Efficient Clustering Algorithm Using Stochastic Association and Its Implementation Using 3D-Nanodot-Array Structures" (Invited) 2003 RCIQE International Seminar on Quantum Nanoelectronics for Meme-Media-Based Information Technologies, pp. 59-63 , Sapporo, Feb. 13, (2003).
IS-C-11] A. Iwata "Advanced Design for Analog-RF and Digital Mixed LSIs- Crosstalknoise Evaluaiton and Reduction", Proc. of the Workshop on SASIMI, pp.17-22, Hiroshima, April 3, (2003) Invited.
[IS-C-12] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Design of Neural Signal Sensing LSI with Multi-Input-Channels", Proc. of the Workshop on SASIMI, pp. 206-210, Hiroshima, April 3, (2003).
[IS-C-13] S. Kameda and T. Yagi, "A silicon retina system that calculates direction of motion", Proc. The 2003 IEEE International Symposium on Circuits and Systems, vol.IV, pp.792-795, Bangkok, Thailand, May, (2003).
[IS-C-14] S. Kameda and T. Yagi, "An analog silicon retina with multi-chip configuration", International Joint Conference on Neural Networks 2003 Conference Proceedings, pp.387-392, Oregon, the United States, July, (2003).
[IS-C-15] T. Morie, T. Nakano, J. Umezawa, and A. Iwata, "Gabor-Type Filtering Using Transient States of Cellular Neural Networks", Intelligent Automation and Soft Computing, Vol. 10, No. 2, pp. 95-104, (2004).
[IS-C-16] K. Korekado, T. Morie, O. Nomura, H. Ando, T. Nakano, M. Matsugu, and A. Iwata, "A VLSI Convolutional Neural Network for Image Recognition Using Merged/Mixed Analog-Digital Architecture," Int. J. Fuzzy and Intelligent Systems, in press, (2004).
[IS-C-17] T. Morie, J. Umezawa, and A. Iwata, "Gabor-Type Filtering Using Transient States of Cellular Neural Networks", Intelligent Automation and Soft Computing,Vol. 10, No. 2, pp. 95-104, (2004).
[IS-C-18] M. Shiozaki, T. Mukai, M. Ono, M. Sasaki and A. Iwata, "A 2Gbps and 7-multiplexing CDMA Serial Receiver Chip for Highly Flexible Robot Control System", 2004 Symposium on VLSI Circuits, Digest of Technical Papers, pp.194-197,Honolulu, Hawaii, June 17-19, (2004).
[IS-C-19] T. Morie, J. Umezawa, and A. Iwata, "A Pixel-Parallel Image Processor for Gabor Filtering Based on Merged Analog Digital Architecture", 2004 Symposium on VLSI Circuits, Digest of Technical papers, pp. 212-213, Honolulu, Hawaii, June 18, (2004).
[IS-C-20] T. Morie, T. Nakano, J. Umezawa, and A. Iwata, "Gabor Filtering Using Cellular Neural Networks and its Application to Face/Object Recognition", World Automation Congress, #IFMIP075, Seville, Spain, June 28 - July 1, (2004).
[IS-C-21] K. Sasaki, T. Morie, and A. Iwata, "A Spiking Neural Network with Negative Thresholding and Its Application to Associative Memory", 2004 IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS2004), pp. III-89 – III92, Hiroshima, July 25-28, (2004).
[IS-C-22] O. Nomura, T. Morie, K. Korekado, M. Matsugu, and A. Iwata, "A Convolutional Neural Network VLSI Architecture Using Thresholding and Weight Decomposition", Int. Conf. on Knowledge-Based Intelligent Information and Engineering Systems (KES'2004), Wellington, New Zealand, Sept. 22-24, (2004).
[IS-C-23] T. Yoshida, T. Mashimo, M. Akagi, A. Iwata, M. Yoshida and K. Uematsu, "A Low Noise Amplifier using Chopper Stabilization for a Neural Sensor LSI", Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials (Tokyo), pp.148-149, (2004).
[IS-C-24] A. Iwata, M. Sasaki, T. Kikkawa, S. Kameda, H.Ando, K.Kimoto, D.Arizono and H.Sunami, "A 3D-Integration Scheme Utilizing Wireless Interconnections for Implementing Hyper Brains", IEEE 2005 International Solid-State Circuits Conference Digest of Technical Papers, TP14.4, pp. 262-263, San Francisco, Feb 6-10, (2005).
[IS-C-25] M. Nagata, M. Fukazawa, N. Hamanishi, M. Shiochi, T. Iida, J. Watanabe, Y. Murasaka and A. Iwata, "Substrate Integrity Beyond 1GHz", IEEE 2005 International Solid-State Circuits Conference Digest of Technical Papers, TP14.6, pp. 266-267, San Francisco, Feb 6-10, (2005).

[IS-C-26] T. Yoshida, M. Akagi, M. Sasaki and A. Iwata, “A 1V Supply Successive Approximation ADC with Rail-to-Rail Input Voltage Range”, Proceedings of 2005 IEEE International Symposium on Circuits and Systems (ISCAS2005), pp.192-195, Kobe, May 24, (2005).
[IS-C-27] T. Yoshida, Y. Masui, T. Mashimo, M. Sasaki and A. Iwata, “A 1V Supply 50nV/√Hz Noise PSD CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization”, IEEE 2005 SYMPOSIUM ON VLSI CIRCUITS, Kyoto, June 16, (2005).
[IS-C-28] K. Korekado, T. Morie, O. Noura, T. Nakano, M. Matsugu and A. Iwata, “An Image Filtering Processor for Face/Object Recognition Using Merged/Mixed Analog-Digital Architecture”, IEEE 2005 SYMPOSIUM ON VLSI CIRCUITS, Kyoto, June 17, (2005).
[IS-C-29] D. Kosaka, M. Nagata, Y. Hiraoka, I. Imanishi, M. Maeda, Y. Murasaka and A. Iwata, “Isolation Strategy against Substrate Coupling in CMOS Mixed-Signal/RF Circuits”, IEEE 2005 SYMPOSIUM ON VLSI CIRCUITS, Kyoto, June 17, (2005).
[IS-C-30] M. Sasaki and A. Iwata, “A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip Interconnect with Asynchronous Communication Scheme”, IEEE 2005 SYMPOSIUM ON VLSI CIRCUITS, Kyoto, June 17, (2005).
[IS-C-31] M. Hori, M. Ueda and A. Iwata, “A stochastic computing chip for measurement of Manhattan distance”, Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, pp. 316-317, (2005).

論文リスト （マタウシュ, 小出グループ）

[MK-1] H.J. Mattausch, T. Gyohten, Y. Soda and T. Koide, “Compact Associative-Memory Architecture with Fully Parallel Search Capability for the Minimum Hamming Distance”, IEEE Journal of Solid-State Circuits, 37, 218-227, (2002).
[MK-2] S. Nakaya, T. Koide, S.Wakabayashi, “A VLSI floorplanning method based on an adaptive genetic algorithm”, The Transactions of Information Processing of Society Japan, Vol.43, No.5, pp.1361-1371, (2002). (in Japanese)
[MK-3] S. Yamasaki, S. Nakaya, S. Wakabayashi, and T. Koide, “A Performance-Driven Floorplanning Method with Interconnect Performance Estimation”, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E85-A, No.12, pp. 2775-2784, December, (2002).
[MK-4] S. Wakabayashi,.S. Koizumi, T. Koide, N. Imura, K. Fujiwara, “ A RISC Processor DLX-GA with Instruction Set Suitable for High-Speed Execution of a Genetic Algorithm”, The Transactions of Information Processing of Society Japan, Vol.44, No.2, pp.340-343, (2003). (in Japanese)
[MK-5] T. Sasaki, T. Inoue, N, Omori, T. Hironaka, H.J. Mattausch, and T. Koide, “Chip Size and Performance Evaluations of Shared Cache for On-chip Multiprocessors ”, IEICE Trans. on Information & Systems Part 1, vol. J87-D-I, 350-363 (2004).(in Japanese)
[MK-6] S. Fukae, T. Inoue, H.J. Mattausch, T. Koide, and T. Hironaka, “Distributed against centralized crossbar function for realizing bank-based multiport memories“, IEE Electronics Letters 40, 101-103, (2004).
[MK-7] K. Johguchi, Z. Zhu, T. Hirakawa, T. Koide, T. Hironaka, and H.J. Mattausch, “Distributed-crossbar architecture for area-efficient combined data/instruction caches with multiple ports ”, IEEE Electronics Letters 40, 160-162, (2004).
[MK-8] T. Morimoto, Y. Harada, T. Koide, and H.J. Mattausch, “Efficient Video-Picture Segmentation Algorithm for Cell Network-Based Digital CMOS Implementation ”, IEICE Trans. on Information & Systems, vol. E87-D, 500-503, (2004).
[MK-9] H. Noda, K. Inoue, M. Kuroiwa, F. Igaue, K. Yamamoto, H.J. Mattausch, T. Koide, A. Amo, A. Hachisuka, S. Soeda, F. Morishita, K. Dosaka, K. Arimoto, and T. Yoshihara, “A Cost-Efficient High-Performance Dynamic TCAM with Pipelined Hierarchical Searching and Shift Redundancy Architecture“, IEEE Journal of Solid-State Circuits, 40, 245-253, (2005).
[MK-10] T. Sasaki, T. Inoue, N, Omori, T. Hironaka, H.J. Mattausch, and T. Koide, “Chip Size and Performance Evaluations of Shared Cache for On-chip Multiprocessors”, Systems & Computers in Japan No. 36(9), 1-13, (2005).
[MK-11] H. Noda, K. Inoue, H.J. Mattausch, T. Koide, K. Dosaka, K. Arimoto, K. Fujishima, K. Anami, and T. Yoshihara, “Embedded Low-Power Dynamic TCAM Architecture with Transparently Scheduled Refresh ”, IEICE Trans. on Electronics, vol. E88-C, 622-629, (2005).
[MK-12] K. Inoue, H. Noda, K. Arimoto, H.J. Mattausch, and T. Koide, “A CAM-based signature-matching

co-processor with application-driven power-reduction features ", IEICE Trans. on Electronics, vol. E88-C, 1332-1342, (2005).

[MK-13] T. Inoue, T. Hironaka, T. Sasaki, S. Fukae, T. Koide, and H.J. Mattausch, "Evaluation of a Bank-based Multi-port Memory Architecture with Blocking Network ", IEICE Trans. on Fundamentals of Electronics, Communications and Computer Science, vol. J87-A, 498-510, (2005). (in Japanese)

[MK-14] T. Morimoto, Y. Harada, T. Koide, H.J. Mattausch, "Pixel-Parallel Digital-CMOS Implementation of Image Segmentation by Region Growing ", IEE Proc. Circuits, Devices & Systems , in press, (2006).

[MK-15] T. Morimoto, H. Adachi, O. Kiriyama, T. Koide, and H.J. Mattausch, "Boundary-Active-Only Adaptive Power Reduction Scheme for Region-Growing Video Segmentation", IEICE Trans. on Information & Systems, vol. E88-D, in press, (2006).

国際会議リスト(マタウシュ, 小出グループ)

[MK-C-1] H.J. Mattausch, N. Omori, S. Fukae, T. Koide and T. Gyohten, "Fully-Parallel Pattern-Matching Engine with Dynamic Adaptability to Hamming or Manhattan Distance", 2002 Symposium on VLSI Circuits Digest of Technical Papers, 252-255, (2002).

[MK-C-2] Y. Yano, T. Koide and H.J. Mattausch, "Fully Parallel Nearest Manhattan-Distance-Search Memory with Large Reference-Pattern Number", Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials (SSDM'2002), 254-255, (2002).

[MK-C-3] T. Koide, H.J. Mattausch, Y. Yano, T. Gyohten and Y. Soda, "A Nearest-Hamming-Distance Search Memory with Fully Parallel Mixed Digital-Analog Match Circuitry", Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2003), 591-592, Special Feature Award, University Design Contest, (2003).

[MK-C-4] T. Koide, Y. Yano, H. J. Mattausch, "An Associative Memory for Real-Time Applications Requiring Fully-Parallel Nearest Manhattan-Distance Search", 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2003), 200-205, (2003).

[MK-C-5] S. Fukae, N. Omori, T. Koide, H.J. Mattausch, T. Inoue and T. Hironaka, "Optimized Bank-Based Multi-Port Memories through a Hierarchical Multi-Bank Structure", 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2003), 323-330, (2003).

[MK-C-6] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, High Access Bandwidth Multi-Port-Cache Design with Compact Hierarchical 1-Port-Bank Structure, 11th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2003), 394-400, (2003).

[MK-C-7] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, "High-Speed and Low-Power Multi-Port-Cache", Proceedings of COOL Chips VI, 76, (2003).

[MK-C-8] H. Noda, K. Inoue, H.J. Mattausch, T. Koide and K. Arimoto, "A Cost-Efficient Dynamic Ternary CAM in 130nm CMOS Technology with Planar Complementary Capacitors and TSR Architecture", 2003 Symposium on VLSI Circuits Digest of Technical Papers, 83-84, (2003).

[MK-C-9] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, T. Hirakawa and T. Hironaka, "A Novel Hierarchical Multi-Port Cache", Proceedings of the 29th European Solid-State Circuits Conference (ESSCIRC'2003), Estoril, Portugal, September 16-18, 405-408, (2003).

[MK-C-10] T. Sueyoshi, H. Uchida, Y. Mitani, K. Hiramatsu, H.J. Mattausch, T. Koide, and T. Hironaka, "Bank-Type Multiport Register File for Highly-Parallel Processors", Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.400-401, (2003).

[MK-C-11] K. Johguchi, Z. Zhu, T. Hirakawa, T. Koide, T. Hironaka, and H.J. Mattausch, Combined Data/Instruction Cache with Bank-Based Multi-Port Architecture, Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.152-153, (2003).

[MK-C-12] S. Fukae, N. Omori, T. Koide, H.J. Mattausch, and T. Hironaka, "A Hierarchical 512-Kbit SRAM with 8 Read/Write Ports in 130nm CMOS", Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM'2003), pp.150-151, (2003).

[MK-C-13] T. Sueyoshi, H. Uchida, Y. Mitani, K. Hiramatsu, H.J. Mattausch, T. Koide, and T. Hironaka, "Compact 12-Port Multi-Bank Register File Test Chip in 0.35mm CMOS for Highly Parallel Processors", Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2004), pp.551-552, (2004).

[MK-C-14] Y. Yano, T. Koide, and H.J. Mattausch, "Associative Memory with Fully Parallel Nearest-Manhattan-Distance Search for Low-Power Real-Time Single-Chip Applications", Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC'2004), pp.

543-544, (2004).

[MK-C-15] H. Noda, K. Inoue, M. Kuroiwa, A. Amo, A. Hachisuka, H.J. Mattausch, T. Koide, S. Soeda, K. Dosaka, and K. Arimoto, "A 143MHz, 1.1W, 4.5Mb dynamic TCAM with hierarchical searching and shift redundancy architecture", IEEE International Solid-State Circuits Conference Digest of Tech. Papers (ISSCC'2004), pp.208-209, (2004).

[MK-C-16] T. Inoue, T. Hironaka, T. Sasaki, S. Fukae, T. Koide, H.J. Mattausch, "Proposition and Evaluation of a Bank-Based Multi-Port Memory with Blocking Network", Proceedings of the 2004 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC'2004), 6C2L-3, (2004).

[MK-C-17] Z. Zhu, K. Johguchi, H.J. Mattausch, T. Koide, and T. Hironaka, "Low Power Bank-based Multi-port SRAM Design due to Bank Standby Mode", Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2004) Vol. I, 569-572, (2004).

[MK-C-18] Y. Shirakawa, H.J. Mattausch, and T. Koide, "Reference-Pattern Learning and Optimization from an Input-Pattern Stream for Associative-Memory-Based Pattern-Recognition System", Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2004) Vol. I, 561-564, (2004).

[MK-C-19] K. Kamimura, K. M. Rahman, H.J. Mattausch, and T. Koide, "Optimized Multi-Stage Minimum-Distance-Search Circuit with Feedback Stabilization for Fully-Parallel Associative Memories", Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2004) Vol. I, 161-164, (2004).

[MK-C-20] K. Takemura, T. Koide, H.J. Mattausch, and T. Tsuji, "Analog-Circuit-Component Optimization with Genetic Algorithm", Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2004) Vol. I, 489-492, (2004).

[MK-C-21] Y. Shirakawa, M. Mizokami, T. Koide and H.J. Mattausch, "Automatic Pattern-Learning Architecture Based on Associative Memory and Short/Long Term Storage Concept", Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials (SSDM'2004), 362-363, (2004).

[MK-C-22] T. Koide, Y. Yano and H.J. Mattausch, "Bank-Type Associative Memory for High-Speed Nearest Manhattan Distance Search in Large Reference-Pattern Space", Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials (SSDM'2004), 360-361, (2004).

[MK-C- 23] T. Fuji, K. Kobayashi, T. Koide, H.J. Mattausch and T. Hironaka, "Highly Efficient Switch Architecture Based on Banked Memory with Multiple Ports", 12th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI'2004), 491-498, (2004).

[MK-C-24] A. Ahmadi, H.J. Mattausch, T. Koide, "A Numerical Approach for Snake Models and Implementation with an FPGA Architecture", Proceedings of the Annual Workshop on Circuits, Systems and Signal Processing (ProRISC'2004), 1-6, (2004).

[MK-C-25] T. Saito, M. Maeda, T. Hironaka, K. Tanigawa, T. Sueyoshi, K. Aoyama, T. Koide, and H.J. Mattausch, "Design of Superscalar Processor with Multi-Bank Register File", Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS'05), Kobe 2005, 3507-3510, May, (2005).

[MK-C-26] T. Kumaki, Y. Kuroda, T. Koide, H.J. Mattausch, H. Noda, K. Dosaka, K. Arimoto, and K. Saito, "CAM-based VLSI Architecture for Huffman Coding with Real-time Optimization of the Code Word Table", Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS'05), Kobe 2005, 5202-5205, May, (2005)

[MK-C-27] A. Ahmadi, H.J. Mattausch, and T. Koide, "A Parallel Hardware Design for Snake Models with an FPGA Architecture", International Workshop on Nonlinear Signal and Image Processing (NSIP'2005), 146-150, May, (2005).

[MK-C-28] T. Kumaki, Y. Kuroda, T. Koide, H.J. Mattausch, H. Noda, K. Dosaka, K. Arimoto, and K. Saito, "Multi-Port CAM based VLSI Architecture for Huffman Coding with Real-time Optimized Code Word Table", Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2005), 55-58, Aug, (2005).

[MK-C-29] A. Ahmadi, Y. Shirakawa, Md. A. Abedin, K. Kamimura, H.J. Mattausch, and T. Koide, "An LSI hardware design for online character recognition using associative memory", Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'2005), 464-467, Aug, (2005)

[MK-C-30] A. Ahmadi, Md. A. Abedin, H.J. Mattausch, and T. Koide, "A Parallel Hardware Design for Parametric Active Contour Models", Proceedings of the IEEE International Conference on Advanced

Video and Signal based Surveillance (AVSS‘2005), 609-613, Sep, (2005).
[MK-C-31] Y. Kuroda, T. Kumaki, T. Koide, H.J. Mattausch, H. Noda, K. Dosaka, K. Arimoto, and K. Saito, “Highly Parallel Huffman Encoding by Exploiting Multiple Matches in Content Addressable Memory”, Proceedings of the International SoC Design Conference (ISOCC’2005), 313-316, Nov, (2005).
[MK-C-32] T. Koide, T. Morimoto, Y. Harada, H.J. Mattausch, “Digital Gray-Scale/Color Image-Segmentation Architecture for Cell-Network-Based Real-Time Applications”, Proceedings of the 2002 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC‘2002), 670-673, (2002).
[MK-C-33] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, “Real-Time Segmentation Architecture of Gray-Scale/Color Motion Pictures and Digital Test-Chip Implementation”, Proceedings of the 2002 IEEE Asia-Pacific Conference on ASICs (AP-ASIC‘2002), 237-240, (2002).
[MK-C-34] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, Low-Complexity, “Highly-Parallel Color Motion-PicturebSegmentation Architecture for Compact Digital CMOS Implementation”, Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials (SSDM’2002), 242-243, (2002).
[MK-C-35] Y. Harada, T. Morimoto, T. Koide, H.J. Mattausch, “CMOS Test Chip for a High-Speed Digital Image Segmentation Architecture with Pixel-Parallel Processing”, Proceedings of the 2003 International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC‘2003), 284-287, (2003).
[MK-C-36] T. Morimoto, Y. Harada, T. Koide and H.J. Mattausch, “Low-Power Real-Time Region-Growing Image Segmentation in 0.35mm CMOS due to Subdivided-Image and Boundary-Active-Only Architectures”, Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials (SSDM’2003), 146-147, (2003).
[MK-C-37] T. Morimoto, Y. Harada T. Koide, and H.J. Mattausch, “350nm CMOS Test-Chip for Architecture Verification of Real-Time QVGA Color-Video Segmentation at the 90nm Technology Node”, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC‘2004), 531-532, (2004),
[MK-C-38] O. Kiriyama, T. Morimoto, H. Adachi, Y. Harada, T. Koide and H.J. Mattausch, “Low-Power Design for Real Time Image Segmentation LSI and Compact Digital CMOS Implementation”, Proceedings of the 2004 IEEE Asia Pacific Conference on ASICs (AP-ASIC‘2004), 432-433, (2004).
[MK-C-39] T. Morimoto, O. Kiriyama, H. Adachi, T. Koide and H.J. Mattausch, “Digital Low-Power Real-Time Video Segmentation by Region Growing”, Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials (SSDM’2004), 138-139, (2004).
[MK-C-40] H. Adachi, T. Morimoto, O. Kiriyama, T. Koide and H.J. Mattausch, “Real-Time Segmentation of Large-Scale Images by Pipeline Processing with Small-Size Cell Network”, 12th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI’2004), 95-102, (2004).
[MK-C-41] T. Morimoto, O. Kiriyama, H. Adachi, Z. Zhu, T. Koide, and H.J. Mattausch, “A Low-Power Vide SegmentationbLSI with Boundary-Active-Only Architecture”, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC‘2005.1), D13-D14, Best Design Award, (2005).
[MK-C-42] T. Morimoto, O. Kiriyama, Y. Harada, H. Adachi, T. Koide, and H.J. Mattausch, “Object Tracking in Video Pictures based on Image Segmentation and Pattern Matching”, Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS’05), Kobe 2005, 3215-3218, May, (2005).
[MK-C-43] H. Adachi, T. Morimoto, K. Yamaoka, T. Koide, and H.J. Mattausch, “Image-Scan Architecture for Efficient FPGA/ASIC Implementation of Video-Segmentation by Region Growing”, Proceedings of the International SoC Design Conference (ISOCC’2005), 301-304, Nov, (2005).
[MK-C-44] K. Yamaoka, T. Morimoto, H. Adachi, T. Koide, and H.J. Mattausch, “Image Segmentation and Patter Matching Based FPGA/ASIC Implementation of Real-Time Object Tracking”, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC‘2006.1), in press, Jane, (2006).
[MK-C-45] H. Kubota, S. Wakabayashi, and T. Koide, “A Hierarchical Placement Method for Standard Cell Layout Base on Wire Length Driven Clustering”, Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS‘2004), in press, (2004).

論文リスト （三浦, 江崎グループ）

[ME-1] T. Okagaki, M.Tanaka, H.Ueno, and M. Miura-Mattausch, “Importance of ballistic carriers for the dynamic response in sub-100nm MOSFETs”, IEEE Electron Device Letters, Vol. 23, No. 3, pp. 154-156, (2002).

[ME-2] M. Miura-Mattausch, “The 100nm-MOSFET model HiSIM and its extension to RF applications”, Int. Sym. Quality Electronic Design, (2002).
[ME-3] H. J. Mattausch, M. Suetake, D. Kitamaru, M. Miura-Mattausch, S. Kumashiro, N. Shigyo, S. Odanaka, and N. Nakayama, “Simple nondestructive extraction of the vertical channel-impurity profile of small-size metal-oxide semiconductor field-effect transistors”, Appl. Phys. Letters, Vol. 80, No. 16, pp. 2994-2996, (2002).
[ME-4] H. Ueno, M. Tanaka, K. Morikawa, T. Takahashi, M. Miura-Mattausch, and Y. Ohmura, “Origin of transconductance oscillations in silicon-on-insulator metal-oxide-semiconductor field-effect transistors with an ultrathin 6-nm-thick active Si layer”, J. Appl. Phys., Vol. 91, No. 8, pp. 5360-5364, (2002).
[ME-5] H. Ueno, M. Tanaka, K. Morikawa, T. Takahashi, M. Miura-Mattausch, and Y. Ohmura, “Evidence of mesoscopic carrier transport in SOI-MOSFETs with ultra-thin active Si-layer”, Physica B, Vol. 314, pp. 367-371, (2002).
[ME-6] M. Miura Mattausch, H. Ueno, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “HiSIM: self-consistent surface-potential MOS-Model valid down to sub-100nm technologies”, Proc. Modeling and Simulation of Microsystems, pp. 678-681, (2002).
[ME-7] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Circuit simulation models for coming MOSFET generations”, IEICE Trans. Fund. Electron., Vol. E85-A, No. 4, pp. 740-748, (2002).
[ME-8] K. Morikawa, H. Ueno, D. Kitamaru, M. Tanaka, T. Okagaki, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Quantum effect in sub-0.1μm MOSFET with pocket technologies and its relevance for the on-current condition”, Jpn. J. Appl. Phys., Vol. 41, No. 4B, pp. 2359-2362, (2002).
[ME-9] H. Kawano, M. Nishizawa, S. Matsumoto, S. Mitani, M. Tanaka, N. Nakayama, H. Ueno, M. Miura-Mattausch, and H. J. Mattausch, “A practical small-signal equivalent circuit model for RF-MOSFETs valid up to the cut-off frequency”, IEEE Int. Microwave Sym. Digest, pp. 2121-2124, (2002).
[ME-10] 三浦道子、上野弘明, “デバイスモデルと回路シミュレーション (Device model and its applications for circuit simulation)”, 応用物理 基礎講座第 71 巻, pp. 726-730, (2002).
[ME-11] S. Jinbou, H. Ueno, H. Kawano, K. Morikawa, N. Nakayama, M. Miura-Mattausch, and H. J. Mattausch, “Analysis of non-quasistatic contribution to small-signal response for deep sub-μm MOSFET technologies”, Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 26-27, (2002).
[ME-12] N. Nakayama, H. Ueno, T. Isa, M. Tanaka, and M. Miura-Mattausch, “A self-consistent non-quasi static MOSFET model for circuit simulation based on transient carrier response”, Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 408-409, (2002).
[ME-13] D. Navarro, K. Hisamitsu, T. Yamaoka, M. Tanaka, H. Kawano, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Circuit-simulation model of gate drain-capacitance changes in small-size MOSFETs due to high channel-field gradient”, Proc. Int. Conf. Simulation Semicon. Processes & Devices, pp. 51-54, (2002).
[ME-14] H. Ueno, S. Jinbou, H. Kawano, K. Morikawa, N. Nakayama, M. Miura-Mattausch, and H. J. Mattausch, “Drift-diffusion-based modeling of the non-quasistatic small-signal response for RF-MOSFET applications”, Proc. Int. Conf. Simulation Semicon. Processes & Devices, pp. 71-74, (2002).
[ME-15] 三浦道子、上野弘明, “高速デバイスを用い過渡解析に要求される輸送記述 (Carrier transport descripti on required for transient analysis of RF-Devices)”, STARC シンポジウム講演予稿集, pp. 39-48, (2002).
[ME-16] M. Miura-Mattausch, “HiSIM: MOSFET-model for circuit simulation with self-consistent surface potential”, Fabless-Semiconductor-Association Meeting, (2002).
[ME-17] H. Ueno,D. Kitamaru, K. Morikawa, M. Tanaka, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Impurity-profile-based threshold-voltage model of pocket implanted MOSFETs for circuit simulation”, IEEE Transactions on Electron Devices, Vol. 49,No. 10, pp. 1783-1789, (2002).
[ME-18] S. Matsumoto, K. Hisamitsu, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, S. Odanaka, and N. Nakayama, “Validity of mobility universality for scaled metal-oxide semiconductor field-effect transistors down to 100nm gate length”, J. Appl. Phys., Vol. 92, No. 9, pp. 5228-5232, (2002).

[ME-19] M. Miura Mattausch, H. Ueno, M. Tanaka, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “HiSIM: A MOSFET model for circuit simulation connecting circuit performance with technology”, Tech. Digest Int. Electron Devices Meeting, pp. 109-112, (2002).
[ME-20] K. Hisamitusu, H. Ueno, M. Tanaka, D. Kitamaru, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Temperature-Independence-Point Properties for 0.1μm-Scale Pocket-Implant Technologies and the Impact on Circuit Design”, Proc. Of Asia and South Pacific Design Automation Conference, pp. 179-183, (2003).
[ME-21] M. Miura-Mattausch, D. Navarro, H. Ueno, S. Jinbou, H, J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, “HiSIM: Accurate charge modeling important for RF era”, Proc. Modeling and Simulation of Microsystems, Vol. 2, pp. 258-261, (2003).
[ME-22] Q. Ngo, D. Navarro, T. Mizoguchi, S. Hosokawa, H. Ueno, M. Miura-Mattausch, and C. Y. Yang, Proc. Modeling and Simulation of Microsystems, “Gate current partitioning in MOSFET models for circuit simulation”, Vol. 2, pp. 322-325, (2003).
[ME-23] M. Tanaka, H. Ueno, O. Matsushima, and M. Miura-Mattausch, “High-electric-field electron transport at silicon/ silicon-dioxide interface inversion layer”, Jpn. J. Appl. Phys., Vol. 42, No. 3B, pp. L280-282, (2003).
[ME-24] D. Navarro, H. Kawano, K. Hisamitsu, T. Yamaoka, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Circuit-simulation model of Cgd changes in small-size MOSFETs due to high channel-field gradients”, IEICE Transactions on Electronics, Vol. E86-C, No. 3, pp. 474-480, (2003).
[ME-25] T. Mizoguchi, H. J. Mattausch, H. Ueno, D. Kitamaru, K. Hisamitsu, M. Miura-Mattausch, S. Itoh, and K. Morikawa, “Extraction of inter-and intra-chip device-parameter variations with a differntial-amplifier-stage test circuit”, SASIMI 2003 Proceedings(1-8), pp. 76-82, (2003).
[ME-26] N. Nakayama, H. Ueno, T. Inoue, T. Isa, M. Tanaka, and M. Miura-Mattausch, “A self-consistent non-quasi static MOSFET model for circuit simulation based on transient carrier response”, Jpn. J. Appl. Phys., Vol. 42, No. 4B, pp. 2132-2136, (2003).
[ME-27] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, “100nm-MOSFET model for circuit simulation: challenges and solutions”, IEICE Transactions on Electronics, Vol. E86C, No. 6, pp. 1009-1021, (2003).
[ME-28] S. Ito, K. Morikawa, A. Kobayashi, H. Masuda, S. Fujimoto, T. Mizoguchi, H. Ueno, and M. Miura-Mattausch, “Parameter exteaction of HiSIM 1.1/ HiSIM 1.2” DA シンポジウム 2003 論文集, Vol. 2003, No.11, pp. 247-252, (2003).
[ME-29] O. Matsushima, M. Tanaka, H. Ueno, K. Hara, K. Konno, and M. Miura-Mattausch, “Carrier transport in highly generated carrier concentration,” Proc. Int. Conf. Nonequilibrium Carrier Dynamics in Semicnoductors, pp. PTu4-8, (2003).
[ME-30] S. Hosokawa, Y. Shiraga, H. Ueno, M. Miura Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, H. Masuda, and S. Miyamoto, “Origin of enhanced thermal noise for 100nm-MOSFETs”, Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 20-21, (2003).
[ME-31] D. Kitamaru, Y. Uetsuji, and M. Miura-Mattausch, “A complete surface-potential-based SOI-MOSFET model for circuit simulation”, Ext. Abs. Int. Conf. Solid-State Devices and Materials, pp. 622-623, (2003).
[ME-32] H. Ueno, S. Matsumoto, S. Hosokawa, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, “Modeling of $1/f$ Noise with HiSIM for 100nm CMOS technology”, Proc. On the 1st Intetnational Workshop on Compact Medeling, pp. 18-23, (2004).
[ME-33] M. Miura-Mattausch, “MOSFET modeling for RF-CMOS design”, Proc. Asia and South Pacific Design Automation Conference 2004, 6A-1, pp. 482-490, (2004).
[ME-34] K. Konno, O. Matsushima, D. Navarro, and M. Miura-Mattausch, “Limit of validity of the drift-diffusion approximation for simulation of photodiode characteristics”, Appl. Phys. Letters, Vol. 84, No. 8, pp. 1398-1400, (2004).
[ME-35] N. Nakayama, D. Navarro, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, T. Kage, and S. Miyamoto,“Non-quasi-static model for MOSFET based on carrier-transit delay”, IEEE Electronics Letters, Vol. 40, No. 4, pp. 276-278, (2004).
[ME-36] M. Miura-Mattausch, S. Hosokawa, D. Navarro, S. Matsumoto, H. Ueno, H. J. Mattausch, T. Ohguro, T. Iizuka, T. Taguchi, and S. Miyamoto, “Noise modeling with HiSIM based on self-consistent surface-potential description”, Nanotech 2004 Conference Technical Proc., Vol. 2, pp. 66-69, (2004).

[ME-37] M. Miura-Mattausch, S. Matsumoto, K. Mizoguchi, D. Miyawaki, H. J. Mattausch, S. Itoh, and K. Morikawa, “Test circuits for extracting sub-100nm MOSFET technology variations with the MOSFET model HiSIM”, Proc. IEEE 2004 Int. Conference on Microelectronic Test Structures, Vol. 17, No. 9. 1, pp. 267-272. (2004).
[ME-38] O. Matsushima, K. Konno, M. Tanaka, K. Hara, and Miura-Mattausch, “Carrier transport in highly generated carrier concentration”, Semiconductor science and technology, Vol. 19, No. 4, pp. 185-187, (2004).
[ME-39] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch, “Complete surface-potential-based fully depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistor model for circuit simulation”, Jpn. J. Appl. Phys., Vol. 43, No. 4B, pp. 2166-2169, (2004).
[ME-40] 村川正宏、樋口哲也、和田哲典、小田嘉則、馬場俊祐、遠藤伸裕、三浦道子、芝原健太郎、西謙二、伊藤桂一，“高騰するプロセス開発コストを新しいモデル探索手法で削減”，NIKKEI MICRODEVICES, pp. 51-58, (2004).
[ME-41] M. Miura-Mattausch, D. Navarro, Y. Takeda, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Miyamoto, “MOSFET modeling for RF-circuit era”, Proc. of the 11th Int. Conference on Mixed Design of Integrated Circuits and Systems 2004, pp. 62-66, (2004).
[ME-42] N. Sadachika, Y. Uetsuji, D. Kitamaru, H. J. Mattausch, M. Miura-Mattausch, L. Weiss, U. Feldmann, and S. Baba, “Fully-depleted SOI-MOSFET model for circuit simulation and its application to $1/f$ Noise analysis”, Proc. Int. Conf. Simulation Semiconductor Processes & Devices (Munich), pp. 255-258, (2004).
[ME-43] D. Navarro, N. Nakayama, K. Machida, Y. Takeda, S. Chiba, H. Ueno, H. J. Mattausch, M. Miura-Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, and S. Miyamoto, “Modeling for carrier transport dynamics at GHz Frequencies for RF circuit-simulation”, Proc. Int. Conf. Simulation Semiconductor Processes & Devices (Munich), pp. 259-262, (2004).
[ME-44] M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, “MOSFET modeling for RF-circuit simulation,” Proc. of the 2004 Int. Conference on Solid-State and Integrated Circuit Technology (Beijing), pp. 1188-1122, (2004).
[ME-45] K. Konno, O. Matsushima, D. Navarro, and M. Miura-Mattausch, “High frequency response of *p-i-n* photodiodes analyzed by an analytical model in Fourier space” Journal of Applied Physics. Vol. 96. No. 7, (2004).
[ME-46] K. Konno, O. Matsushima, K. Hara, G. Suzuki, D. Navarro, and M. Miura-Mattausch, “Carrier transport model for lateral *p-i-n* photodiodes at high-frequency operation,” Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, pp 946-947, (2004).
[ME-47] K. Hara, O. Matsushima, G. Suzuki, D. Navarro, K. Konno, Y. Isobe, and M. Miura-Mattausch, “Shot noise measurement in p-i-n diode and its analysis,” Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, pp. 438-439, (2004).
[ME-48] M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, “MOSFET model HiSIM based on surface-potential description for enabling accurate RF-CMOS design,” Journal of Semiconductor Technology and Science, Vol. 4, No. 3, pp. 133-140, (2004).
[ME-49] M. Murakawa, M. Miura-Mattausch, T. Higuchi, “Towards automatic parameter extraction for surface potential based MOSFET models with the genetic algorithm,” Asia and South Pacific Design Automation Conference 2005, pp. 204-207, (2005).
[ME-50] M. Murakawa, M. Miura-Mattausch, S. Mimura, T. Higuchi, “Genetic algorithm for reliable parameter extraction of complete surface-potential-based models,” The 2nd International Workshop on Compact modeling, pp. 7-12, (2005).
[ME-51] D. Navarro, N. Nakayama, K. Machida, Y. Takeda, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, and S. Miyamoto, “A carrier transit time delay-based non-quasi-static MOSFET model for RF circuit simulation,” The 2nd International Workshop on Compact modeling, pp. 23-27, (2005).
[ME-52] S. Matsumoto, H. Ueno, S. Hosokawa, T. Kitamura, M. Miura-Mattausch, H. J. Mattausch, T. Ohguruo, S. Kumashiro, T. Yamaguchi, K. Yamashita, N. Nakayama, “1/f-noise characteristics in 100nm-MOSFETs and its modeling for circuit simulation,” IEICE Transactions on Electronics, Vol. E88-C, No. 2, pp. 247-254, (2005).

[ME-53] K. Konno, O. Matsushima, K. Hara, G. Suzuki, D. Navarro and M. Miura-Mattausch, "Carrier transport model for lateral *p-i-n* photodiode in high-frequency operation," J. J. A. P., Vol. 44, No. 4B, pp. 2584-2585, (2005).
[ME-54] D. Navarro, T. Mizoguchi, M. Suetake, K. Hisamitsu, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "A compact model of the pinch-off region of 100nm MOSFETs based on the surface-potential," IEICE Transactions on Electronics, Vol. E88-C, No. 5, pp.1079-1086, (2005).
[ME-55] N. Sadachika, M. Md Yusoff, Y. Uetsuji, M. H. Bhuyan, D. Kitamaru, H. J. Mattausch, M. Miura-Mattausch, L. Weiss, U. Feldmann, S. Baba, "The surface-potential-based model HiSIM-SOI and its application to 1/*f* noise in fully-depleted SOI-MOSFET," Modeling and Simulation of Microsystems 05, pp. 155-158, (2005).
[ME-56] M. Miura-Mattausch, N. Sadachika, M. Murakawa, S. Mimura, T. Higuchi, K. Itoh, R. Inagaki, and Y. Iguchi, "RF-MOSFET model-parameter Extraction with HiSIM," Modeling and Simulation of Microsystems 05, pp.69-74, (2005).
[ME-57] Josef Watts (editor), Colin McAndrew (presenteor), Christian Enz, Carlos Galup-Montoro, Gennady Gildenblat, Chenming Hu, Ronald van Langevelde, Mitiko Miura-Mattausch, Rafael Rios, Chih-Tang Sah, "Advanced compact models for MOSFETs," Modeling and Simulation of Microsystems 05, pp. 3-12, (2005).
[ME-58] T. Ezaki, D. Navarro, Y. Takeda, N. Sadachika, G. Suzuki, M. Miura-Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, S. Miyamoto, "Non-quasi-static analysis with HiSIM, a complete surface-potential-based MOSFET model," MIXDES 2005, pp. 923-928, (2005).
[ME-59] S. Hosokawa, D. Navarro, M. Miura-Mattausch, and H. J. Mattausch, "Gate-length and drain-voltage dependence of thermal drain noise in advanced metal-oxide-semiconductor-field effect transistors, " Appl. Phys. Letters 87, (2005).
[ME-60] M. Miura-Mattausch, "MOSFET modeling beyond 100nm technology: Challenges and perspectives", SISPAD 2005, (2005).
[ME-61] G. Suzuki, K. Konno, D. Navarro, N. Sadachika, Y. Mizukane, O. Matsushima and M. Miura-Mattausch, "Time-domain-based modeling of carrier transport in lateral p-i-n photodiode", SISPAD 2005, (2005).
[ME-62] Y. Takeda, D. Navarro, S. Chiba, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "MOSFET harmonic distortion analysis up to the non-quasi-static frequency regime", IEEE 2005 Custom Integrated Circuits Conference, pp. 827-830, (2005).
[ME-63] 三浦道子、名野隆夫、盛健次, "回路シミュレーション技術と MOSFET モデリング (Circuit-simulation technics and MOSFET modeling)", Sipec, (2003).

論文リスト(角南グループ)

[Su-1] K. Itoh, H. Sunami, K. Nakazato, and M. Horiguchi, " Pathways to DRAM Design and Technology for the 21st Century ", the 193rd Electrochemical Society Spring Meeting, Abs. No. 303, San Diego, California, May 3-8, 1998; Proceedings of the 8th Internat. Symp. Silicon Materials Science and Technology, Volume 98-1, pp. 350-369, 1998.
[Su-2] 角南英夫, 鈴木道夫,「次世代集積回路と製造ライン-今後のデバイス展望と 300mm ウェハ製造ラインの動向 」, エアロゾル研究, 第 14 巻, 第 1 号, pp. 11-18, (1999).
[Su-3] T. Furukawa, H. Yamashita, and H. Sunami, "A Proposal of Corrugated-Channel Transistor (CCT) with Vertically Formed Channels for Area-Conscious Applications ", Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2067-2072, April, (2003).
[Su-4] A. Takase, T. Kidera, and H. Sunami, "Field-Shield Trench Isolation with Self-Aligned Field Oxide," Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2100-2105, April, (2003).
[Su-5] 角南英夫,「ULSI の将来展望と高分子材料への期待」, 高分子, 第 52 巻, 8 月号, pp. 546-550, (2003).
[Su-6] H. Sunami, T. Furukawa, and T. Masuda, "A Three-Dimensional MOS Transistor Formation Technique with Crystallographic Orientation-Dependent TMAH Etchant ", SENSORS and ACTUATORS A: PHYSICAL, A111, pp. 310-316, (2004).
[Su-7] A. Katakami, K. Kobayashi, and H. Sunami, "A High-Aspect Ratio Silicon Gate Formation Technique for Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation ", Jpn. J. Appl. Phys., Vol. 43,

No. 4B, pp. 2145-2150, April, (2004).
[Su-8] K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara, and H. Sunami, "Application of Arsenic Plasma Doping in Three Dimensional MOS Transistors and the Doping Profile Evaluation ", Jpn. J. Appl. Phys., Vol. 44, No. 4B, pp. 2273-2278, April, (2005).

国際会議リスト(角南グループ)

[Su-C-1] K. Itoh, H. Sunami, K. Nakazato, and M. Horiguchi, " Pathways to DRAM Design and Technology for the 21st Century ", the 193rd Electrochemical Society Spring Meeting, Abs. No. 303, San Diego, California, May 3-8, 1998.
[Su-C-2] H. Sunami, " Pathways to Giga-scale Electronics for the 21st Century ", Seventh Hitachi Cambridge Seminar, Cambridge, July 6, (1998).
[Su-C-3] H. Sunami, T. Furukawa, and T. Masuda, " Orientation-Dependent Anisotropic TMAH Etchant Applied to 3-D Silicon Nanostructure Formation ", Proc. Pacific Rim Workshop on Transducers and Micro/nano Technologies, pp. 367-372, Xiamen, July 22-24, (2002).
[Su-C-4] T. Furukawa, H. Yamashita, and H. Sunami, " Corrugated-Channel Transistor (CCT) for Area-Conscious Applications ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. A-3-2, pp. 139-140, Nagoya, Sept. 17-19, (2002).
[Su-C-5] A. Takase, T. Kidera, and H. Sunami, " Field-Shield Trench Isolation with Self-Aligned Field Oxide ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. A-7-4, pp. 694-695, Nagoya, Sept. 17-19, (2002).
[Su-C-6] A. Katakami, K. Kobayashi, and H. Sunami, " High-Aspect Ratio gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced oxidation of Silicon Gate ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. D-5-2, pp. 282-283, Tokyo, Sept. 16-18, (2003).
[Su-C-7] K. Kobayashi, T. Eto, K. Okuyama, K. Shibahara, and H. Sunami, " An Impurity-Enhanced Oxidation Assisted Doping Profile Evaluation for Three-Dimensional and Vertical-Channel Transistors ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. B-6-3, pp. 208-209, Tokyo, Sept. 15-17, (2004).
[Su-C-8] M. Kawai, K. Endo, T. Tabei, and H. Sunami, " An Experimental Analysis of 1.55-mm Infrared Light Propagation in Integrated SOI Structure ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. P7-1, pp. 556-557, Tokyo, Sept. 15-17, (2004).
[Su-C-9] H. Sunami, K. Kobayashi, and S. Matsumura, " Integrated Power Transistor Application of Three-Dimensional Sidewall Channel MOS Transistor (invited) ", Proc. the 7th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT 2004), Abs. No. A7.3, pp. 336-339, Beijin, China, Oct. 18-21, (2004).
[Su-C-10] H. Sunami, " Recent Activities for Nano-device and Process Technology Development in the 21st COE: Nanoelectronics for Terabit Information Processing ", Tech. Dig. 2004 International Symposium on Nano Science and Technology, pp. 3-8, Tainan, Taiwan, Nov. 20-21, (2004).
[Su-C-11] T. Tabei, K. Maeda, S. Yokoyama, and H. Sunami, " Fabrication of spin-coat opticl waveguides for optically interconnected LSI and influence of fabrication process on lower layer MOS capacitors ", Extended Abstracts of International Symp. on Solid State Devices and Materials, Abs. No. E-4-4, pp. 332-333, Tokyo, Sept. 13-15, (2004).
[Su-C-12] H. Sunami and K. Okuyama, " High-Aspect-Ratio Structure Formation Techniques for Three-Dimensional Metal-Oxide Semiconductor Transistors ", Abstract of 31st International Conference on Micro- and Nano-Engineering, No. 11B_03, Sept. 19-22, Vienna, Austria, (2005).

論文リスト(芝原グループ)

[Sh-1] K. Shibahara, " Ultra-Shallow Junction Formation with Antimony Implantation ", IEICE Trans. Electron., Vol. E.85 C, pp. 1091-1097, (2002). (Invited)
[Sh-2] D. Notsu, N. Ikechi, Y. Aoki, N. Kawakami, and K. Shibahara, " Fabrication of 100 nm Width Fine Active-Region Using LOCOS Isolation ", IEICE Trans. Electron., Vol. E.85-C, pp. 1119-1123, (2002).
[Sh-3] K. Shibahara, D. Onimatsu, Y. Ishikawa, T. Oda, and T. Kikkawa, " Copper Drift in Low Dielectric Constant Insulator Films Caused by O2+ Primary Ion Beam ", Appl. Surf. Sci., Vol. 203-204, pp. 387-390, (2002).
[Sh-4] K. Imai, S. Shishiguchi, K. Shibahara and S. Yokoyama, " Phosphorus-Assisted Low-Energy Arsenic

Implantation Technology for N-Channel Metal-Oxide-Semiconductor Field-Effect Transistor Source/Drain Formation Process ", Jpn. J. Appl. Phys., Vol. 42, No. 5A, pp. 2654-2659, (2003).
[Sh-5] S. Nakamura, M. Itano, H. Aoyama, K. Shibahara1, S. Yokoyama and M. Hirose, " Comparative Studies of Perfluorocarbon Alternative Gas Plasmas for Contact Hole Etch ", Jpn. J. Appl. Phys., Vol. 42, No. 9A, pp. 5759-5764, (2003).
[Sh-6] T. Eto and K. Shibahara, " Accuracy of SIMS Depth Profiling for Sub-keV As+ Implantation ", Jpn. J. Appl. Phys. Part 1. Vol.44, No.4B, pp. 2433-2436, (2005).
[Sh-7] E. Takii, T. Eto, K. Kurobe, and K. Shibahara, " Ultra Shallow Junction Formation by Green-Laser Annealing with Light Absorber ", Jpn. J. Appl. Phys. Part 2. Letter, Vol.44, No.24, pp. L756-L759, (2005).
[Sh-8] K. Sano, M. Hino, N. Ooishi, and K. Shibahara, "Workfunction Tuning Using Various Impurities for Fully Silicided NiSi ", Jpn. J. Appl. Phys. Part 1. Vol.44, No.6A, pp. 3774-3777, (2005).
[Sh-9] A. Matsuno, E. Takii, T. Eto, K. Kurobe, and K. Shibahara, " Merits and Demerits of Light Absorbers for Ultra Shallow Junction Formation by Green Laser Annealing ", Nucl. Instr. and Meth. B (NIM-B), Vol. 237, pp. 136-141, (2005).
[Sh-10] K. Kurobe, Y. Ishikawa and K. Shibahara, "Sheet Resistance Reduction and Crystallinity Improvement inultrashallow n+/p Junctions by Heat-Assisted Excimer Laser Annealing", Jpn. J. Appl. Phys, Vol. 44, No. 12, pp. 8391-8395, (2005).

国際会議リスト(芝原グループ)

[Sh-C-1] T. Amada, N. Maeda, and K. Shibahara, "Degradation in a Molybdenum-Gate MOS Structure Caused by N+ Ion Implantation for Work Function Control ", Mat. Res. Soc. Symp. Proc. Vol. 716, pp. 299-314, (2002).
[Sh-C-2] A. Matsuno, K. Kagawa and Y. Niwatsukino, T. Nire, and K. Shibahara, "Pulse Duration Effects on Laser Anneal Shallow Junction", Proc. of the 2nd Int. Semiconductor Tech. Conf., Vol.2002-17, pp. 148-156, (2002).
[Sh-C-3] N. Maeda, D. Onimatsu, Y. Ishikawa and K. Shibahara, " Gate-Extension Overlap Control by Sb Tilt Implantation", Proc. of the 2nd Int. Semiconductor Tech. Conf. (ISTC2002), Vol.2002-17, pp. 165-171, (2002).
[Sh-C-4] K. Kagawa, Y. Niwatsukino, M. Matsuno, and K. Shibahara, " Influence of pulse duration on KrF excimer laser annealing process for ultra shallow junction formation ", Int. Workshop on Junction Tech., pp. 31-34, (2002).
[Sh-C-5] K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno, and K. Shibahara, "Formation of Low-resistive Ultra-shallow n+/p Junction by Heat-assisted Excimer Laser Annealing", Int. Workshop on Junction Tech. (IWJT'02), pp. 35-36, (2002).
[Sh-C-6] K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno, and K. Shibahara, "Defect density reduction and sheet resistance improvement by multi-pulse KrF-excimer-laser annealing", Extend. Abst. Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors (USJ 2003), pp. 98-103, (2003).
[Sh-C-7] K. Imai, S. Maruyama, T. Suzuki, T. Kudo, S. Miyake, M. Ikeda, T. Abe, S. Masuda, A. Tanabe, J.-W. Lee, K. Shibahara, S. Yokoyama and H. Ooka, " 60-nm Gate Length SOI CMOS Technology Optimized for System-on-a SOI-Chip Solution", Proc. of the 203rd Meeting of Electrochemical Society, Silicon-on-insulator Technology and Devices XI, pp. 149-158, (2003).
[Sh-C-8] M. Hino, T. Amada, N. Maeda, and K. Shibahara, "Influence of Nitrogen Profile on Metal Workfunction in Mo/SiO2/Si MOS Structure", Ext. Abst. Int. Conf. on Solid State Devices and Materials, pp. 494-495, (2003).
[Sh-C-9] M. Murakawa, K. Shibahara, Y. Oda, T. Higuchi, and K. Nishi, " Ultra-shallow Boron Profile Fitting Compensating for Surface Contamination by Utilizing Genetic Algorithms ", Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'03), pp. 504-505, (2003).
[Sh-C-10] K. Shibahara, K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, and A. Matsuno, " KrF Excimer Laser Annealing For Ultra Shallow Junction Formation: Approach For Irradiation Energy Density Reduction ", Extend. Abst. 11th Int. Conf. on Adv. Thermal Processing of Semiconductors (RTP 2003), pp. 13-16, (2003). (Invited)
[Sh-C-11] M. Shibahara, S. Kotake, T. Inoue, A. Matsuno, K. Kagawa and K. Shibahara, "Molecular Dynamics Simulation On Excimer Laser Annealing Process For Ultra Shallow Junction Formation", The 1st Int. Symp. on Micro & Nano Technology, pp. VIII-1-02-1-VIII-1-02-5, (2004).

[Sh-C-12] T. Eto, and K. Shibahara, " Precise Depth Profi ling of Sub-keV Implanted Arsenic", Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'04), pp. 532-533, (2004).
[Sh-C-13] K. Sano, M. Hino, N. Ooishi, and K. Shibahara, "Workfunction Tuning Using Various Impurities for Fully Silicided NiSi Gate ", Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'04), pp. 456-457, (2004).
[Sh-C-14] E. Takii, T. Eto, K. Kurobe, A. Matsuno, and Kentaro Shibahara, "Merits and Demerits of light absorber for Ultra shallow junction formation by green laser annealing ", Int. Conf. on Ion Implantation Technology, p. 63, (2004).
[Sh-C-15] K. Shibahara, K. Kurobe and T. Eto, "Sub-20-nm Junction Formation by Heat-Assited Laser Annealing", Proceedings of 2004 Korea-Japan Joint Workshop on Advanced Semiconductor Processes and Equipments (ASPE 2004), pp. 162-165, (2004).
[Sh-C-16] T. Hosoi, M. Hino, K. Sano, N. Ooishi, and K. Shibahara, "Molybdenum-Gate MOSFET Threshold Voltage Modification Based on Two-Dimensional Nitrogen Distribution Control in Gate Electrode", Abstracts of MRS 2005 spring meeting, pp.191-192, (2005).
[Sh-C-17] K. Shibahara, K. Kurobe, T. Eto, and Y. Ishikawa, "Diffusion-less junction formation by heat-assisted laser annealing", Extended Abstracts of Int. Meeting for Future Electron Devices, Kansai (2005 IMFEDK, Kyoto, Apr 11-13), pp. 135-136, (2005).
[Sh-C-18] K. Shibahara, "Benefits of heat-assist for laser annealing ", Extended Abstracts of Int. Workshop on Junction Technology, (IWJT,Osaka, Jun 6-7), pp. 53-54, (2005).Invited
[Sh-C-19] K. Hosawa, K. Matsumoto, and K. Shibahara, "Anomalous Doping Profile in Heavily Doped Ge", Extended Abstracts of Int. Workshop on Junction Technology, (IWJT,Osaka, Jun 6-7), pp. 39-40, (2005).
[Sh-C-20] A. Matsuno, and K. Shibahara, "Function of Phase Switch Layer for Ultra Shallow Junction Formation by Green Laser Annealing", Ext. Abst. Int. Conf. on Solid State Devices and Materials (SSDM'05, Kobe, Sep. 13-15), pp.914-915, (2005).
[Sh-C-21] K. Shibahara, A. Matsuno, E.. Takii, and T. Eto, "Green laser annealing with light absorber", 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors - RTP 2005 (Santa Barbara, Oct. 4-7), pp.101-104, (2005).
[Sh-C-22] K. Sano, T. Hosoi, and K. Shibahara, "Importance of heat-up ramp rate for palladium-silicide fully-silicided-gate structure formation", 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors RTP 2005, (Santa Barbara, Oct. 4-7), pp. 145-148, (2005).
[Sh-C-23] T. Hosoi, K. Sano, M. Hino, A. Ohta, K. Makihara, H. Kaku, S. Miyazaki, and K. Shibahara, "Characterization of Sb-Doped Fully-Silicided NiSi/SiO2/Si MOS Structure", 2005 International Semiconductor Device Research Symposium Proceedings (ISDRS 2005, Bethesda, Maryland, USA, Dec. 7-9), pp. WP-4-05-1-WP-4-05-2, (2005).

論文リスト(中島グループ)

[Na-1] A. Nakajima and M. Ishigame, " Local-hopping mechanism of an oxygen vacancy in ZrO2 doped with Sc3+ studied by measuring quasi-elastic light scattering ", Solid State Ionics Vol. 146, No. 1-2, pp.133-141, Jan, (2002).
[Na-2] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, " NH3-annealed atomic-layer-deposited silicon nitride as a high-k gate dielectric with high reliability ", Appl. Phys. Lett. Vol. 80, No. 7, pp. 1252-1254, Feb, (2002).
[Na-3] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " Low thermal-budget ultrathin NH3-annealed atomic-layer-deposited Si-nitride/SiO2 stack gate dielectrics with excellent reliability ", IEEE Electron Device Lett. Vol. 23, No. 4, pp. 179-181, April, (2002).
[Na-4] K. Kawamura, T. Kidera, A. Nakajima, and S. Yokoyama, " Coulomb blockade effects and conduction mechanism in extremely thin polycrystalline-silicon wires ", J. Appl. Phys. Vol. 91, No. 8, pp. 5213-5220, Apr, (2002).
[Na-5] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " Reliable extraction of the energy distribution of Si/SiO2 interface traps in ultrathin metal-oxide-semiconductor structures ", Appl. Phys. Lett. Vol. 80, No. 21, pp. 3952-3954, May, (2002).
[Na-6] Y. Ito, T.i Hatano, A. Nakajima, and S. Yokoyama, " Fabrication of Si single-electron transistors having double SiO2 barriers ", Appl. Phys. Lett. Vol. 80, No. 24, pp. 4617-4619, June, (2002).
[Na-7] A. Nakajima, Y. Ito, and S. Yokoyama, " Conduction mechanism of Si single-electron transistors having an one-dimensional regular array of multiple tunnel junctions ", Appl. Phys. Lett. Vol. 81, No.

4, pp. 733-735, July, (2002).
[Na-8] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " High quality NH3-annealed atomic Layer Deposited Si-nitride/SiO2 Stack Gate Dielectrics for Sub-100nm Technology Generations ", Solid State Electron. Vol. 46, No.10, pp. 1659-1664 Oct, (2002).
[Na-9] 横山新、吉野雄信、藤井敏昭、芝原健太郎、中島安理、吉川公麿、角南英夫、Q.D.M. Khosru, "ウェハ保管環 MOS デバイス特性への影響",エアロゾル研究 第 17 巻, 第 2 号, pp. 96-104, (2002).
[Na-10] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, " Low temperature formation of highly-reliable silicon-nitride gate dielectrics with suppressed soft-breakdown phenomena for advanced complementary metal-oxide-semiconductor technology ", J. Vac. Sci. & Technol. B Vol. 20, No. 4, pp. 1406 1409, July/August, (2002).
[Na-11] A. Nakajima, T. Kidera, H. Ishii, and S. Yokoyama, " Atomic-layer deposition of ZrO2 with a Si nitiride barrier layer ", Appl. Phys. Lett. Vol. 81, No. 15, pp. 2824-2826, Oct, (2002).
[Na-12] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " Response to " Comment on 'Reliable extraction of the energy distribution of Si/SiO2 interface traps in ultrathin metal-oxide-semiconductor structures' ' ' [Appl. Phys. Lett. 81, 3681 (2002)] ", Appl. Phys. Lett. Vol. 81, No. 19, pp. 3683-3684, Nov, (2002).
[Na-13] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, and S. Yokoyama, " Atomic-layer-deposited silicon nitride/SiO2 stack ---- a highly potential gate dielectrics for advanced CMOS technology " Microelectronics Reliability Vol. 42, pp.1823-1835, Dec, (2002). (Introductory Invited)
[Na-14] A. Nakajima, Q.D.M. Khosru, T. Kasai, and S. Yokoyama, " Carrier Mobility in p-MOSFET with Atomic-Layer-Deposited Si-Nitride/SiO2 Stack Gate Dielectrics ", IEEE Electron Device Lett. Vol. 24, No. 7, pp. 472 474, July, (2003).
[Na-15] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kasai, and S. Yokoyama, " High Quality Atomic-Layer-Deposited Ultrathin Silicon-Nitride Gate Dielectrics with Low Density of Interface and Bulk Traps ", Appl. Phys. Lett. Vol. 83, No.2, pp. 335-337, July, (2003).
[Na-16] Q.D.M. Khosru, S. Yokoyama, A. Nakajima, K. Shibahara, T. Kikkawa, H. Sunami, and Takenobu Yoshino, " Organic Contamination Dependence of Process-Induced Interface Trap Generation in Ultrathin Oxide Metal Oxide Semiconductor Transistors ", Jpn. J. Appl. Phys. Vol. 42, No. 12A, pp. L1429-L1432, Dec, (2003).
[Na-17] H. Ishii, A. Nakajima, and S. Yokoyama, " Growth and electrical properties of atomic-layer deposited ZrO2/Si-nitride stack gate dielectrics ", J. Appl. Phys. Vol. 95, No. 2, pp.536-542, Jan, (2004).
[Na-18] T. Kitade and A. Nakajima, " Application of highly doped Si single-electron transistors to an exclusive-NOR operation ", Jpn. J. Appl. Phys. Vol. 43, No. 3B, pp. L418-L420, March, (2004).
[Na-19] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " Modified Direct-Current Current-Voltage Method for Interface Trap Density Extraction in Metal-Oxide-Semiconductor Field-Effect-Transistor with Tunneling Gate Dielectrics at High Temperature ", Jpn. J. Appl. Phys. Vol. 44, No. 2A, pp. L60–L62, Jan, (2005).
[Na-20] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " An abnormal enhancement of interface trap generation under dynamic oxide field stress at Mega Hz region ", Appl. Phys. Lett. Vol. 86, No.8, 083501 (3 pages) Feb, (2005).
[Na-21] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " Interface Trap Generation Induced by Charge Pumping Current under Dynamic Oxide Field Stresses ", IEEE Electron Device. Lett. Vol. 26, No.3, pp. 216-218, March, (2005).
Na-22] T. Kitade, K. Ohkura, and A. Nakajima, " Room-temperature operation of an exclusive-OR circuit using a highly doped Si single-electron transistor ", Appl. Phys. Lett. Vol. 86, No.8, 123-118 (3 pages), March, (2005).
[Na-23] S. Zhu, and A. Nakajima, " Annealing Temperature Dependence on Nickel-Germanium Solid-State Reaction ", Jpn. J. Appl. Phys. Vol. 44, No. 24 pp. L753–L755, June, (2005).
[Na-24] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " Enhancement of BTI Degradation in pMOSFETs under High-Frequency Bipolar Gate Bias ", IEEE Electron Device. Lett. Vol. 26, No. 6, pp. 387-389, June, (2005).
[Na-25] A. Nakajima, H. Ishii, and S. Yokoyama, " Carrier Mobility in Metal-Oxide-Semiconductor Field Effect Transistor with Atomic-Layer-Deposited Si-Nitride Gate Dielectrics ", Jpn. J. Appl. Phys. Vol. 44, No. 28 pp. L903-L905, July, (2005).

[Na-26] A. Nakajima, T. Ohashi, S. Zhu, S. Yokoyama, S. Michimata, and H. Miyake, " Atomic-Layer-Deposited Si-Nitride/SiO2 Stack Gate Dielectrics for Future High-Speed DRAM with Enhanced Reliability ", IEEE Electron Device. Lett. Vol. 26, No. 8, pp. 538-540, August, (2005).

[Na-27] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " Pulse Waveform Dependence on Ac Bias Temperature Instability in pMOSFETs ", IEEE Electron Device. Lett. Vol. 26, No. 9, pp. 658-660, Sept. (2005).

[Na-28] S. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, " Interface trap and oxide charge generation under negative bias temperature instability of p-channel metal-oxide-semiconductor field-effect transistors with ultrathin plasma-nitrided SiON gate dielectric ", J. Appl. Phys. Vol. 98, No. 11, in press.

[Na-29] K. Ohkura, T. Kitade, A. Nakajima, " Periodic Coulomb oscillation in Si single-electron transistor based on multiple islands ", J. Appl. Phys. Vol. 98, No. 12, in press.

国際会議リスト(中島グループ)

[Na-C-1] A. Nakajima and S. Yokoyama, " Atomic-layer-deposition of Si nitride and ZrO2 for gate dielectrics ", Abst. AVS Topical Conference on Atomic Layer Deposition (ALD 2002) (Seoul, August 19-21), pp. 6-6, (2002). (Invited)

[Na-C-2] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " A novel method for extracting the energy distribution of Si/SiO2 interface traps in ultrathin oxide MOS structures ", presented in the Second IEEE Conference on Nanotechnology (Washington, D.C., August 26-28), (2002).

[Na-C-3] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, " Time-dependent breakdown of ultrathin SiO2 gate dielectrics under static and dynamic stress ", Abst. 2nd ECS Int. Semiconductor Technology Conf. (Tokyo, September 11-14), Abstract No.71, (2002).

[Na-C-4] H. Ishii, T. Kidera, A. Nakajima, and S. Yokoyama, " Atomic-layer deposition of ZrO2 with a Si nitiride barrier layer ", Extend. Abst. 2002 Int. Conf. on Solid State Devices and Materials (Nagoya, September 17 19), pp. 452-453, (2002).

[Na-C-5] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, " A comparative study of bulk and interface trap generation in ultrathin SiO2 and atomic-layer-deposited Si-nitride/SiO2 stack gate dielectrics ", Forth Int. Symposium on Control of Semiconductor Interface (ISCSI-IV) (Karuizawa, October 21-25), pp. A6-3-A6-3, (2002).

[Na-C-6] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, " An Effective Method for Obtaining Interface Trap Distribution in MOS capacitors with Tunneling Gate Oxides ", Proceedings 2002 IEEE Int. Conf. on Semiconductor Electronics (ICSE 2002) (Penang, December 19-21) pp. 402-406, (2002).

[Na-C-7] T. Kitade, K. Ohkura, and A. Nakajima, " Periodic Coulomb oscillation in highly doped Si single electron transistor ", Extend. Abst. 2003 Int. Conf. on Solid State Devices and Materials (SSDM2003) (Tokyo, September 16-18), pp. 584-585, (2003).

[Na-C-8] A. Nakajima, H. Ishii, T. Kitade, and S. Yokoyama, " Atomic-Layer-Deposited Ultrathin Si-Nitride Gate Dielectrics ---A Better Choice for Sub-tunneling Gate Dielectrics--- ", Technical Digest of the 2003 IEEE International Electron Devices Meeting (Washington, D.C., Dec. 8-10), pp.657-660, (2003).

[Na-C-9] T. Kitade, K. Ohkura, and A. Nakajima, " Room Temperature Operation of an Exclusive-OR Circuit Using a Highly-doped Si Single-Electron Transistors ", Extend. Abst. 2004 Int. Conf. on Solid State Devices and Materials (SSDM2004), pp.890-891, (2004).

[Na-C-10] A. Nakajima and S. Yokoyama, " Atomic-layer-deposition of ultrathin silicon nitride for sub-tunneling gate dielectrics ", ECS Symposium I1: Proceedings of the First International Symposium on Dielectrics for Nanosystems (Honolulu, Hawaii, October 3-8) Vol. 2004-04, pp.418-424, (2004). (Invited)

[Na-C-11] Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake, " Interface Trap Generation on Thin SiO2 and Plasma-Nitrided SiO2 Gate Dielectrics under Static and Dynamic Stresses ", Proceedings 2004 7th Int. Conf. on Solid-State and Integrated-Circuits Technology (ICSICT'04) (Beijing, October 18-21), pp. 828-831, (2004).

[Na-C-12] Shiyang Zhu, Anri Nakajima, Yuichi Yokoyama, Kensaku Ohkura, " Temperature Dependence of Ni-Germanide Formed by Ni-Ge Solid-State Reaction ", Extend. Abst. 5th International Workshop on Junction Technology 2005 (IWJT2005)(Osaka, June 7-8), pp. 85-86, (2005).

[Na-C-13] Shiyang Zhu, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake, " Influence of bulk bias on NBTI of pMOSFETs with ultrathin SiON gate dielectric ", Extend. Abst. 2005 Int. Conf. on Solid State Devices and Materials (SSDM2005)(Kobe, Sept. 13-15), pp. 872-873, (2005).

論文リスト(吉川グループ)

[Ki-1] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, " High Transmission Gain Integrated Antenna on Extremely High Resistivity Si for ULSI Wireless Interconnect ", IEEE Electron Device Letters, Vol. 23, No.12, December, pp.731-733, (2002).

[Ki-2] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, " Characteristics of Integrated Antenna on Si for On Chip Wireless Interconnect ", Japanese Journal of Applied Physics, Vol. 42, No. 4B, April, pp. 2204-2209, (2003).

[Ki-3] A.B.M.H. Rashid, S. Watanabe and T. Kikkawa, " Characteristics of Si Integrated Antenna for Inter-Chip Wireless Interconnection ", Japanese Journal of Applied Physics Vol. 43, No. 4B, pp.2283-22287, (2004).

[Ki-4] S. Watanabe, A.B.M.H. Rashid and T. Kikkawa, " Effect of High Resistivity Si substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects ", Japanese Journal of Applied Physics Vol. 43, No. 4B, pp.2297-2301, (2004).

[Ki-5] Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa, " A CMOS Monocycle Pulse Generation Circuit in a Ultra-Wideband Transmitter for Intra/Inter Chip Wireless Interconnection ", Japanese Journal of Applied Physics Vol. 44, No. 4B, pp.2104-2108, (2005).

[Ki-6] Kentaro Kimoto and Takamaro Kikkawa, " Transmission Characteristics of Gaussian Monocycle Pulses for Inter Chip Wireless Interconnections Using Integrated Antennas ", Japanese Journal of Applied Physics Vol. 44, No. 4B, pp.2756-2760, (2005).

[Ki-7] A. B. M. H. Rashid, Nasrin Sultana, M. Rezwan Khan and T. Kikkawa, " Efficient Design of Integrated Antennas on Si for On-Chip Wireless Interconnects in Multi-Layer Metal Process ", Japanese Journal of Applied Physics Vol. 44, No. 4B, pp.2761-2765, (2005).

[Ki-8] T. Kikkawa, K. kimoto and S. Watanabe, " Ultrawideband characteristics of fractal dipole antennas integrated on Si for ULSI wireless interconnects ", IEEE Electron Device Letters, Volume 26, Issue 10, Oct, pp.767–769, (2005).

国際会議発表リスト(吉川グループ)

[Ki-C-1] A.B.M. H. Rashid, S. Watanabe, T. Kikkawa, X. Guo and K. K. O, " Interference suppression of wireless interconnection in Si integrated antenna ", Proceedings of International Interconnect Technology Conference, pp.173-175, San Francisco, USA, June 3-5, (2002).

[Ki-C-2] S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, " Influence of Si Substrate Ground on Antenna Transmission Gain for on-chip Wireless Interconnects ", Proceedings of Advanced Metallization Conference 2002, Asian Session, pp.94-95, (2002).

[Ki-C-3] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, " Wireless Interconnection on Si using Integrated Antenna ", Ext. Abst. of 2002 International Conference on Solid State Devices and Materials, pp.648-649, Nagoya, Japan, September (2002).

[Ki-C-4] T. Kikkawa, A.B.M. H. Rashid and S. Watanabe, " Effect of silicon substrate on the transmission characteristics of integrated antenna ", Proceedings of 2003 IEEE Topical Conference on Wireless Communication Technology, S06P09, Honolulu, Oct. 15-17, (2003).

[Ki-C-5] A.B.M. H. Rashid, S. Watanabe and T. Kikkawa, " Crosstalk Isolation of Monopole Integrated Antenna on Si for ULSI Wireless Interconnect ", Proceedings of 2003 IEEE International Interconnect Technology Conference, pp.156-158. San Francisco, USA, June 2-4, (2003).

[Ki-C-6] A.B.M. H. Rashid, S.Watanabe and T. Kikkawa, " Inter-chip Wireless Interconnection using Si Integrated Antenna ", Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp.394-395, Tokyo, Sept. 16-18, 2003.

[Ki-C-7] S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, " Effect of High Resistivity Si Substrate on Antenna Transmission Gain for On-Chip Wireless Interconnects," Ext. Abst. of Inter. Conf. on Solid State Devices and Materials, pp.668 669, Tokyo, Sept. 16-18, (2003).

[Ki-C-8] K. Kimoto, S. Watanabe, T. Kikkawa, P. S. Hall, and Y. Yuan, " Characteristics of Fractal Dipole Antennas Integrated on Si for ULSI Wireless Interconnects ", Proc. of IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting, Vol. 4, pp.3437-3440, Monterey, California, June 20-25, (2004).

[Ki-C-9] S. Watanabe, K. Kimoto and T. Kikkawa, " Transient Characteristics of Integrated Dipole Antennas on Silicon for Ultra Wideband Wireless Interconnects ", Proc. of IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting, Vol. 3, pp.2277-2280, Monterey, California, June

20-25, (2004).
[Ki-C-10] K. Kimoto, S. Watanabe, A.B.M. H. Rashid and T. Kikkawa, " Inter-chip Signal Transmission using Si Integrated Antenna ", Proc. IEICE 2004 International Symposium on Antennas and Propagation, Vol. 1 pp.109-112, Sendai, August 17-21, (2004).
[Ki-C-11] K. Kimoto and T. Kikkawa, " Transmission characteristics of Gaussian monocycle pulse for inter-chip wireless interconnection using integrated antenna ", Ext. Abst. of the 2004 International Conference on Solid State Devices and Materials 2004, pp.304-305, Tokyo, September 15-17, (2004).
[Ki-C-12] P. K. Saha, N Sasaki and T. Kikkawa, " A CMOS UWB Transmitter for Intra/Interchip wireless communication ", 2004 IEEE International Symposium on Spread Spectrum Techniques and Applications, pp.962-966, Sydney Australia, 30 August-2 September, (2004).
[Ki-C-13] P. K. Saha, N Sasaki and T. Kikkawa, " A CMOS Monocycle Pulse Generation Circuit of UWB Transmitter for Intra/Inter Chip Wireless Interconnection ", Extended Abstract of the 2004 International Conference on Solid State Devices and Materials, Tokyo, pp.394-395, (2004).
[Ki-C-14] K. Kimoto and T. Kikkawa, " Data Transmission Characteristics of Integrated Linear Dipole Antennas for UWB Communication in Si ULSI ", Proc. of IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting, Vol. 1B, pp.678-681, Washington DC, July 3-8, 2005.
[Ki-C-15] M. Nitta and T. Kikkawa, " Interference of Digital Noise with Integrated Dipole Antenna for Inter-chip Signal Transmission in ULSI ", Proc. of IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting, Vol. 3B, pp.264-267, Washington DC, July 3-8, (2005).
[Ki-C-16] K. Kimoto, N. Sasaki, P. K. Saha, M. Nitta, T. Kikkawa and M. Sasaki, " Analysis of Transmission Characteristics of Gaussian Monocycle Pulse for Silicon Integrated Antennas ", Ext. Abst. of the 2005 International Conference on Solid State Devices and Materials, Kobe, September 13-15, pp.308-309, (2005).
[Ki-C-17] P. K. Saha, N. Sasaki and T. Kikkawa, " A 2.5 GHz Differential Wavelet Generator in 0.18 μm CMOS for 1.4 Gbps UWB Impulse Radio in Wireless Inter/Intra-Chip Data Communication ", Extended abstract of the 2005 International Conference on Solid State Devices and Materials, Kobe, September 13-15, pp.310-311, (2005).
[Ki-C-18] N. Sasaki, P. K. Saha and T. Kikkawa, " A Single Chip UWB Receiver based on 0.18-μm CMOS Technology ", Proceedings of 2005 International Workshop on UWB Technologies, Yokosuka, December 8-10, pp.46-50.769, (2005).

論文リスト(横山グループ)

[Yo-1] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, " Soft Breakdown Suppressed Ultra-Thin Atomic-Layer-Deposited Silicon Nitride/SiO2 Stack Gate Dielectrics for Advanced Complementary Metal-Oxide Semiconductor Technology ", Appl. Phys. Lett. 79, No. 21, pp. 3488-3490, (2001).
[Yo-2] T. Yoshino, S. Yokoyama and T. Fujii, " Influence of Organic Contaminant on Trap Generation in Thin SiO2 of Metal-Oxide-Semiconductor Capacitors," Jpn. J. Appl. Phys. 41, No. 7A, pp.4750-4753, (2002).
[Yo-3] A. Nakajima, Quazi D.M. Khosru, T. Yoshimoto, T. Kidera and S. Yokoyama, "NH3-annealed atomic-layer deposited silicon nitride as a high-k gate dielectric with high reliability ", Appl. Phys. Lett. 80, No. 7, pp. 1252-1254, (2002).
[Yo-4] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto and S. Yokoyama, " Low Thermal-Budget Ultrathin NH3 Annealed Atomic-Layer-Deposited Si-Nitride/SiO2 Stack Gate Dielectrics With Excellent Reliability ", IEEE Electron Device Lett. 23 No. 4, pp. 179-181, (2002).
[Yo-5] K. Kawamura, T. Kidera, A. Nakajima and S. Yokoyama, " Coulomb blockade effects and conduction mechanism in extremely thin polycrystalline-silicon wires," J. Appl. Phys. 91, No. 8, pp. 5213-5220, (2002).
[Yo-6] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto and S. Yokoyama ", Reliable extraction of the energy distribution of Si/SiO2 interface traps in ultrathin metal-oxide-semiconductor," Appl. Phys. Lett. 80, No. 21, pp. 3952-3954, (2002).
[Yo-7] Y. Ito, T. Hatano, A. Nakajima, and S. Yokoyama ", Fabrication of Si single-electron transistors having double SiO2 barriers," Appl. Phys. Lett. 80, No. 24, pp. 4617-4619, (2002).
[Yo-8] 横山新、吉野雄信、芝原健太郎、中島安理、吉川公麿、角南英夫、Quazi D. M. Khosru, " ウェハ保

管環境　MOS デバイス特性への影響,"エアロゾル研究、第 17 巻、第 2 号 pp. 96-104, (2002).
[Yo-9] A. Nakajima, Y. Ito and S. Yokoyama, " Conduction mechanism of Si single-electron transistor having a one dimensional regular array of multiple tunnel junctions ", Appl. Phys. Lett. 81, No. 4, pp. 733-735, (2002).
[Yo-10] A. Nakajima, Quazi D.M. Khosru, T. Yoshimoto, T. Kidera and S. Yokoyama, " Low-temperature formation of highly reliable silicon-nitride gate dielectrics with suppressed soft-breakdown phenomena for advanced complementary metal-oxide-semiconductor technology ", J. Vac. Sci. & Tech. B, 20, No. 4, pp. 1406-1409, (2002).
[Yo-11] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto and S. Yokoyama, " High-quality NH3-annealed atomic layer deposited Si-nitride/SiO2 stack gate dielectrics for sub-100 nm technology generations ", Solid-State Electronics, 46, pp. 1659-1664, (2002).
[Yo-12] A. Nakajima, Toshirou Kidera, Hiroyuki Ishii and S. Yokoyama, " Atomic-layer deposition of ZrO2 with a Si nitride barrier layer ", Appl. Phys. Lett. 81, No. 15, pp. 2824-2826 (2002).
[Yo-13] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto and S. Yokoyama, " Response to ", Comment on 'Reliable extraction of the energy distribution of Si/SiO2 interface traps in ultrathin metal-oxide-semiconductor structurtes' ", [Appl. Phys. Lett. 81、3681 (2002)], ", Appl. Phys. Lett. 81, No. 19, pp. 3683-3684, (2002).
[Yo-14] A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, and S. Yokoyama, " Atomic-layer-deposited silicon-nitride/SiO2 stack - a highly potential gate dielectrics for advanced CMOS technology ", Microelectronics Reliability 42, pp.1823-1835, (2002). (Introductory Invited)
[Yo-15]A. Nakajima, Q.D.M. Khosru, T. Kasai, and S. Yokoyama, " Carrier Mobility in p-MOSFET with Atomic-Layer Deposited Si-Nitride/SiO2 Stack Gate Dielectrics ", IEEE Electron Device Lett. 24, pp. 472-474, (2003).
[Yo-16] A. Nakajima, Quazi D.M. Khosru, Takashi Yoshimoto, Tetsurou Kasai, and Sin Yokoyama, " High quality atomic layer deposited ultrathin Si-nitride gate dielectrics with low density of interface and bulk traps ", Appl. Phys. Lett. 84, No. 2, pp. 335-337, (2003).
[Yo-17] K. Imai, S. Shishiguchi, K. Shibahara and S. Yokoyama, " Phosphorous-Assisted Low-Energy Arsenic Implantation Technology for N-Channel Metal-Oxide-Semiconductor Field Effect Transistor Source/drain Foramation Process ", Jpn. J. Appl. Phys. 42, No. 5A, pp.2654-2659, (2003).
[Yo-18] S. Nakamura, M. Itano, H. Aoyama, K. Shibahara, S. Yokoyama and M. Hirose, " Comparative Studies of Perfluorocarbon Alternative Gas Plasmas for Contact Hole Etch ", Jpn. J. Appl. Phys. 42, No. 9A, pp.5759-5764 (2003).
[Yo-19] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, " Evaluation of Surface Contamination by Noncontact Capacitance Method under UV Irradiation ", Jpn. J. Appl. Phys. 42, No. 9A, pp.5837-5843, (2003).
[Yo-20] Y. Hara, S. Yokoyama and K. Umeda, " Compact Branched Optical Waveguides Using High-Index-Contrast Stacked Structure ", Optical Review 10, No. 5, pp. 357-360, (2003).
[Yo-21] Q.D.M. Khosru, S. Yokoyama, A. Nakajima, K. Shibahara, T. Kikkawa, H. Sunami and T. Yoshino, " Organic Contamination Dependence of Process Induced Interface Trap Generation in Ultrathin Oxide Metal Oxide Semiconductor Transistors ", Jpn. J. Appl. Phys. 42, Pt 2, No. 12A, L1429-L1432, (2003).
[Yo-22] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, " Investigation of Surface Contamination on Silicon Oxide after HF Etching by Noncontact Capacitance Method ", Jpn. J. Appl. Phys. 42, Pt 1, No. 12, pp.7601-7602, (2003).
[Yo-23] H. Setyawan, M. Shimada, Y. Hayashi, K. Okuyama and S. Yokoyama, " Particle Formation and Trapping Behavior in a TEOS/O2 Plasma and Their Effects on Contamination of a Si Wafer ", Aerosol Science and Technology 38, No. 2, pp. 120-127, (2004).
[Yo-24] H. Ishii, A. Nakajima, and S. Yokoyama, "Growth and electrical properties of atomic-layer deposited ZrO2/Si nitride stack gate dielectrics ", J. Appl. Phys. 95, pp.536-542, (2004).
[Yo-25] M. Ooka and S. Yokoyama, "SiO2 Hole Etching Using Perfluorocarbon Alternative Gas with Small Global Greenhouse Effect ", Jpn. J. Appl. Phys. 43, No. 6A, pp.3586-3589 (2004).
[Yo-26] M. Suzuki and S. Yokoyama, " Evaluation of Front-Opening Unified Pod with Attached UV/Photocatlyst Cleanig Unit ", Jpn. J. Appl. Phys. 44, No. 2, pp.1130-1131, (2005).
[Yo-27] M. Suzuki and S. Yokoyama, "Mechanism of Anomalous Behavior of Metal-Oxide-Semiconductor Capacitors Contaminated with Organic Molecules", Jpn. J. Appl. Phys. 44, No. 3, pp.1208-1212 (2005).

[Yo-28] M. Ooka and S. Yokoyama, ”Contact-Hole Etching with NH3-Added C5F8 Pulse-Modulated Plasma ”, Jpn. J. Appl. Phys. 44, No. 9A, pp.6476-640, (2005).
[Yo-29] 近藤洋平、中島健、田中武、高木俊宜、渡邉悟志、大倉健作、芝原健太郎、横山新, ”プラズマベースイオン 入滅菌法における窒素イオンエネルギーの推定”,真空, 48, No. 5 pp. 339-342, (2005).
[Yo-30] T. Tanaka, S. Watanabe, K. Shibahara, S. Yokoyama, and T. Takagi, ”Plasma-based ion implantation sterilization technique and ion energy estimatio ”, J. Vac. Sci. Technol. A 23, No. 4, July/Aug. pp. 1018-1021, (2005).
[Yo-31] 島田学、柏原伸紀、林豊、奥山喜久夫、横山新、池田弥央、” 新規変調プラズマによるSiH4/H2プラズマﾘｱ クター内のダスﾄ微粒子の抑制”,エアロゾル研究、第20巻、第3号 pp. 231-237, (2005).
[Yo-32] Zhimou Xu, M. Suzuki, and S. Yokoyama, ”Structure and Optical Band-Gap Energies of Ba0.5Sr0.5TiO3 Thin Films Fabricated by RF Magnetron Plasma Sputtering”, Jpn. J. Appl. Phys. 44, No. 12, pp.8507-8511 (2005).
[Yo-33] Y. Tanushi and S. Yokoyama, ”Design and Simulation of Ring Resonator Switches using Electro-Optic Materials”, Jpn. J. Appl. Phys. to be published, (2006).
[Yo-34] M. Suzuki, Zhimou Xu, Y. Tanushi and S. Yokoyama, ”Structural and Optical Properties of Electro-Optic Material: Sputtered (Ba,Sr)TiO3 ”, Jpn. J. Appl. Phys. to be published, (2006).
[Yo-35] Zhimou Xu, M. Suzuki, Y. Tanushi, K. Wakushima and S. Yokoyama, ”Groove-Buried Optical Waveguides Based on Metal Organic Solution-Derived Ba0.7Sr0.3TiO3 Thin Films”, Jpn. J. Appl. Phys. to be published, (2006).
[Yo-36] T. Tabei, K. Maeda, S. Yokoyama, and H. Sunami, ”Fabrication of spin-coat optical waveguides for optically interconnected LSI and influence of fabrication process on lower layer MOS capacitors”, Jpn. J. Appl. Phys. to be published, (2006).

国際会議ﾘｽﾄ(横山グループ)

[Yo-C-1] M. Ooka and S. Yokoyama, ” Ultrasmall SiO2 Hole Etching using PFC Alternative Gas with Small Global Greenhouse Effect ”, Digest of Pacific Rim Workshop on Transducers and Micro/Nano Technologies (MEMS2002), pp. 111-114, (2002).
[Yo-C-2] M. Kohno, T. Kitajima, S. Hirae and S. Yokoyama, ” Evaluation of Surface Contamination by Noncontact Capacitance Method under UV Irradiation ”, Extend. Abst. Int. Conf. on Solid State Devices and Materials (SSDM2002), pp. 724-725, (2002).
[Yo-C-3] H. Ishii, T. Kidera, A. Nakajima and S. Yokoyama, ” Atomic-layer deposition of ZrO2 with a Si nitride barrier layer ”, Extend. Abst. Int. Conf. on Solid State Devices and Materials (SSDM2002), pp. 452-453, (2002).
[Yo-C-4] A. Nakajima and S. Yokoyama, ”A tomic-layer-deposition of Si nitride and ZrO2 for gate dielectrics ”, Abst. AVS Topical Conference on Atomic Layer Deposition (ALD 2002) (Seoul, August 19-21), pp. 6-6, (2002). (Invited)
[Yo-C-5] Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, ” A novel method for extracting the energy distribution of Si/SiO2 interface traps in ultrathin oxide MOS structures ”, presented in the Second IEEE Conference on Nanotechnology (Washington, D.C., August 26-28), (2002).
[Yo-C-6] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, ” Time-dependent breakdown of ultrathin SiO2 gate dielectrics under static and dynamic stress ”, Abst. 2nd ECS Int. Semiconductor Technology Conf. (Tokyo, September 11-14), Abstract No.71, (2002).
[Yo-C-7] H. Ishii, T. Kidera, A. Nakajima, and S. Yokoyama, ” Atomic-layer deposition of ZrO2 with a Si nitiride barrier layer ”, 2002 Int. Conf. on Solid State Devices and Materials (Nagoya, September 17-19), pp. 452-453, (2002).
[Yo-C-8] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, ” A comparative study of bulk and interface trap generation in ultrathin SiO2 and atomic-layer-deposited Si-nitride/SiO2 stack gate dielectrics ”, Forth Int. Symposium on Control of Semiconductor Interface (ISCSI-IV) (Karuizawa, October 21-25) pp. A6-3-A6-3, (2002).
[Yo-C-9] Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, ” An Effective Method for Obtaining Interface Trap Distribution in MOS capacitors with Tunneling Gate Oxides ”, Proceedings 2002 IEEE Int. Conf. on Semiconductor Electronics (ICSE 2002) (Penang, December 19-21) pp. 402-406, (2002).
[Yo-C-10] M. Ooka and S. Yokoyama, ” Excellent Contact-Hole Etching with NH3 Added C5F8 Pulse-Modulated Plasma,” Extend. Abst. Int. Conf. on Solid State Devices and Materials (SSDM2003), pp. 454-455, (2003).
[Yo-C-11] A. Nakajima, H. Ishii, T. Kitade, and S. Yokoyama, ” Atomic-Layer-Deposited Ultrathin

Si-Nitride Gate Dielectrics ---A Better Choice for Sub-tunneling Gate Dielectrics--- ", Technical Digest of the 2003 IEEE International Electron Devices Meeting (Washington, D.C., Dec. 8-10) pp.657-660, (2003).
[Yo-C-12] S. Yokoyama, "Fabrication Technology for 26 nm Si MOS Transistors", The 1st International Workshop on Nanoscale Semiconductor Devices (Seoul, May 18-19) pp.105-124, (2004). (Invited)
[Yo-C-13] M. Suzuki and S. Yokoyama, "Anomalous Behavior of Interface Traps of Si MOS Capacitors Contaminated with Organic Molecules", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2004), pp. 530-531, (2004).
[Yo-C-14] Y. Tanushi, M. Wake, and S. Yokoyama, " Race-Track Optical Ring Resonators with Groove Coupling ", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2004), pp. 940-941, (2004).
[Yo-C-15] Y. Tanushi, M. Wake, K. Wakushima, M. Suzuki, and S. Yokoyama, "Technology for Ring Resonator Switches using Electro-Optic Materials", presented at 1st International Conference on Group IV Photonics (Hong Kong, China, Sept. 29-Oct. 1), WB3, (2004).
[Yo-C-16] T. Kakite, M. Wake, and S. Yokoyama, "Characterization of Porous Silicon Nitride Formed by Plasma-Enhanced Chemical Vapor Deposition", presented at ECS Symposium H1-843: Dielectric Science and Technology/Electronics (Honolulu, Hawaii, October 3-8), (2004).
[Yo-C-17]A. Nakajima and S. Yokoyama, "Atomic-layer-deposition of ultrathin Si Nitride for sub-tunneling gate dielectrics--", presented at ECS Symposium I1-890: First International Symposium on Dielectrics for Nanosystems (Honolulu, Hawaii, October 3-8), (2004). (Invited)
[Yo-C-18]Y. Tanushi and S. Yokoyama, "Design and Simulation of Ring Resonator Switches using Electro-Optic Materials", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2005), pp. 318-319, (2005).
[Yo-C-19] M. Suzuki, Zhimou Xu, Y. Tanushi and S. Yokoyama, " Structural and Optical Properties of Electro-Optic Material: Sputtered (Ba,Sr)TiO3", Abst. Int. Conf. on Solid State Devices and Materials, pp. 732-733, (2005).
[Yo-C-20] Zhimou Xu, M. Suzuki, Y. Tanushi, K. Wakushima and S. Yokoyama, " Groove-Buried Optical Waveguides Based on Metal Organic Solution-Derived Ba0.7Sr0.3TiO3 Thin Films ", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2005), pp. 738-739, (2005).
[Yo-C-21]T. Tabei, K. Maeda, S. Yokoyama, and H. Sunami, "Fabrication of spin-coat optical waveguides for optically interconnected LSI and influence of fabrication process on lower layer MOS capacitors", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2005), pp. 332-333, (2005).
[Yo-C-22] S. Yokoyama and T. Kakite, "Novel Fabrication Technique of Optical Waveguides using Low Density Silicon Nitride Films Deposited by Plasma-Enhanced Chemical Vapor Deposition", Abst. Int. Conf. on Solid State Devices and Materials (SSDM2005), pp. 736-737, (2005).
[Yo-C-23] Y. Tanushi and S. Yokoyama, "High-Speed and Low-Voltage Ring Resonator Optical Switches Using Electro- and Magneto-Optic Materials", presented at 2nd International Conference on Group IV Photonics (Antwerp, Belgium, Sept. 21-23), pp. 165 -167, (2005).

論文リスト(宮崎, 東グループ)

[MH-1] Y. Okamoto, K. Makihara, S. Higashi and S. Miyazaki, "Formation of microcrystalline germanium (μc-Ge:H) films from inductively coupled plasma CVD", Appl. Surf. Sci., Vol. 244 No. 1-4, pp. 12-15, (2005).
[MH-2]K. Makihara, H. Deki, H. Murakami, S. Higashi and S. Miyazaki, "Control of the nucleation density of Si quantum dots by remote hydrogen plasma treatment ", Appl. Surf. Sci., Vol. 244 No. 1-4, pp. 75-78, (2005).
[MH-3] N. Kosku, H. Murakami, S. Higashi and S. Miyazaki, "Influence of substrate dc bias on crystallinity of silicon films grown at a high rate from inductively-coupled plasma CVD", Appl. Surf. Sci., Vol. 244 No. 1-4, pp. 39-42, (2005).
[MH-4] H. Kaku, S. Higashi, H. Taniguchi, H. Murakami and S. Miyazaki, "A new crystallization technique of Si films on glass substrate using thermal plasma jet", Appl. Surf. Sci., Vol. 244 No. 1-4, pp. 8-11, (2005).
[MH-5] K. Makihara, Y. Okamoto, H.Murakami, S.Higashi and S.Miyazaki, " Characterization of germanium nanocrystallites grown on SiO2 by a conductive AFM probe technique ", IEICE Trans. on Electronics, Vol. E88-C No. 4, pp. 705-708, (2005).
[MH-6] T. Shibaguchi, M. Ikeda, H. Murakami and S. Miyazaki, "Charging and Discharging Characteristics of

Stacked Floating Gates of Silicon Quantum Dots", IEICE Trans. on Electronics, Vol. E88-C No. 4, pp. 709-712, (2005).
[MH-7] H. Murakami, W. Mizubayashi, H. Yokoi, A. Suyama and S. Miyazaki, "Electrical Characterization of Aluminum Oxynitride Stacked Gate Dielectrics Prepared by a Layer-by-Layer Process of Chemical Vapor Deposition and Rapid Thermal Nitridation", IEICE Trans. on Electronics, Vol. E88-C No. 4, pp. 640-645, (2005).
[MH-8] H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi and S. Miyazaki, "Characterization of Atom Diffusion in Polycrystalline Si/SiGe/Si Stacked Gate", IEICE Trans. on Electronics, Vol. E88-C No. 4, pp. 646-650, (2005).
[MH-9] S. Higashi, H. Kaku, H. Murakami, S. Miyazaki, H. Watakabe, N. Ando and T. Sameshima, "Application of Plasma Jet Crystallization Technique to Fabrication of Thin-Film Transistor ", Japanese J. of Applied Physics, Vol. 44 No. 3, pp. L108-L110, (2005).
[MH-10] S. Higashi, H. Kaku, H. Taniguchi, H. Murakami and S. Miyazaki, " Crystallization of Si Films on Glass Substrate Using Thermal Plasma Jet ", Thin Solid Films, Vol. 487, pp. 122-125, (2005).
[MH-11] S. Nagamachi, A. Ohta, F. Takeno, H. Nakagawa, H. Murakami, S. Miyazaki, T. Kawahara and K. Torii, "Analysis of Leakage Current through Al/HfAlOx/SiONx/Si(100) MOS Capacitors", Trans. of the Mat. Res. Soc. Of Japan , Vol. 30 No. 1, pp. 197-200, (2005).
[MH-12] Y. Pei, S. Nagamachi, H. Murakami, S. Higashi, S. Miyazaki, T. Kawahara and K. Torii, " Electrical Characterization of HfAlOx/SiON Dielectric Gate Capacitors ", Trans. of the Mat. Res. Soc. of Japan , Vol. 30 No. 1, pp. 205-208, (2005).
[MH-13] F. Takeno, A. Ohta, S. Miyazaki, K. Komeda, M. Horikawa and K. Koyama, " Impact of Rapid Thermal Anneal on ALCVD-Al2O3/Si3N4/Si(100) Stack Structures-Photoelectron Spectroscopy ", Trans. of the Mat. Res. Soc. Of Japan , Vol. 30 No. 1, pp. 213-217, (2005).
[MH-14] H. Kaku, S. Higashi, S. Miyazaki, M. Asami, H. Watakabe, N. Andoh and T. Sameshima, " Fabrication of Polycrystalline Si Thin Film Transistor Using Plasma Jet Crystalliztion Technique ", Trans. of the Mat. Res. Soc. Of Japan , Vol. 30 No. 1, pp. 283-286, (2005).
[MH-15] N. Kosku and S. Miyazaki, " High-Rate Growth of Highly-Crystallized Si Films from VHF Inductively-Coupled Plasma CVD ", Trans. of the Mat. Res. Soc. of Japan , Vol. 30 No. 1, pp. 279-282, (2005).
[MH-16] Y. Pei, S. Nagamachi, H. Murakami, S. Higashi, S. Miyazaki, T. Kawahara, K. Torii and Y. Nara, " Characterization of Charge Trapping and Dielectric Breakdown of HfAlO_X/SiON Dielectric Gate Stack ", Dielectric and semiconductor materials, devices, and processing, Physics and Chemistry of SiO2 and the Si SiO2 Interface-5, Vol. 1, No. 1, pp. 163-172, (2005).
[MH-17] Y. Darma, Hideki Murakami and S. Miyazaki, " Influence of Thermal Annealing on Compositional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core ", Appl. Surf. Sci., Vol. 224, pp. 156-159, (2004).
[MH-18] A. Ohta, H. Nakagawa, H. Murakami, S. Higashi, T, Kawahara, K. Torii and S. Miyazaki, " Impact of Rapid Thermal O2 Anneal on Dielectric Stack Structures of Hafnium Aluminate and Silicon Dioxide Formed on Si(100) ", Jpn. J. Appl. Phys., Vol. 43 No. 11B, pp. 7831-7836, (2004).
[MH-19] H. Nakagawa, A. Ohta, F. Takeno, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki, " Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on NH3-nitrided Si(100) ", Jpn. J. Appl. Phys., Vol. 43 No. 11B, pp. 7890-7894, (2004).
[MH-20] A. Ohta, M. Yamaoka and S. Miyazaki, "Photoelectron Spectroscopy of ultrathin yttrium oxide films on Si(100), " Microelec. Eng., Vol. 72, pp. 154-159, (2004).
[MH-21] K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki, " Electricalcharacterization of Ge microcrystallites by atomic force microscopy using a conducting probe ", Thin Solid Films ,Vol. 457, pp. 103-108, (2004).
[MH-22] S. Miyazaki, M. Narasaki A. Suyama M. Yamaoka and H. Murakami, " Electronic Structure and Energy BandOffsets for Ultrathin Silicon Nitride on Si(100) ", Appl. Surf. Sci. , Vol. 216/1-4, pp. 252-257, (2003).
[MH-23] M. Yamaoka, H. Murakami and S. Miyazaki, " Diffusion and Incorporation of Zr into Thermally-Grown SiO2 on
Si(100) ", Appl. Surf. Sci. , Vol. 216/1-4, pp. 223-227, (2003).
[MH-24] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, " Multiple-Step Electron Charging in Silicon-Quantum-DotFloating Gate Metal-Oxide-Semiconductor Memories ", Jpn. J. Appl. Phys., Vol. 42 No. 6B, pp. 4134-4137, (2003) .

[MH-25] Y. Darma, H. Murakami and S. Miyazaki, “ Formation of Nanometer Silicon Dots with Germanium Core byHighly-Slective Low-Pressure Chemical Vapor Deposition ”, Jpn. J. Appl. Phys., Vol. 42 No. 6B, pp. 41294133, (2003).

[MH-26] Y. Darma, R. Takaoka, H. Murakami and S. Miyazaki, “ Self-assembling formation of silicon quantum dots with agermanium core by low-pressure chemical vapor deposition ”, Nanotechnology , Vol. 14, pp. 413-415, (2003).

[MH-27] N. Kosku, F. Kurisu, M. Takegoshi, H. Takahashi and S. Miyazaki, “ High-rate deposition highly crystallizedsilicon films from inductively coupled plasma ”, Thin Solid Films , Vol. 435, pp. 39-43, (2003).

[MH-28] S. Miyazaki, "Characterization of High-k Gate Dielectric/Silicon Interfaces, “ Appl. Surf. Sci., Vol. 190/14, pp. 66-74, (2002).

[MH-29] S. Miyazaki, H. Takahashi, H. Yamashita, M. Narasaki and M. Hirose, “ Growth and Characterization ofMicrocrystalline Silicon-Germanium Films ”, J. Non-Cryst. Solid, Vol. 299-302 Part I, pp. 148-152, (2002).

[MH-30] H. Murakami, T. Mihara, S. Miyazaki and M. Hirose, "Carrier Depletion Effect in the n+Poly-Si Gate SideWall/SiO2 Interfaces as Evaluated by Gate Tunnel Leakage Current ”, Jpn. J. Appl. Phys., Vol. 41 No. 5A, pp.L512-L514, (2002).

[MH-31]W. Mizubayashi, Y. Yoshida, S. Miyazaki and M. Hirose, “ Quantitative Analysis of Oxide Voltage and FieldDependence of Time-Dependent Dielectric Soft Breakdown and Hard Breakdown in Ultrathin Gate Oxides ”, Jpn. J.Appl. Phys., Vol. 41 No. 4B, pp. 2426-2430, (2002).

[MH-32]S. Miyazaki, M. Narasaki, M. Ogasawara and M. Hirose, “ Chemical and Electronic Structure of UltrathinZirconium Oxide Films on Silicon as Determined by Photoelectron Spectroscopy ”, Solid State Electronics , Vol.16, pp. 1679-1685, (2002).

国際会議リスト(宮崎, 東グループ)

[MH-C-1] S. Miyazaki, “ Characterization of Electric Charged States of Silicon Nanocrystals as a Floating Gate in MOSStructure ”, Mat. Res. Soc. Symp. Proc, pp. 249-254, (2005). (Invited)

[MH-C-2] S. Miyazaki, “ Self-Assembling Formation of Si-based Quantum Dots and Control of Their Electric Charged Statesfor Multi-valued Memories ”, SPIE conference on Nanofabrication: Technologies, Devices, and Applications II(SA111) at Optics East(Oct.23-26, Boston), (2005) . [No. OE05-SA111-41](Invited)

[MH-C-3] S. Miyazaki, “ Control of Charged States of Silicon-Based Quantum Dots and Its Application to Floating Gate MOSMemories ”, Abst. of First Int. Workshop on New Group IV Semiconductor Nanoelectronics (May 27-28), pp. 39-40, (2005). [Session V-2](Invited)

[MH-C-4] K. Makihara, J. Xu, H. Deki, Y. Kawaguchi, H. Murakami, S. Higashi and S. Miyazaki, “ Fabrication of MultiplyStacked Structures Consisting of Si-QDs with Ultrathin SiO2 and Its Application of Light Emitting Diodes ”, Abst.of First Int. Workshop on New Group IV Semiconductor Nanoelectronics (May 27-28, Sendai), (2005), pp. 47-48, (2006). [P-13].

[MH-C-5] T. Okada, S. Higashi, H. Kaku, H. Murakami and S. Miyazaki, “ Analysis of Transient Temperature Profile DuringThermal Plasma Jet Annealing of Si Films on Quartz Substrate ”, Dig. of Tech. Papers 2005 Int. Workshop onActive-Matrix Liquid-Crystal Displays (July 6-8, Kanazawa), pp. 171-174, (2005). [TFTp1-3]

[MH-C-6] K. Makihara, Y. Kawaguchi, H. Murakami, S. Higashi and S. Miyazaki, “ The Application of Maltiple-Stacked SiQuantum Dots to Light Emitting Diodes ”, 2005 Asia-Pacific Workshop on Fundamentals and Applications ofAdvanced Semiconductor Devices (June 28-30, Seoul, Korea), pp. 173-176, (2005). [A9.3]

[MH-C-7] T. Nagai, M. Ikeda, Y. Shimizu, S. Higashi and S. Miyazaki, “ Characterization of MaltiStep Electron Charging toSilicon-Quantum-Dot Floating Gate by Applying Pulsed Gate Biases ”, Ext. Abst. of The 2005 Int. Conf.on Solid State Devices and Materials, pp. 174-175, (2005). [G-2-6]

[MH-C-8] Y. Pei, S. Nagamachi, H. Murakami, S. Higashi, S. Miyazaki, “ Characterization of Charge Trapping andDielectric Breakdown of HfAlOX/SiON Dielectric Gate Stack ”, The Electrochemical Society, 208th Meeting (Oct.16-21, Los Angeles, U.S.A), pp. 163-172, (2005). [J1-739]

[MH-C-9] H. Kaku, S. Higashi, T. Okada, H. Murakami and S. Miyazaki, “ Phase Transformation of Amorphous Si Films inMillisecond Time Domain Induced by Thermal Plasma Jet Irratiation ”, Abst. of The 18th Symposium on PlasmaScience for Materials (June 28-29, Tokyo), pp. 17-18, (2005). [B1-9]

[MH-C-10] S. Miyazaki, “ Control of Charged States of Silicon Quantum Dots and Their Application to

Floating Gate MOSMemories and Light Emitting Diodes ", Ext. Abst. of the 4th Hiroshima Int. Workshop on 21th Century COE,Nanoelectronics for Tera-bit Information Processing (Sep. 16, Hiroshima), pp. 92-93, (2005). [P-30]

[MH-C-11] H. Murakami, F. Takeno, A. Ohta, S. Higashi, S. Miyazaki, K. Komeda, M. Horikawa and K. Koyama, " Impact ofRapid Thermal Annealing on ALCVD-Al2O3/Si3N4/Si(100) Stack Structures -Photoelectron Spectroscopy ", Ext.Abst. of the 4th Hiroshima Int. Workshop on 21th Century COE, Nanoelectronics for Tera-bit InformationProcessing (Sep. 16, Hiroshima), pp. 94-95, (2005). [P-31]

[MH-C-12] S. Higashi, T. Okada, N. Fujii, N. Koba, H. Murakami and S. Miyazaki, " Formation of Si Nano-crystals byMillisecond Annealing of SiOX Films using Thermal Plasma Jet ", Ext. Abst. of the 4th Hiroshima Int. Workshop on 21th Century COE, Nanoelectronics for Tera-bit Information Processing (Sep. 16, Hiroshima), pp. 9697, (2005). [P-32]

[MH-C-13] S. Miyazaki, " Control of Discrete Charged States in Si-Based Quantum Dots and Its Application to Floating GateMemories ", Int. Symp. on Surface Science and Nanotechnology (November 14-17, Omiya, Saitama), (2005).[Th-A6(I)](Invited).

[MH-C-14] T.Okada, S.Higashi, H.Kaku, N.Koba, H.Murakami and S.Miyazaki, " Control of Substrate Surface Temperaturein Millisecond Annealing Technique Using Thermal Plasma Jet ", Proceedings of Int. Symposium on DryProcess(November 28-30, Jeju), pp. 405-406, (2005).

[MH-C-15] T.Okada, S.Higashi, H.Kaku, N.Koba, H.Murakami and S.Miyazaki, " Analysis of Transient Temperature ProfileDuring Thermal Plasma Jet Annealing of Si Films on Quartz Substrate ", Extended Abstracts of the Fourth Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing (Septempber 16), pp. 114-115, (2005).

[MH-C-16] K. Makihara, J. Xu, H.Deki, Y. Kawaguchi, H. Murakami, S. Higashi and S. Miyazaki, " Light Emitting Devices from Multilayered Si Quantum Dots Structures ", Abst. of 2005 Int. Meeting for Future of Electron Devices(Kyoto, April 11-13), pp. 93-94, (2005). [P-D5]

[MH-C-17] H. Kaku, S. Higashi, T. Okada, H. Murakami, S. Miyazaki, H. Watakabe, N. Andoh and T. Sameshima, " Fabrication of Polycrystalline Si Thin Film Transistor using Plasma Jet Crystallization Technique ", Abst. of 2005 Int. Meeting for Future of Electron Devices(Kyoto, April 11-13), pp. 91-92, (2005). [P-D4]

[MH-C-18] S. Miyazaki, " Control of Discrete Charged States in Si-Based Quantum Dots and Its Application to Floating Gate Memories ", The 4th Int. Symp. Surface Science and Nanotechnology (ISSS-4, November 14 - 17), (2005). (Invited)

[MH-C-19] K. Makihara, J. Xu, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki, " Characterization of Electronic Charged States of P-doped Si Quantum Dots Using AFM/Kelvin Probe ", Abst. of The Fourth Int. conf. on Silicon Epitaxy and Heterostructures(ICSI-4)(Awaji Island, Hyogo, Japan, May 23-26), pp. 32-33, (2005). [23D-6]

[MH-C-20] S. Miyazaki, " Electron charging and discharging characteristics of Si-based quantum dots floating gate ", Abst. Of The Second Int. Symp. on Point Defects and Nonstoichiometry (ISPN-2, Kaohsiung, Taiwan, Oct 3-5), p. 19, (2005). [Th-A1-1](Invited)

[MH-C-21] Y. Pei, S. Nagamachi, H. Murakami, S. Higashi, S. Miyazaki, T. Kawahara and K. Torii, " Characterization of Charge Trapping and Dielectric Breakdown of HfAlOx/SiON Dielectric Gate Stack ", 207th Meeting of The Electrochemical Society(Quebec City, Canada, May 15-20), (2005) .

[MH-C-22] H. Nakagawa, F. Takeno, A. Ohta, H. Murakami, S. Higashi and S. Miyazaki, " Characterization of Chemical Bonding Features of NH3-Annealed Hafnium Oxides Formed on Si(100) ", 8th Atomically Controlled Surfaces, Interfaces and Nanostructures (ACSIN-8)(Stockholm, the Royal Capital of Sweden: June 19-23), (2005) .

[MH-C-23] S. Miyazaki, " High Rate Growth of Crystalline Si and Ge Films from Inductively-Coupled Plasma ", SREN 2005 Int. conf. on Solar Renewable Energy News, Low Energy Buildings, Research of Historical Artifacts(Florence, Italy, 2nd - 8th April), (2005). [Section 1-1](Invited)

[MH-C-24] A. Yamashita, Y. Okamoto, S. Higashi, S. Miyazaki, H. Watakabe and T. Sameshima, " In-Situ Observation of Rapid Crystalline Growth Induced by Excimer Laser Irradiation to Ge/Si Stacked Structure ", Abst. of The Fourth Int. conf. on Silicon Epitaxy and Heterostructures(ICSI-4)(Awaji Island, Hyogo, Japan, May 23-26), pp. 44-45, (2005). [24F-2]

[MH-C-25] N. Kosku and S. Miyazaki, " HIGH-RATE GROWTH OF HIGHLY-CRYSTALLIZED Si FILMS FROM VHF INDUCTIVELY-COUPLED PLASMA CVD ", The European Materials Research

Society (EMRS)(Palais de la Musique et des Congres Strasbourg, France - May 31 to June 3), (2005). [F/PII.08]

[MH-C-26] S. Miyazaki, " Self-Assembling Formation of Si-based Quantum Dots and Control of Their Electric Charged States for Multi-valued Memories ", SPIE conference on Nanofabrication: Technologies, Devices, and Applications II (SA111) at Optics East(Oct.23-26, Boston), (2005). [No. OE05-SA111-41](Invited)

[MH-C-27] S. Miyazaki, " Control of Charged States of Silicon-Based Quantum Dots and Its Application to Floating Gate MOS Memories ", Abst. of First Int. Workshop on New Group IV Semiconductor Nanoelectronics (May 27-28, Sendai), (2005). [Session V-2](Invited)

[MH-C-28] K. Makihara, J. Xu, H. Deki, Y. Kawaguchi, H. Murakami, S. Higashi and S. Miyazaki, " Fabrication of Multiply-Stacked Structures Consisting of Si-QDs with Ultrathin SiO2 and Its Application of Light Emitting Diodes ", Abst. of First Int. Workshop on New Group IV Semiconductor Nanoelectronics (May 27-28, Sendai), pp. 47-48, (2006). [P-13]

[MH-C-29] K. Makihara, Y. Kawaguchi, H.Murakami, S.Higashi and S.Miyazaki, " The Application of Multiple-Stacked Si Quantum Dots to Light Emitting Diodes ", Abst. of 2005 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, (2005).

[MH-C-30] S. Miyazaki, T. Shibaguchi and M. Ikeda, " Characterization of Electronic Charged States of Silicon Nanocrystals as a Floating Gate in MOS Structures ", Mat. Res. Soc. Symp. Proc., Vol. 830(2005)p. D5.8.

[MH-C-31] F. Takeno, A. Ohata and S. Miyazaki, " Impact of Rapid Thermal Anneal on ALCVD-Al2O3/Si3N4/Si(100) Stack Structures - Photoelectron Spectroscopy ", Abst. of The 15th Symp. of The Materials Reserch Society of Japan (Tokyo, Dec. 23-24), pp. 129, (2004). [G1-O08-M]

[MH-C-32] S. Higashi, H. Kaku, H. Taniguchi, H. Murakami and S. Miyazaki, " Crystallization of Si Films on Glass Substrate Using Thermal Plasma Jet ", Int. Conf. Polycrystalline Semiconductors 2004 (Potsdam, Germany, September 5-10), in series to be published in Thin Solid Films, (2004) .

[MH-C-33] S. Higashi, H. Kaku, H. Murakami, S. Miyazaki, M. Asami, H. Watakabe, N. Ando and T. Sameshima, " Crystallization of Si Thin Film Using Thermal Plasma Jet and Its Application to Thin-Film Transistor Fabrication ", Proc. Int. Workshop on Active-Matrix Liquid-Crystal Displays 2004, (Tokyo Japan, August 25-27), pp. 179-180, (2004).

[MH-C-34] H. Kaku, S.Higashi, H.Taniguchi, H.Murakami and S.Miyazaki, " A new crystallization technique of Si flms on glass substrate using thermal plasma jet ", Abst. of 12th Int. conf. on Solid Films and Surfaces (Hamamatsu, June 21-25), pp. 7, (2004). [A1-4]

[MH-C-35] K. Makihara, H. Deki, H. Murakami, S. Higashi and S. Miyazaki, " Control of the Nucleation Density of Si Quantum Dots by Remote Hydrogen Plasma Treatment ", Abst. of 12th Int. conf. on Solid Films and Surfaces (Hamamatsu, June 21-25), pp. 137, (2004). [A5-2]

[MH-C-36] N. Kosku, H. Murakami, S. Higashi and S. Miyazaki, " Influence of Substrate DC Bias on Crystallinity of Si Films Grown at a High Rate from Inductively-Coupled Plasma CVD ", Abst. of 12th Int. conf. on Solid Films and Surfaces (Hamamatsu, June 21-25), pp. 202, (2004). [P2-26]

[MH-C-37] Y. Okamoto, K. Makihara, S.Higashi and S.Miyazaki, " Formation of Microcrystalline Germanium(μc-Ge:H) Films from Inductively-Coupled Plasma CVD ", Abst. of 12th Int. conf. on Solid Films and Surfaces (Hamamatsu, June 21-25), pp. 10, (2004). [A2-3]

[MH-C-38] K. Makihara, H. Nakagawa, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki, " Fabrication of Multiply Stacked Structures of Si Quantum-Dots Embedded in SiO2 by Combination of Low-Pressure CVD and Remote Plasma Treatments ", Dig. of Papers 2003 Int. Microprocesses and Nanotechnol. Conf. (Tokyo, October 27-29), pp. 216-217, (2004). [28P-6-68L]

[MH-C-39] K. Makihara, Y. Okamoto, H. Murakami, S. Higashi and S. Miyazaki, " Characterization of Germanium Nanocrystallites Grown on SiO2 by a Conductive AFM Probe Technique ", Ext. Abst. of 2004 Asia-Pacific Workshop on Fundamentals and Application of Advanced Semiconductor Devices (Nagasaki, June 30-July 2), pp. 277-280, (2004). [A10.5]

[MH-C-40] T. Shibaguchi, M. Ikeda, H. Murakami and S. Miyazaki, " Charging and Discharging Characteristics of Stacked Floating Gates of Silicon Quantum Dots ", Ext. Abst. of 2004 Asia-Pacific Workshop on Fundamentals and Application of Advanced Semiconductor Devices (Nagasaki, June 30-July 2), pp. 273-276, (2004). [A10.4]

[MH-C-41] H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi and S. Miyazaki, " Characterization of Atom Diffusion in Polycrystalline Si/SiGe/Si Stacked Gate ", Ext. Abst. of

2004 Asia-Pacific Workshop on Fundamentals and Application of Advanced Semiconductor Devices (Nagasaki, June 30-July 2), pp. 189-193, (2004). [B6.3]

[MH-C-42] M. Sugimura, A. Ohta, H. Nakagawa, T. Shibaguchi, S. Higashi and S. Miyazaki, " Evaluation of Electronic Defect States at Poly-Si/HfO2 interface by Photoelectron Yield Spectroscopy ", Ext. Abst. of 2004 Int. Conf. on Solid State Devices and Materials (Tokyo, September 15-17), pp. 792-793, (2004). [C-9-4]

[MH-C-43] T. Nagai, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki, " Photo-Induced Electron Charging to Silicon Quantum-Dot Floating Gate in Metal-Oxide-Semiconductor Memories ", Ext. Abst. of 2004 Int. Conf. on Solid State Devices and Materials (Tokyo, September 15-17), pp. 126-127, (2004). [H-2-4]

[MH-C-44] A. Ohta, S. Miyazaki, H. Murakami, T. Kawahara and K. Torii, " Impact of Rapid Thermal O2-Anneal on Dielectric Stack Structures of Hafnium Aluminate and Silicon Dioxide Formed on Si(100) ", Ext. Abst. of 2004 Int. Workshop on DIELECTRIC THIN FILMS FOR FUTURE ULSI DEVICES: SCIENCE AND TECHNOLOGY (Tokyo, May 26-28), pp. 97-98, (2004).

[MH-C-45] H. Nakagawa, A. Ohta, F. Takeno, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki, " Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on NH3-nitrided Si(100) ", Ext. Abst. of 2004 Int. Workshop on DIELECTRIC THIN FILMS FOR FUTURE ULSI DEVICES: SCIENCE AND TECHNOLOGY (Tokyo, May 26-28), pp. 35-36, (2004).

[MH-C-46] S. Miyazaki, T. Shibaguchi and M. Ikeda, " Characterization of Electronic Charged States of Silicon Nanocrystals as a Floating Gate in MOS Structures ", Abst. of 2004 MRS Fall Meeting (Boston, U.S.A., Nov. 29-Dec. 3), (2004). [D5.8]

[MH-C-47] N. Kosku and S. Miyazaki, " High-Rate Growth of Highly-Crystallized Si Films from VHF Inductively-Coupled Plazma CVD ", Proc. of 4th Int. Symp. on Dry Process (Tokyo, Nov. 30-Dec.1), pp. 145-150, (2004). [P-25]

[MH-C-48] S. Miyazaki, T. Shibaguchi and M. Ikeda, " Characterization of Charged States of Si Quantum Dots Floating Gate in MOS Structures ", Abst. of Electrochemical Society-Int. Symp. on Nanoscale Devices and Materials (Hawai, Oct. 3-8), (2004). [No. 1013]

[MH-C-49] W. Mizubayashi, Y. Yoshida, H. Murakami, S. Miyazaki and M. Hirose, " Statistical Analysis of Soft and Hard Breakdown in 1.9-4.8nm-thick Gate Oxides ", IEEE Electron Device Lett, Vol. 25 No. 5, pp. 305-307, (2004).

[MH-C-50] N. Kosku, S. Higashi and S. Miyazaki, " High-Rate Growth of Highly-Crystallized Si Films from VHF Inductively-Coupled Plazma CVD ", Abst. of Int. Union of Materials Research Societies-Int. Conf. in Asia (Hsinchu, Taiwan, Nov. 16-18), pp. 176, (2004). [E-O-08]

[MH-C-51] S. Miyazaki, " Characterization of Charged States of Silicon-based Quantum Dots and Its Application to Floating Gate MOS Memories ", Abst. of Int. Union of Materials Research Societies-Int. conf. in Asia-(Hsinchu, Taiwan, Nov. 16-18), pp. 208, (2004). [F-I-08](Invited)

[MH-C-52] S. Miyazaki, " Characterization of Charged States of Silicon-based Quantum Dots and Its Application to Floating Gate MOS Memories ", Proc. of Int. Union of Materials Research Societies-Int. conf. in Asia-(Hsinchu, Taiwan, Nov. 16-18), pp. F231, (2004).

[MH-C-53] W. Mizubayashi and S. Miyazaki, " Analysis of Soft Breakdown of 2.6-4.9nm-Thick Gate Oxides ", Jpn. J. Appl. Phys., Vol. 43 No. 10(2004)pp. 6925-6929.

[MH-C-54] S. Miyazaki, " Electrical Charging Characteristics of Silicon Dots Floating Gates in MOS Devices ", Proc. of 7th China-Japan Symp. on Thin Films (Chengdu Sichuan, China, September 20-22), pp. 7-10, (2004). [3](Invited)

[MH-C-55] S. Miyazaki, " Charging/Discharging Characteristics of Silicon Quantum Dots and Their Application to Memory Devices ", Abst. of The 2004 Joint conf. of The 7th Int. conf. on Advanced Surface Enginnering (ASE2004) and The 2nd Int. Conf. on Surface and Interface Science and Engineering (SISE 2004) FSISE 2004(Guangzhou , China, May 14-16), p. 138, (2004). [No. 270](Invited)

[MH-C-56] N. Kosku and S. Miyazaki, " Insights into High-Rate Growth of Highly-Crystallized Silicon Films from Inductively-Coupled Plasma of H2-diluted SiH4-Comparison between RF- and VHF-ICP ", The 3rd Asian conf. on Chemical Vapor Deposition (Taipei, Taiwan, Nov. 12-14), p. 52, (2004). [A21]

[MH-C-57] K. Makihara, K. Takeuchi, M. Ikeda, H. Murakami and S. Miyazaki, " Characterization of nucleation and growth of Ge microcrystallites by AFM (Atomic Force Microscopy) with a conducting probe ", Proc. 20th Symp. On Plasma Processing (Nagaoka, Jan 29-31), pp. 321-322, (2003). [P2-48]

[MH-C-58] N. Kosku and S. Miyazaki, " Microcrystalline Silicon Films Form Inductively-coupled Plasma ", Proc. 20th Symp. on Plasma Processing (Nagaoka, Jan 29-31), pp. 319-320, (2003). [P2-47]

[MH-C-59] A. Ohta, M. Yamaoka and S. Miyazaki, " Photoelectron Spectroscopy of Ultrathin Yttrium Oxide Films on Si(100) ", 13th Bi-annual Conf. on Insulating Films on Semiconductors (Barcelona, June18-20), (2003). [GS20]

[MH-C-60] K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki, " Electrical Characterization
of Ge Microcrystallites by Atomic Force Microscopy Using a Conduncing Probe ", 16th symp. on Plasma Science
for Materials (Tokyo, June 4-5), p. 115, (2003). [B6-3]

[MH-C-61] N. Kosku, H. Murakami and S. Miyazaki, " High-Rate Deposition of Highly-Crystallized Silicon Films From Inductively-Coupled Plasma ", 16th symp. on Plasma Science for Materials (Tokyo, June 4-5), p. 114, (2003). [B6-2]

[MH-C-62] Y. Darma, H. Murakami and S. Miyazaki, " Infuence of Thermal Annealing on Compotional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core", Ext. Abst. of 1st Int. SiGe Technology and Device Meeting (Nagoya, Jan. 15-17), pp. 209-210, (2003). [P2-45]

[MH-C-63] K. Makihara, Y. Okamoto, H. Nakagawa, M. Ikeda, H. Murakami and S. Miyazaki, " Local Characterization of Electronic Transport in Microcrystalline Germanium Thin Films by Atomic Force Microscopy Using a Conducting Probe ", Proc. 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (Busan, June 30-July2), pp. 37-40, (2003). [2.4]

[MH-C-64] Y. Darma and S. Miyazaki, " Thermal Stability of Nanometer Dot Consisting of Si Clad and Ge Core as Detected by Raman and Photoemission Spectroscopy", Proc. 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (Busan, June 30-July2), pp. 145-149. (2003). [7.3]

[MH-C-65] T. Shibaguchi, Y. Shimizu, M. Ikeda, H. Murakami and S. Miyazaki, " Analysis of Charging Characteristics in MOSFETs with a Si-Quantum-Dots Floating Gate ", Proc. 2003 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (Busan, June 30-July2), pp. 151-154, (2003). [7.4]

[MH-C-66] M. Ikeda, Y. Shimizu, T. Shibaguchi, H. Murakami and S. Miyazaki, " Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs ", Ext. Abst. of 2003 Int. Conf. on Solid State Devices and Materials (Tokyo, September 16-18), pp. 846-847, (2003). [E-9-1]

[MH-C-67] M. Yamaoka, A. Ohta and S. Miyazaki, " Characterization of Hafnium Diffusion into Thermally-Grown SiO2 on Si(100) ", Ext. Abst. of 2003 Int. Conf. on Solid State Devices and Materials (Tokyo, September 16-18), pp. 810-811, (2003). [D-8-3L]

[MH-C-68] Y. Darma, K. Takeuchi and S. Miyazaki, " Electronic Charged States of Single Si Quantum Dots with Ge Core as Detected by AFM/Kelviin Probe Technique ", Ext. Abst. of 2003 Int. Conf. on Solid State Devices and Materials (Tokyo, September 16-18), pp. 300-301, (2003). [E-3-3]

[MH-C-69] Y. Darma and S. Miyazaki, " Characterization of Electronic Transport Through Si Dot with Ge Core Using AFM Conducting Probe ", Dig. of Papers 2003 Int. Microprocesses and Nanotechnology Conf. (Tokyo, October 29-31), pp. 22-23, (2003). [29B-2-3]

[MH-C-70] A. Sakai, S. Sakashita, M. Sakashita, S. Zaima, Y. Yasuda and S. Miyazaki, " Praseodymium silicate formation by post-growth high-temperature aneeling ", Abst. of 2003 MRS Fall Meeting (Boston, U.S.A., Dec. 1-4) (2003) [E3.23].

[MH-C-71] A. Ohta, M. Yamaoka, S. Miyazaki, A. Ino, M.Taniguchi, H Namatame, M. Nakatake, A. Kimura and H. Sato, " Photoelectron Spectroscopy of Ultrathin Yttrium Oxide Films on Silicon ", 7th Hiroshima Int. Symp. On Synchrotron Radiation (Higashi-Hiroshima, March 13-14), p. 218, (2003). [P13]

[MH-C-72] S. Miyazaki, " Photoemission Study of High-k Gate Dielectric/Si(100) Heterostructures - Chemical Bonding Features and Energy Band Alignment ", Abst. of American Vacuum Society 50th Inter. Symp. and Exhibition (Baltimore U.S.A, Nov. 3), (2003). [DI-MoM7](Invited)

[MH-C-73] S. Miyazaki, H. Yamashita, H. Nakagawa and M. Yamaoka, " Photoemission Study of Interfacial Oxidation in ZrO2/Sub-Nanometer SiONx/Si(100) Stacked ", Mat. Res. Soc. Symp. Proc., Vol. 747, pp. 281-286, (2003).

[MH-C-74] H. Nakagawa, A. Ohta, F. Takeno, H. Murakami and S. Miyazaki, " Characterization of Interfacial Oxide Layers in Heterostructures of Zirconium Oxides Formed on Si(100) and NH3-nitrided Si(100) surfaces ", Abst. of The 7th Int. Conf. on Atomically Controlled Surfaces,

Interfaces and Nanostructures (Nara, November 16-20), p. 253, (2003) [20D72]

[MH-C-75] A. Ohta, S. Miyazaki, H. Murakami, T. Kawahara and K. Torii, " Characterization of Dielectric Stack Structures of Hafnium Aluminate and Silicon Dioxide formed on Si(100) ", Abst. of The 7th Int. Conf. on Atomically Controlled Surfaces, Interfaces and Nanostructures (Nara, November 16-20), p. 255, (2003). [20D74]

[MH-C-76] Y. Darma, R. Takaoka, H. Murakami and S. Miyazaki, " Self-Assembling Formation of Silicon Quantum Dot with Germanium Core by LPCVD ", Proc. 2002 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices(Sapporo, July 1-3), pp. 307-310, (2002). [7.9]

[MH-C-77] S. Miyazaki, H. Yamashita, H. Nakagawa and M. Yamaoka, " Photoemission Study of Interfacial Oxidation in ZrO2/Sub-Nanometer SiONx/Si(100) Stacked ", Abst. of 2002 MRS Fall Meeting (Boston, Dec. 2-6), (2002). [V3.7].

MH-C-78] S. Miyazaki, H. Takahashi, M. Sagara and M. Hirose, "Growth and Characterization of Amorphous and Microcrystalline Silicon-Germanium Films", Abst. of 2002 MRS Spring Meeting (San Francisco, April 4), (2002). [A18.1](Invited)

[MH-C-79] S. Miyazaki, "Self-Assembling of Si quantum Dots and Their Application to Memory Devices ", Abst. of The 2nd Vacuum & Surface Sciences conf. of Asia and Australia (Hong Kong, August 26-30, 2002) (2002) [Mo7](Invited).

[MH-C-80]M. Yamaoka, H. Murakami and S. Miyazaki, "Diffusion and Incorporation of Zr into Thermally-Grown SiO2 on Si(100) ", 4th Int. Symp. on Control of Semiconductor Interfaces (Karuizawa, Oct. 21-25), (2002). [A4-3]

[MH-C-81] S. Miyazaki, M. Narasaki and H. Murakami, "Electronic Structure and Energy Band Offsets for Ultrathin Silicon Nitride on Si(100) ", Abst. of 4th Int. Symp. on Control of Semiconductor Interfaces (Karuizawa, Oct. 21-25), (2002). [A5-3]

[MH-C-82] M. Ichioka, S. Miyazaki, M. Taniguchi, H. Namatame, A. Kimura and H. Sato, "Characterization on As+ Heavily-Implanted Layer on Si(100) by X-ray Photoelectron Spectroscopy", 6th Hiroshima Int. Symp. On Synchrotron Radiation (Higashi-Hiroshima, March 14), (2002). [P-11]

[MH-C-83] A. Suyama, H. Yokoi, M. Narasaki, W. Mizubayashi, H. Murakami and S. Miyazaki, "Photoemission Study of Aluminum Oxynitride/Si(100) Heterostructures-Chemical Bonding Features and Energy Band Lineup", Ext. Abst. of Inter. Conf. on Solid State Devices and Materials (Nagoya, Sept. 17-19), pp. 307-310, (2002). [C-8-3]

[MH-C-84] H. Murakami, W. Mizubayashi, H. Yokoi, A. Suyama and S. Miyazaki, "Electrical Characterization of Aluminum-Oxynitride Stacked Gate Dielectrics Prepared by a Layer-by-Layer Process of Chemical Vapor Deposition and Rapid Thermal Nitridation", Ext. Abst. of Inter. Conf. on Solid State Devices and Materials (Nagoya, Sept. 17-19), pp. 712-713, (2002). [B-7-1]

[MH-C-85] S. Miyazaki, "Self-Assembling of Si Quantum Dots and Their Application to Memory Devices", Abst. of Int. Conf. on Polycrystalline Semiconductors (Nara, Sept. 10-13), p. 56, (2002). [105](Invited)

[MH-C-86] Y. Darma, H. Murakami and S. Miyazaki, " Formation of Nanometer Silicon Dots with Germanium Core by Highly-Selective Low-Pressure Chemical Vapour Deposition", Dig. of Papers Int. Microprocesses and Nanotechnology Conf. (Tokyo, Nov. 6-8), pp. 58-59, (2002). [7B-4-2]

[MH-C-87] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, " Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate MOS Memories ", Dig. of Papers Int. Microprocesses and Nanotechnology Conf. (Tokyo, Nov. 6-8), pp. 116-117, (2002). [7P-7-10]

[MH-C-88] M. Yamaoka, M. Narasaki, H. Murakami and S. Miyazaki, " Photoemission Study of Ultrathin Hafnium Oxide Films Evaporated on Si(100) ", Semiconductor Technology: Proc. of Int. Smiconductor Technology Conf. (Tokyo, Sept. 12-14), pp. 229-236, (2002).

[MH-C-89] K. Takeuchi, H. Murakami and S. Miyazaki, " Electronic Charging State of Si Quantum Dots formed on Ultrathin SiO2 as Evaluated by AFM/Kelvin Probe Method ", Semiconductor Technology: Proc. of Int. Smiconductor Technology Conf. (Tokyo, Sept. 12-14), pp. 1-8, (2002). [33]

[MH-C-90] N. Kosku, F. Kurisu, M. Takegoshi, H. Takahashi and S. Miyazaki, " High-rate Deposition of Highly-crystallized Silicon Films from Inductively-coupled plasma ", Meeting Abst. of Joint Int. Plasma Symp. of 6th APCPST, 15th SPSM, and 11th KAPRA (Cheju, July 1-4), p. 131, (2002).

[MH-C-91] S. Miyazaki, "Characterization of Ultrathin Gate Dielectrics on Silicon by Photoelectron Spectroscopy", Proc of 2001 MRS Workshop Series - Alternatives on to SiO2 as Gate Dielectric

for Future Si-Based Microelectronics, pp. 8/1-7, (2002).

[MH-C-92] N. Kosku, F. Kurisu, H. Takahashi and S. Miyazaki, “High-rate deposition of highly-crystallized silicon films from inductively-coupled plasma”, Ext.Abst. of The 5th SANKEN Int. Symp. (Osaka, March 14), pp. 52-53, (2002). [P1.6]

[MH-C-93]S. Miyazaki and H. Murakami, “ Characterization of Deposition Process of Microcrystalline Silicon-Germanium Films: In-situ Infrared Attenuated Total Reflection and Ex-situ Raman Scattering Studies ”, Ext. Abst. of The 5th SANKEN Int. Symp. (Osaka, March 14), pp. 65-66, (2002). [P1.13](Invited).

特許ﾘｽﾄ (岩田, 佐々木グループ)

[IS-P-1] 画像の直交変換回路, 特願 2002-262316, 平成 14 年 9 月 9 日, 片山光亮、岩田穆

[IS-P-2] マッチングプロセッサ, 特願 2002-307455,平成 14 年 10 月 22 日, 山本美子、岩田穆

[IS-P-3] マッチングプロセッサ, 特願 2002-307479,平成 14 年 10 月 22 日, 山本美子、岩田穆

[IS-P-4] マッチングプロセッサ, 特願 2002-307739,平成 14 年 10 月 23 日, 山本美子、岩田穆

[IS-P-5] プログラマブル･アナログデジタル変換器, 特願 2002-367136, 平成 14 年 12 月 18 日, 岩田穆、山口圭治

[IS-P-6] プログラマブル A/D 変換器, 特願 2001-309280,平成 13 年 10 月 4 日, 岩田穆、山口圭治、森江隆, 永田真

[IS-P-7] 画像情報処理装置, 特願 2002-13464, 今村俊文、岩田穆、森江隆

[IS-P-8] 半導体装置, 特願 2003-117826, 平成 15 年 4 月 23 日, 吉川公麿、岩田穆、角南英夫、マタウシュハンス ユルゲン、横山新、芝原健太郎、中島安理、小出哲士、エービーエムハルンウルラシッド、渡邊慎治

[IS-P-9] アナログディジタル変換回路,特願 2004- 2449, 平成 16 年 1 月 7 日, 吉田毅、岩田穆、佐々木守、赤木美穂

[v10] 画像処理装置, 特願 2004-022317, 平成 16 年 1 月 28 日, 亀田成司、岩田穆、佐々木守、吉川公麿

[IS-P-11] データ転送回路, 特願 2005-061703, 平成 17 年 3.月 7 日, 岩田穆、今村俊文、村坂佳隆

[IS-P-12] 半導体装置, 特願 2004-10053, 平成 16 年 1 月 19 日, 佐々木守、岩田穆、有薗 大介、出願人：岩田穆

[IS-P-13] 信号伝達装置および信号伝達方法, 特願 2005-147216, 平成 17 年 5 月 19 日, 佐々木守、岩田穆、有薗大介、出願人：国立大学法人広島大学

[IS-P-14] 信号伝達方法, 特願 2005-147227, 平成 17 年 5 月 19 日, 佐々木守、岩田穆、有薗大介、出願人：国立大学法人広島大学

[IS-P-15] 半導体記憶装置, 特願 2005-152077, 平成 17 年 5 月 27 日, 池田博明、佐々木守、岩田穆、出願人：エルピーダメモリ株式会社、国立大学法人広島大学

[IS-P-16] アナログディジタル変換回路, 特願 2004-342508,平成 16 年 11 月 26 日, 吉田毅、岩田穆、佐々木守、赤木美穂、後藤邦彦

[IS-P-17] AB 級 CMOS 出力回路, 特願 2004-342421, 平成 16 年 11 月 26 日, 吉田毅、岩田穆、佐々木守、後藤邦彦

[IS-P-18] チョッパ増幅回路, 特願 2005-093683, 平成 17 年 3 月 29 日, 吉田毅、岩田穆、佐々木守、真下隆行、升井義博、中塚淳二

国際特許

[IS-P-19] Analog to digital converter circuit of successive approximation type operating at low voltage, 出願 US11/029492, 平成 17 年 1 月 6 日, Takeshi Yoshida, Atsushi Iwata, Mamoru Sasaki, Miho Akagi, Kunihiro Goto.

[IS-P-20] Class AB CMOS output circuit equipped with CMOS circuit operating by predetermined operating current,出願 US11/287469, 平成 17 年 11 月 28 日, Takeshi Yoshida, Atsushi Iwata, Mamoru Sasaki, Kunihiro Goto.

特許ﾘｽﾄ (マタウシュ, 小出グループ)

[MK-P-1]自己調整型ウィンナ･ラインアップ増幅器 ,特願 2002-159436, マタウシュハンスユルゲン、小出哲士、USA Patent Application No.10/445,033, 平成 15 年 6 月 4 日, EPC Patent Application No.03011724.6, 平成 15 年 6 月 4 日, KOR Patent Application No.2003-34611,平成 15 年 6 月 5 日, TWN Patent Application No.92114262,平成 15 年 6 月 5 日. Patents Obtained: JP3742878 Japan/25.11.2005;TW204285 Taiwan/8.10.2004; US6853251 USA/8.2.2005; K0504294 Korea/20.7.2005

[MK-P-2] H.J. Mattausch and T. Koide, “Pattern matching and pattern recognition system, associative

memory apparatus, and pattern matching pattern recognition processing method ”, JPN Patent Application No.2002-165759,平成 14 年 5 月 31 日, USA Patent Application No.10/453,636,平成 15 年 5 月 27 日, EPC Patent Application No.03012722.9,平成 15 年 5 月 27 日, KOR Patent Application No.2003-36263,平成 15 年 5 月 27 日, TWN Patent Application No.92115261,平成 15 年 5 月 27 日. Patents Obtained: TW204285 Taiwan/1.4.2005

[MK-P-3]最小マンハッタン距離検索連想メモリ装置, 特願 2004-17429, 平成 16 年 1 月 26 日, 小出哲士、マタウシュハンスユルゲン、矢野祐二, USA, Patent Application,平成 16 年 5 月 31 日, EPC Patent Application,平成 16 年 5 月 31 日, KOR Patent Application,平成 16 年 5 月 31 日, TWN Patent Application,平成 16 年 5 月 31 日

[MK-P-4]参照データ認識・学習方法及びパターン認識システム , 特願 2003-434596 ,平成 15 年 12 月 26 日, マタウシュハンスユルゲン、小出哲士、溝上政弘, USA Patent Application No.TBD. 平成 16 年 6 月 15 日, EPC Patent Application No. TBD.平成 16 年 6 月 15 日, KOR Patent Application No. TBD. 平成 16 年 6 月 15 日, TWN Patent Application No. TBD.平成 16 年 6 月 15 日

[MK-P-5]参照データ最適化学習方法とパターン認識システム, 特願 2004-53433, 平成 16 年 2 月 27 日, マタウシュハンスユルゲン、小出哲士、白川佳則

[MK-P-6] T. Hironaka, H.-J. Mattausch and T. Koide, T. Hirakawa, K. Johguchi, “ Multi-port integrated cache ”, Japanese Patent Application 2002-320037,平成 14 年 11 月 11 日, USA Patent Application TBD,平成 15 年 10 月 6 日

[MK-P-7] H. J. Mattausch, T. Koide, T. Hironaka, H. Uchida, K. Johguchi, Z. Zhu, “ Memory with Synchronous Bank Architecture ”, Japanese Patent Application 2003-167989,平成 15 年 6 月 12 日, USA Patent Application No. 10/787240,平成 16 年 2 月 27 日

[MK-P-8] H. J. Mattausch, T. Koide, T. Hironaka, T. Inoue, “ Interconnection Network and thereon based multi-port memory ”, Japanese Patent Application 2005-076253,平成 17 年 3 月 17 日

[MK-P-9] T. Koide, H. J. Mattausch, T. Kumaki, Y. Kuroda, H. Noda, K. Dosaka, K. Arimoto, K. Saito, “Encoding device”, Japanese Patent Application 2005-146211,平成 17 年 5 月 19 日

[MK-P-10] H. J. Mattausch, T. Koide, Md. A. Abedin, “Associative Memory for minimum Euclidean Distance Search”, Japanese Patent Application TBD,平成 17 年 9 月 9 日

[MK-P-11] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, “Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus”, JPN Patent Application No. 2002 152491,平成 14 年 5 月 27 日, USA Patent Application No.10/445,247,平成 15 年 5 月 26 日, EPC Patent Application No.03011840.0,平成 15 年 5 月 26 日, KOR Patent Application No.2003-33324,平成 15 年 5 月 26 日, TWN Patent Application No.92114142,平成 15 年 5 月 26 日

[MK-P-12] T. Koide, H.-J. Mattausch, T. Morimoto, and Y. Harada, “Image segmentation apparatus, image segmentation method, and image segmentation integrated circuit”, JPN Patent Application No. 2003-322163,平成 15 年 9 月 12 日, USA Patent Application No. TBD,平成 16 年 5 月 31 日, EPC Patent Application No. TBD,平成 16 年 5 月 31 日, KOR Patent Application No. TBD,平成 16 年 5 月 31 日, TWN Patent Application No. TBD,平成 16 年 5 月 31 日

[MK-P-13] T. Koide, H.-J. Mattausch, T. Morimoto, Y. Harada, O. Kiriyama, H. Adachi, “Image processing apparatus, image processing integrated circuit, image processing method, image processing program, and computer readable object extraction”, JPN Patent Application No. 2003-256184,平成 16 年 9 月 2 日

[MK-P-14] T. Koide, H.-J. Mattausch, T. Morimoto, Y. Harada, H. Adachi, “Image processing apparatus”, JPN Patent Application No. TBD,平成 17 年 9 月 9 日

特許リスト (マタウシュ, 小出グループ)

[MK-P-1] H.J. Mattausch and T. Koide, Self-adjusting winner lineup amplifier, JPN Patent Application No.2002-159436 (2002.06.06), USA Patent Application No.10/445,033 (2003.06.04), EPC Patent Application No.03011724.6 (2003.06.04), KOR Patent Application No.2003-34611 (2003.06.05), TWN Patent Application No.92114262 (2003.06.05). Patents Obtained: JP3742878 Japan/25.11.2005;TW204285 Taiwan/8.10.2004; US6853251 USA/8.2.2005; K0504294 Korea/20.7.2005

[MK-P-2] H.J. Mattausch and T. Koide, "Pattern matching and pattern recognition system, associative memory apparatus, and pattern matching pattern recognition processing method ", JPN Patent Application No.2002-165759 (2002.05.31), USA Patent Application No.10/453,636 (2003.05.27), EPC Patent Application No.03012722.9 (2003.05.27), KOR Patent Application No.2003-36263 (2003.05.27), TWN Patent Application No.92115261 (2003.05.27). Patents Obtained: TW204285

Taiwan/1.4.2005

[MK-P-3] H.J. Mattausch and T. Koide, "Associative Memory Apparatus for searching data in which Manhattan Distance is Minimum", JPN Patent Application No. 2004-017429 (2004.01.26), USA, Patent Application (2004.05.31), EPC Patent Application (2004.05.31), KOR Patent Application (2004.05.31), TWN Patent Application (2004.05.31).

[MK-P-4] H.J. Mattausch, T. Koide, M. Mizokami, "Recognition and Learning Method of Reference Data and Pattern Recognition System", Japanese Patent Application 2003-434596 (2003.12.26), USA Patent Application No. TBD. (2004. 6. 15), EPC Patent Application No. TBD. (2004. 6. 15), KOR Patent Application No. TBD. (2004.6. 15), TWN Patent Application No. TBD. (2004. 6. 15).

[MK-P-5] H.J. Mattausch, T. Koide, Y. Shirakawa, "Method for Reference-Data Optimization and Pattern-Recognition System", Japanese Patent Application 2004-053433 (2004.2.27)

[MK-P-6] T. Hironaka, H.-J. Mattausch and T. Koide, T. Hirakawa, K. Johguchi, " Multi-port integrated cache ", Japanese Patent Application 2002-320037 (2002.11.11), USA Patent Application TBD (2003.10.06)

[MK-P-7] H. J. Mattausch, T. Koide, T. Hironaka, H. Uchida, K. Johguchi, Z. Zhu, " Memory with Synchronous Bank Architecture ", Japanese Patent Application 2003-167989 (2003.6.12), USA Patent Application No. 10/787240 (2004.2.27).

[MK-P-8] H. J. Mattausch, T. Koide, T. Hironaka, T. Inoue, " Interconnection Network and thereon based multi-port memory ", Japanese Patent Application 2005-076253 (2005.3.17).

[MK-P-9] T. Koide, H. J. Mattausch, T. Kumaki, Y. Kuroda, H. Noda, K. Dosaka, K. Arimoto, K. Saito, "Encoding device", Japanese Patent Application 2005-146211 (2005.5.19).

特許リスト(三浦, 江崎グループ)

[ME-P-1] 酸化膜の角で生じるキャリヤのディープレベル捕獲を利用した不揮発性メモリ, 特願平11-136710,平成11年5月18日, 三浦道子、小野剛史、マタウシュハンスユルゲン

[ME-P-2] 微細化に適した新しい高性能ＭＯＳＦＥＴ,特願平 11-136768,平成 11 年 5 月 18 日, 三浦道子、田中 聖康、マタウシュハンスユルゲン

[ME-P-3] ポケット注入ＭＯＳＦＥＴのしきい値電圧の計算方法,特願 2001-263752,平成 13 年 8 月 31 日, 北丸大輔、三浦道子

[ME-P-4] 半導体装置の設計用シミュレーションモデル、ドレイン電流熱雑音の解析方法、シミュレーション方及びシミュレーション装置, 特願 2003-420845,平成 15 年 12 月 18 日, 三浦道子、上野弘明、細川智士

特許リスト(芝原グループ)

[Sh-P-1] MOS 型半導体装置の製造方法および MOS 型半導体装置, 特願 2004-350934,平成 16 年 12 月 3 日, 芝原 健太郎、今井清隆

[Sh-P-2] MOS 型半導体装置およびその製造方法,特願 2003-311387,平成 15 年 9 月 3 日, 芝原 健太郎

[Sh-P-3]特性値の推定方法、その推定方法の実施に使用する装置および、その推定方法の実施のための処理プログラム,特願 2003-320495,平成 15 年 9 月 12 日,村川 正宏、芝原 健太郎、小田 嘉則、樋口哲也、西謙二

国際特許

[Sh-P-4] Semiconductor Device and Manufacturing Method Threreof Cross-Referece to Related Applications, 10/926711,平成 16 年 8 月 25 日,芝原 健太郎、今井清隆

特許リスト(中島グループ)

[Na-P-1] 半導体装置およびその製造方法, 出願 2002-158788, 平成 14 年 5 月 31 日, 中島安理、出願人:独立行政法人科学技術振興機構

[Na-P-2] 半導体装置およびその製造方法, 出願 2002-268342, 平成 14 年 9 月 13 日,中島安理、出願人:株式会社半導体理工学研究センター

[Na-P-3] 屈折率膜の積層方法およびパターン化積層体, 出願 2003-081181, 平成 15 年 3 月 24 日,中島安理、横山新、吉川公麿、和気勝、出願人:広島大学長

[Na-P-4] 有機レーザーおよびその製造方法, 特願 2004-099015, 平成 16 年 3 月 30 日,中島安理、出願人:財団法人ひろしま産業振興機構

国際特許

[Na-P-5] Semiconductor device and method for manufacturing same, 出願 10/437119, 平成 15 年 5 月 14 日, 出願国:米国、出願人:株式会社半導体理工学研究センター

特許リスト(吉川グループ)

[Ki-P-1] 半導体装置,特願 2004-327568, 吉川公麿他9名、米国出願済、ヨーロッパ出願 04724181.5、韓国出願 2005-7019981、中国出願 200480010685.2

[Ki-P-2] ウルトラワイドバンド半導体集積回路,特願 2005-352935, 吉川公麿他3名

特許リスト(横山グループ)

国内特許

[Yo-P-1] 半導体ウェハ及びこれを用いた半導体装置の製造方法(内容:発光素子の集積化方法), 特願 MA901355, 平成 15 年 9 月 29 日, 荻原光彦、藤原博、横山新

[Yo-P-2] フラッシュメモリの製造方法, 特願 2004-116705, 平成 16 年 4 月 12 日, 包理、大倉健作、池田弥央、新沼仁、横山新、日本無機株式会社、国立大学法人広島大学

[Yo-P-3] 突起構造の形成方法、突起構造、および電子放出素子, 特願 2004-123379, 平成 16 年 4 月 19 日, 西林良樹、宮崎富仁、今井貴浩、横山新、田部井哲也、友電気工業株式会社、国立大学法人広島大学

[Yo-P-4] 炭素を含む材料から成る突起を形成する方法、炭素を含む材料から成る突起を有する基板生産物、および電界放出素子, 特願 2004-123383, 平成 16 年 4 月 19 日, 西林良樹、宮崎富仁、今井貴浩、横山新、田部井哲也、住友電気工業株式会社、国立大学法人広島大学

国際特許

[Yo-P-5] 半導体製造方法及装置(内容:負イオンによるウェハ酸化防止の方法), 中華民国特願 091109971, 平成 14 年 5 月 14 日, 藤井敏明、横山新

[Yo-P-6] Method of Fabricating Semiconductor Device(内容:シリコン窒化膜の原子層成長の方法), ヨーロッパ特許願 02730853.5-2203-JP0205386, 平成 14 年 5 月 31 日, 横山新、中島安理、多田吉秀、中村源志、今井正幸、米川司

特許リスト(宮崎, 東グループ)

[MH-P-1] 微粒子分散絶縁膜の製造方法、これを用いたメモリ素子、発光素子の製造方法及びメモリ素子、発光素子, 特願 2005-94203, 平成 17 年 3 月 29 日, 東清一郎

[MH-P-2] MOS 電界効果トランジスタ型量子ドット発光素子および受光素子、これらを利用した光電子集積チップ, 特願 2004-207620, 平成 16 年 7 月 14 日, 宮崎誠一、東清一郎

[MH-P-3] 光電変換膜とその応用, 特開 2001-007381, 平成 11 年 6 月 24 日, 平野善之、佐藤史郎、斉藤信雄、廣瀬全孝、宮崎誠一

2005年6月29日 (水)　中国新聞　1面

広島大の回路特性予測方法
世界標準最終候補に
欧米と決戦

三浦道子教授

広島大大学院先端物質科学研究科などが共同開発した高性能集積回路の特性予測の方法が、世界標準モデルの最終候補に選ばれ今秋、欧米グループとの一騎打ちに臨む。支援強化のため広島大は「HiSIM(ハイジム)研究センター」の設置を、二十八日に広島市で開いた経営協議会と役員会で決めた。

回路特性の予測方法は「トランジスタモデル」と呼ばれる計算式の集合体。億単位のトランジスタを組み込む回路設計の際に、電圧に対するトランジスタの応答をあらかじめ解析するソフト「回路シミュレーター」の心臓部にあたる。

世界標準に選ばれれば「回路シミュレーター」を通じ、あらゆるトランジスタ利用製品の開発の根幹を、広島大方式が担うことになる。

一九九六年に米国カリフォルニア大のモデルが初めて世界標準に選ばれたが近年、トランジスタの高度化で精度が落ちるなどの問題が出てきた。同研究科は、日本の半導体企業十一社でつくる半導体理工学研究センターと二〇〇一年に高精度モデルを共同開発。正確な方法を確立した。

〇三年に世界の主な半導体関連企業二十七社でつくる協議会が〇三年から次世代モデル選びを開始。一次選考を通過した四つの中から広島大などのモデルと、米国ペンシルベニア州立大などのモデルが今春、同じ票数で二次をパスした。ハイジム研究センターは七月一日に設置し、秋に向けてモデルの検証や改良などに取り組む。同研究科の三浦道子教授は「モデルなしにトランジスタを使う製品は作れない。世界標準となれるよう改良を続けたい」と話している。

2005年12月6日(火)
読売新聞

LSI設計計算式開発

広大大学院グループ 「世界標準」選考会で評価

広島大大学院先端物質科学研究科の三浦道子教授（極微細デバイス工学）らの研究グループが、コンピューターなどの頭脳になる大規模集積回路（LSI）の設計に必要な計算式「HiSIM（ハイジム）」を開発、世界の主要な半導体企業でつくる協議会が選考する次世代世界標準モデルの最終選考に残った。選考では小差で標準モデルには選ばれなかったが、同大は「予想以上の評価を得られた」と手応えを感じている。

計算式は「トランジスターモデル」とも呼ばれ、1998年から、国内の大手半導体メーカー11社でつくる半導体理工学研究センター（STARC、横浜市）と共同開発した。

三浦教授によると、数億個のトランジスターなどで構成するLSIを設計する際、機能しやすいトランジスターや配線などの並び方を効率よく計算。96年に選ばれた現在の世界標準モデルでは4日間かかるが、半日に短縮されるという。

米国企業を中心にした32社で組織する同協議会が2003年秋から次世代モデルの選考を開始。ヨーロッパの半導体大手メーカー「フィリップス」と米ペンシルベニア州立大が共同開発したモデルとの争いとなり、3票差で惜しくも採用されなかった。

今回は採用されなかったが、内外の個別企業からの問い合わせは多数あり、さらに改良して実用化を狙う。広島大も今年9月、「HiSIM研究センター」を設置して研究への支援を強化。三浦教授は「結果は残念だが、性能を高めてさらに次の世代の世界標準を目指す」と話している。

2005年12月6日 (火) 読売新聞

広島大のハイジム

世界標準モデルならず

ナノテク時代に欠かせない半導体回路の特性予測ソフトとして、次世代世界標準の最終候補に残っていた広島大大学院先端物質科学研究科などの「HiSIM（ハイジム）」が、欧米グループとの一騎打ちにわずかの差で敗れた。

同研究科に五日までに入った連絡によると、世界の主な半導体関連企業でつくる協議会が十一月末に最終投票し、十七対十四だった。投票したのはアジア六社、欧米二十五社と地域差があった中、最後まで高評価を得ていたという。同大ハイジム研究センター長で同研究科の三浦道子教授は「世界トップなのは明らか。今後も検証、開発を重ねたい」と話している。

ハイジムは、億単位のトランジスタを組み込む回路設計時の特性予測に必要な「トランジスタモデル」と呼ばれる計算式の集合体。同研究科と日本の半導体企業十一社でつくる半導体理工学研究センターが二〇〇一年に共同開発。〇三年から始まった世界標準選びで、米国ペンシルベニア州立大などの開発モデルとともに一、二次選考を通過していた。（岡田浩平）

COE授業推進者

名前	所属	E-mail
岩田 穆	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 教授	iwa@dsl。hiroshima-u。ac。jp
角南 英夫	広島大学ナノデバイス･システム研究センター 教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	sunami@sxsys。hiroshima-u。ac。jp
吉川 公麿	広島大学ナノデバイス･システム研究センター 教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	kikkawa@sxsys。hiroshima-u。ac。jp
Mattausch Hans Yurgen	広島大学ナノデバイス･システム研究センター 教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	hjm@sxsys。hiroshima-u。ac。jp
横山 新	広島大学ナノデバイス･システム研究センター 教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	yokoyama@sxsys。hiroshima-u。ac。jp
芝原 健太郎	広島大学ナノデバイス･システム研究センター 助教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	shiba@sxsys。hiroshima-u。ac。jp
中島 安理	広島大学ナノデバイス･システム研究センター 助教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	nakajima@sxsys。hiroshima-u。ac。jp
小出 哲士	広島大学ナノデバイス･システム研究センター 助教授 広島大学大学院 先端物質科学研究科 半導体集積科学専攻 兼担	koide@sxsys。hiroshima-u。ac。jp
三浦 道子	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 教授	mmm@hiroshima-u。ac。jp
宮崎 誠一	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 教授	miyazaki@sxsys。hiroshima-u。ac。jp
佐々木 守	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 助教授	sasaki@dsl。hiroshima-u。ac。jp
東 誠一郎	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 助教授	sehiga@sxsys。hiroshima-u。ac。jp
江崎 達也	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 助教授	ezaki@hiroshima-u。ac。jp
村上 秀樹	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 助手	hideki@hiroshima-u。ac。jp
吉田 毅	広島大学大学院 先端物質科学研究科 半導体集積科学専攻 助手	tyoshida@dsl。hiroshima-u。ac。jp

COE研究員(ポスドク)

名前	所属	E-mail
Saha Pran Kanai	広島大学大学院　先端物質科学研究科 半導体集積科学専攻ナノデバイス工学研究室 (ナノデバイス・システム研究センター)	sahapk@sxsys。hiroshima-u。ac。jp
奥山　清	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　ナノ集積工学 (ナノデバイス・システム研究センター)	okuyama@sxsys。hiroshima-u。ac。jp
佐々木　信雄	広島大学大学院　先端物質科学研究科 半導体集積科学専攻ナノデバイス工学研究室 (ナノデバイス・システム研究センター)	nsasaki@sxsys。hiroshima-u。ac。jp
田主　裕一朗	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　ナノプロセス工学研究室 (ナノデバイス・システム研究センター)	tanushi@sxsys。hiroshima-u。ac。jp
Ali Ahmadi	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　知能集積回路工学研究室 (ナノデバイス・システム研究センター)	ahmadi@sxsys。hiroshima-u。ac。jp
細井　卓治	広島大学大学院　先端物質科学研究科 半導体集積科学専攻ナノデバイス工学研究室 (ナノデバイス・システム研究センター)	hosoi@sxsys。hiroshima-u。ac。jp
安藤　博士	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　機能集積システム工学 研究室	ando@dsl。sxsys。hiroshima-u。ac。jp
亀田　成司	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　機能集積システム工学 研究室	kameda@dsl。hiroshima-u。ac。jp
磯部　義興	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　極微細デバイス工学研究室	yoshioki@hiroshima-u。ac。jp

博士課程学生 (Research Assistant)

名前	所属	E-mail
汐崎　充(D6)	広島大学大学院　先端物質科学研究科 量子物質 科学専攻　機能集積システム 工学研究室	shiozaki@dsl。hiroshima-u。ac。jp
大岡　昌洋(D3)	広島大学大学院　先端物質科学研究科 量子物質科学専攻ナノデバイス 集積研究室 (ナノデバイス・システム研究センター)	ooka@sxsys。hiroshima-u。ac。jp
牧原　克典(D3)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　量子半導体工学研究室	makihara@hiroshima-u。ac。jp
小野　将寛(D3)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　機能集積システム 工学研究室	masa@dsl。hiroshima-u。ac。jp
鈴木　昌人(D2)	広島大学大学院　先端物質科学研究科 半導体集積科学専攻　ナノプロセス工学研究室 (ナノデバイス・システム研究センター)	suzuki@sxsys。hiroshima-u。ac。jp
裴　艶麗 (D2)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　量子半導体工学研究室	peiyanli@hiroshima-u。ac。jp
中川　博(D2)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　量子半導体工学研究室	n164@hiroshima-u。ac。jp
佐々木寛弥(D2)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　機能集積システム 工学研究室	kanya@dsl。hiroshima-u。ac。jp
大田　晃生(D1)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　量子半導体工学研究室	ohta@hiroshima-u。ac。jp
向井　徹(D1)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　機能集積システム 工学研究室	toru@dsl。hiroshima-u。ac。jp
升井　義博(D1)	広島大学大学院　先端物質科学研究科 量子物質科学専攻　機能集積システム 工学研究室	masui@dsl。hiroshima-u。ac。jp