

# Proceedings of Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing

January 30, 2004

Hiroshima University Graduate School of Advanced Sciences of Matter

## Preface

The 21st century COE program "Nanoelectronics for Terra-Bit Information Processing" aims at the fusion of silicon-based nanodevices, circuits and integrated circuit-architectures. Fusion of the basic research fields is considered necessary for another goal of the COE, namely the construction of integrated systems with high-level recognition and learning functionality. Bringing up independent researchers which are capable of advanced, visionary and well reflected research in a broad range of fields is regarded as very important to accomplish our goals.

Our main specific research tasks can be summarized as:

- \* Unification of silicon-based system, circuit, device-modeling and device fabrication research
- \* Solution of the persistent 3-dimensional-integration problems by a wireless integration methodology
- \* Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures

Within the scope of the COE program, we hold workshops in the framework of the COE program to demonstrate our progress, to interact with worldwide leading groups for exchanging information as well as to initiate possible collaboration. The first workshop was held on March 17th in 2003 and presented an overview of the research fields in the focus of the COE. Lectures by outstanding leaders over the world were also given for verifying our concepts and enabling future interactions.

The 2nd workshop is held at Hiroshima University, the Graduate School of Advanced Sciences of Matter, Lecture Hall 401N. It focuses on the modeling and simulation tasks of the COE, aiming at providing opportunity to get an overview of present activities undertaken in the world. Requirement for simulations is increasing due to the complexity of device characteristics approaching technological limitations. More efforts are also requested to realize accurate SoC simulations. At the workshop possibilities to realize tight collaborations among different fields to accelerate the achievements are also discussed.

We would like to welcome you to the 2nd Hiroshima International Workshop on Nanoelectronics for Terra-Bit Information Processing. All of the COE members hope that this workshop will provide an opportunity for further interactions and discussions with you.

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PLEN.	ARY SESSION 9:00 – 15:40
	Lecture Hall 401N, the Graduate School of Advanced Sciences of Matter
9:00	<b>Opening Address</b> Taizo Muta, President of Hiroshima University
9:05	Overview & Keynote Address2- Recent Progress of the COE -Atsushi Iwata, Director of the COE, Hiroshima University
9:15	[Invited] Low Power SoC Technology Development at STARC
10:15	<b>[Invited] Quantum Mechanical Carrier Transport and Nano-scale MOS Modeling</b> 18 Zhiping Yu, Tsinghua University, China
11:15	Wireless Interconnection on Si LSI using Integrated Antenna32Takamaro Kikkawa, Hiroshima University
11:30	[Invited] Physics-Based Modeling of Electromagnetic Parasitic Effects in Interconnects
	<u>12:30 – 14:00 Lunch Break</u>
14:00	[Invited] Modeling CMOS Non-Quasi-Static Effects in a Quasi-Static Simulation Engine
15:00	<b>MOSFET Modeling for RF-CMOS Design</b>
	<u>15:40 – 16:00 Coffee Break</u>

#### **POSTER SESSION by COE members** 16:00 – 18:00

The 4-th Floor Lounge, the Graduate School of Advanced Sciences of Matter

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#### **CLOSING REMARKS**

18:00 Mitiko Miura-Mattausch, Hiroshima University