Low Power SoC Technology Development at STARC

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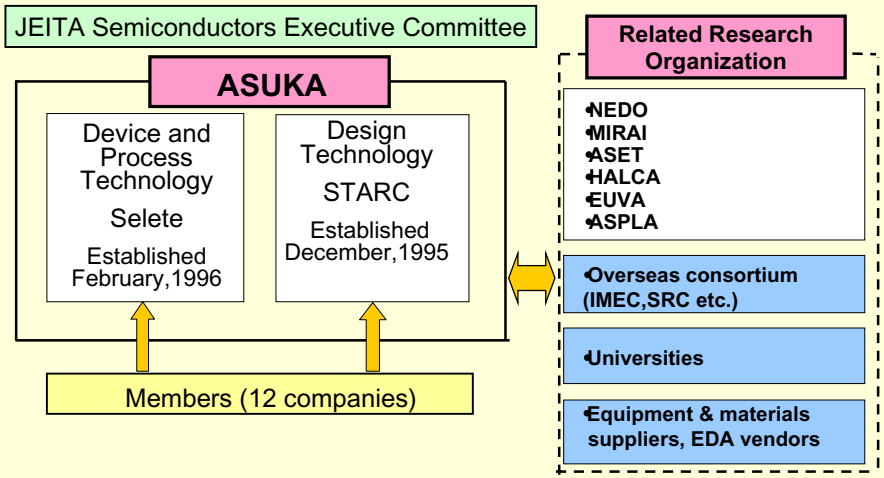
Outline

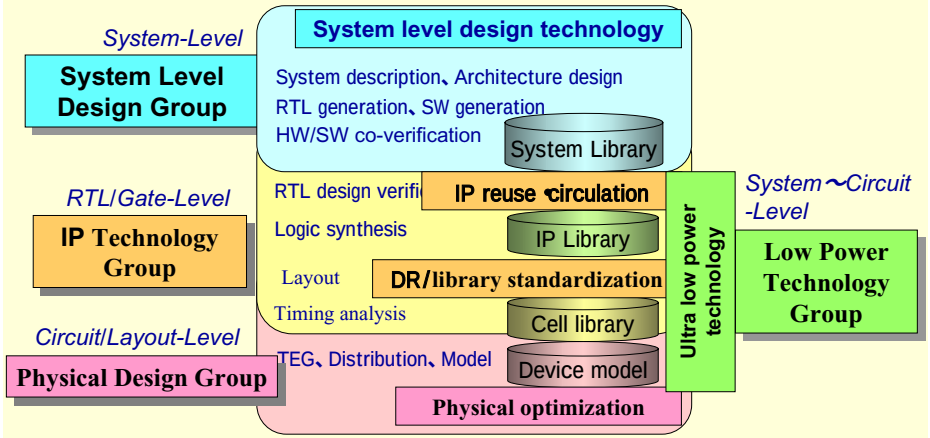
- Outline of Project ASUKA
- Low Power Technology Development at STARC
- Developed Low Power Technology
  - Self-Adjusted Forward Body Bias
  - Body Gating
  - High speed ADC
- Device Model Issues
- Summary

Project ASUKA Development Scheme



Design Technology Development in STARC

- SoC Design Flow -



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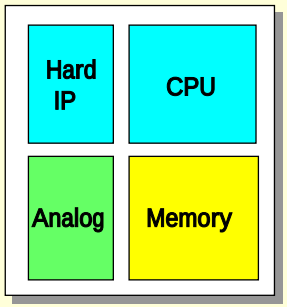
Low Power SoC

- Low power CPU
- Low power hardware macro
- Low voltage ADC
- Low power and high density memory



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Target
- Low voltage operation of each IP block -

- Digital
  - 0.5V digital circuit
  - Power Management
- Analog
  - 1V operation ADC
  - Noise suppression scheme
- Memory
  - 0.5V operation on-chip RAM

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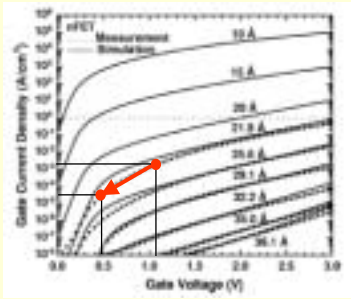
Gate Leak Reduction by Super Low Voltage



Ref.S.H.Lo et al.,

Gate leakage current is reduced by 2 orders of mag. when suply voltage is decreased from 1.2V to 0.5V

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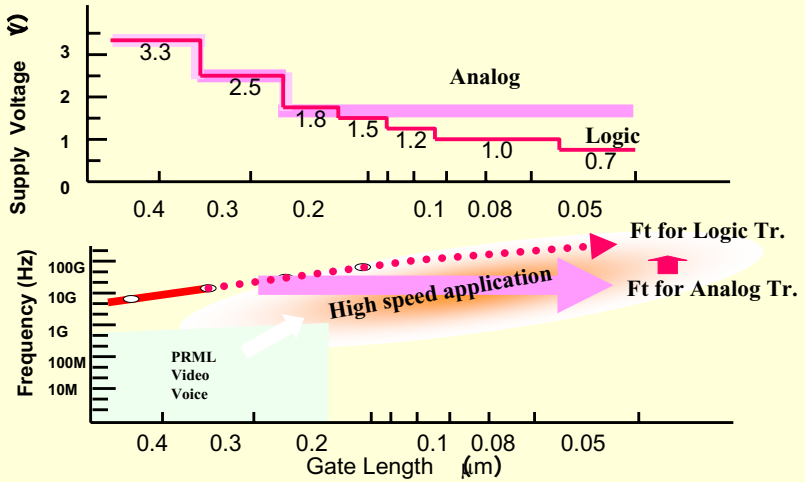
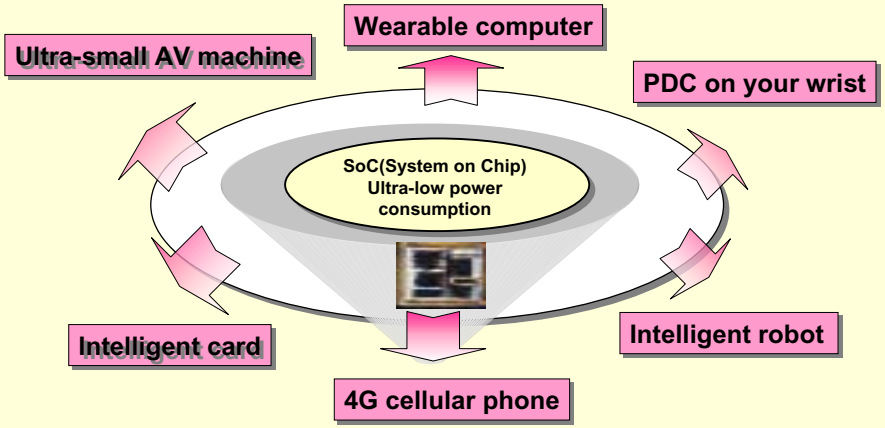
High Speed Analog Circuit using Low Vdd Logic Transistors



New Applications of Low Power SoCs



- Contribution to realize these applications by decreasing the power of SoC to 1/200

Low Power Project Time Line

Fiscal Year	2001	2002	2003	2004	2005
Master Plan	Building Block Development (130nm)		SoC Development (90nm)		T.T.

Presentation at International Conferences

- T. Yamashita et al., “A V-driver Circuit for Lowering Power of sub-0.1 μm Bus,” 2002 AP-ASIC, Taipei
- K. Ishibashi et al., “A 9μW 50MHz 32b Adder Using a Self-Adjusted Forward Body Bias in SoCs,” 2003 ISSCC, San Francisco
- H. Okada et al., “Offset Calibrating Comparator Array for 1.2-V, 6-bit, 4-Gsample/s Flash ADCs using 0.13-μm generic CMOS technology,” 2003 Ess. Circ., Lisbon
- K.Ishibashi et al., "Low Power SoC Project in STARC,” 2003 VLSI-TSA, Taipei
- Y. Arima et al., “A Cosmic-Ray Immune Latch Circuit for 90-nm Technology and Beyond,” 2004 ISSCC, San Francisco
- T. Tsukada et al., "An On-Chip Active Decoupling Circuit to Suppress Crosstalk in Deep Sub-Micron CMOS Mixed-Signal SOCs,” 2004 ISSCC, San Francisco

Strategy to Obtain Low Power Digital Circuit

Combination of

High Performance Device and Super Low Voltage Operation

○ Ultra low AC power with relatively high performance

○ Gate leakage and DIBL is reduced

● Variation due to PVT
→ Self-adjusted Forward body bias

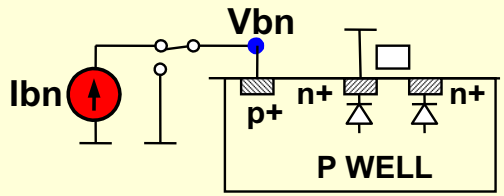
● Large subthreshold leakage current
→ Power management by body gating

SAFBB Technique
(Self-Adjusted Forward Body Bias)

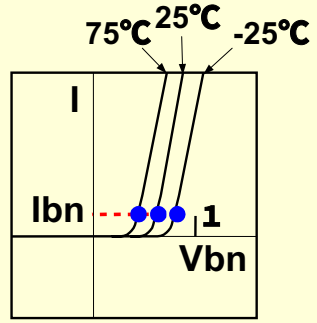
- 9 μW 32bit adder @ 0.3V
- Simple body bias circuit

Self - Adjusted Forward Body Bias Concept

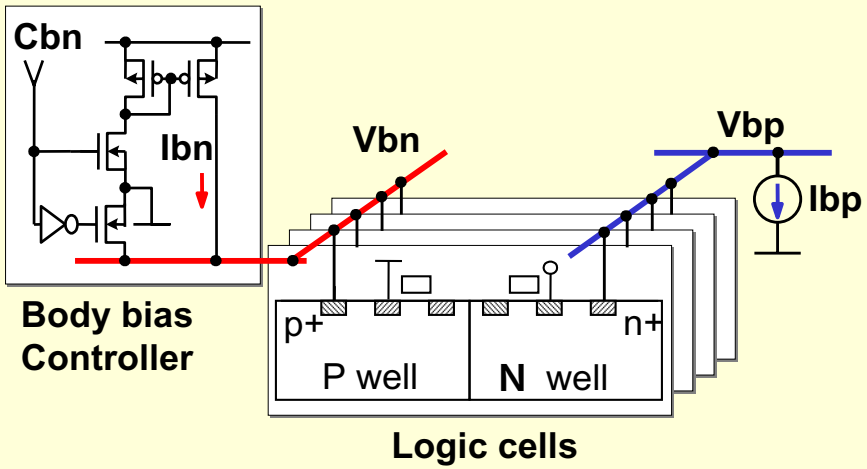
- Forward body bias as Vbe



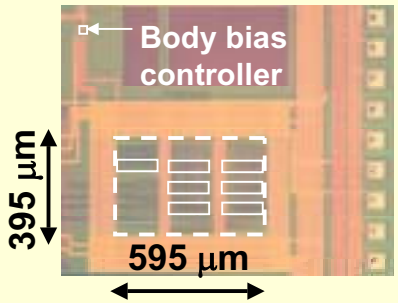
- Self-adjusted depending on temperature



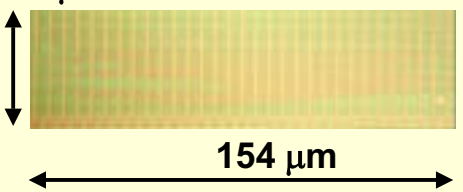
Practical Implementation of SAFBB



Test Chip Structure



- 0.13 μm CMOS
  - P-sub, twin well
  - VT: 0.16V/0.25V



- 32 - bit adder
  - Binary CLA
  - 2.3-k transistors
  - Static CMOS circuits

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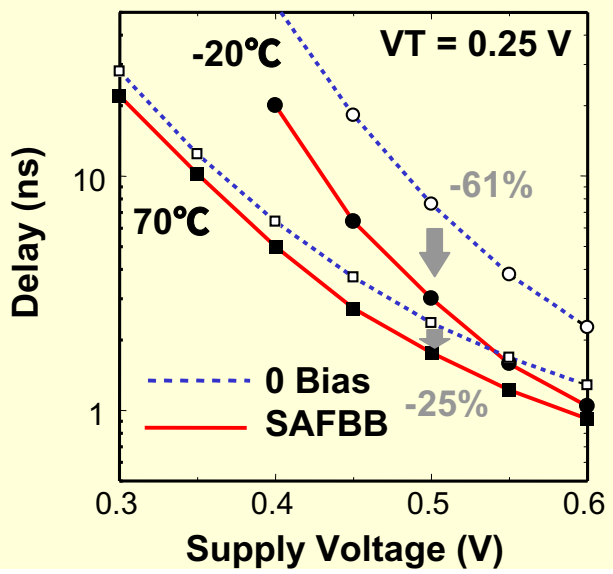
Measured 32-bit Adder Delay



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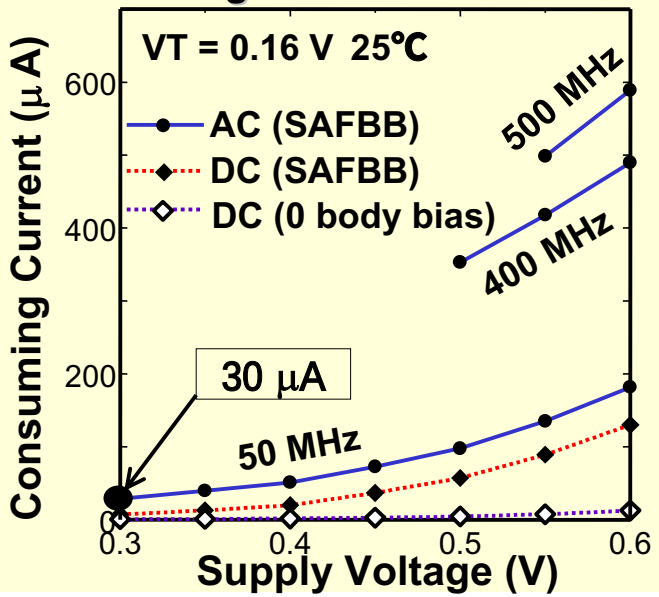
Consuming Current of 32-bit Adder



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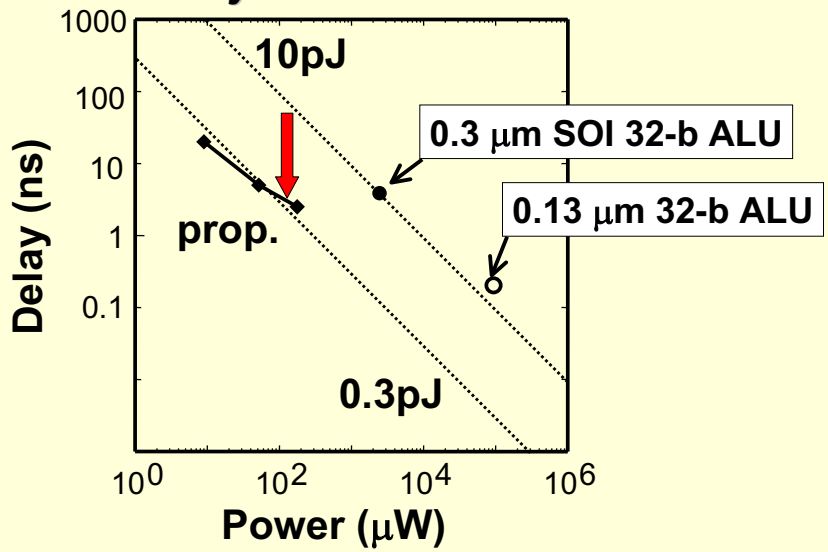
Power Delay Product of 32 - bit Adder



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Body Gating

- 3.6 mW MPEG2 CODEC @0.5V
- Leakage Current Control

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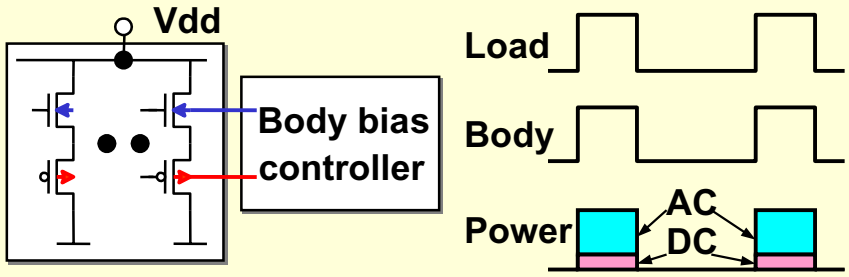
Body Gating Technique

- Leakage reduction by controlling body bias



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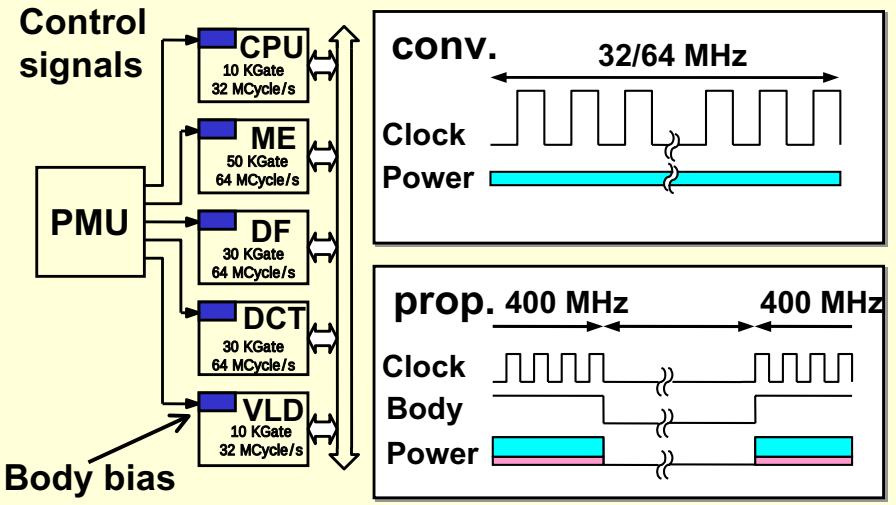
SoC with Body Gating



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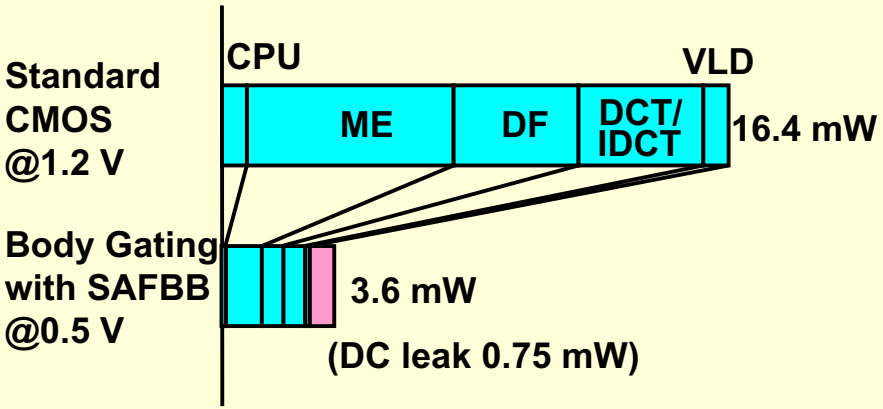
Power Estimation for MPEG2 CODEC



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High Speed ADC

- 2Gsample/s 4bit @ 0.9V
- Offset Voltage Reduction

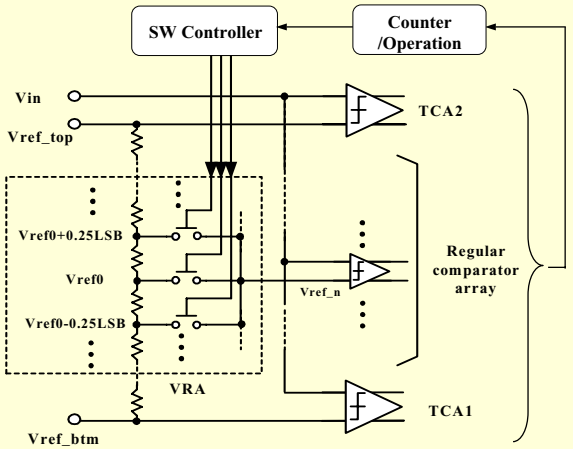
Issues of Low-Voltage ADC

(1) High impedance of switching transistor
→ Avoid switching transistor

(2) Large Vth mismatch of paired transistors
→ Offset voltage cancel circuit

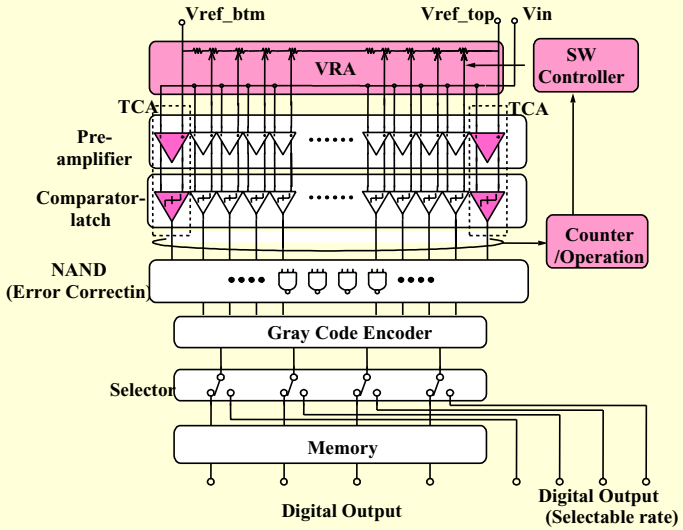
(3) Limited number of transistors in cascade configuration
→ Simple current source circuit

Comparator Array Architecture of ADC - Offset Canceling Circuit -

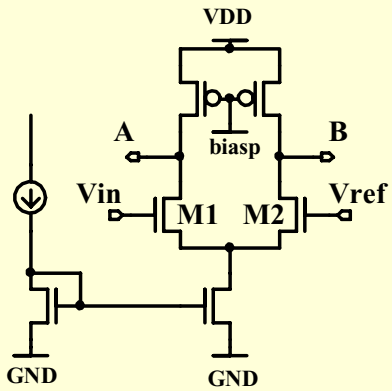


Resolution : +/-0.25 LSB
Adjustable range: +/-1.75 LSB

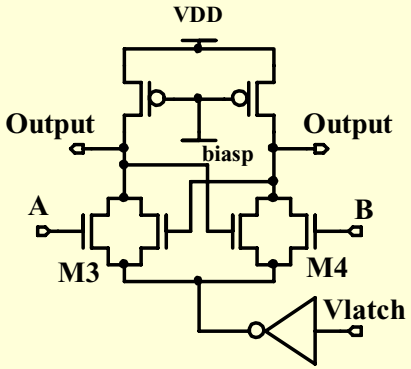
Block Diagram of 4-bit Flash ADC



Circuits of Amplifiers



(a) Low-voltage pre-amplifier



(b) Low-voltage comparator-latch

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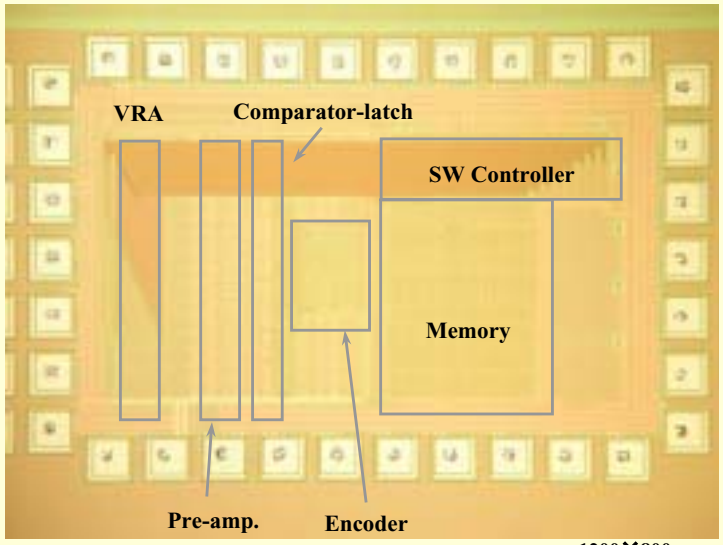
Chip Micrograph of ADC.



1200×800um

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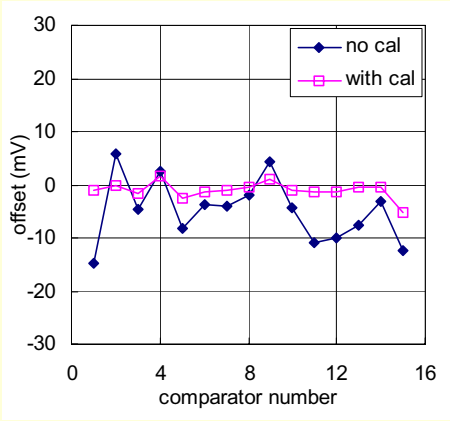
Effect of Offset Calibration



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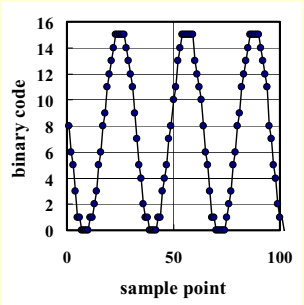
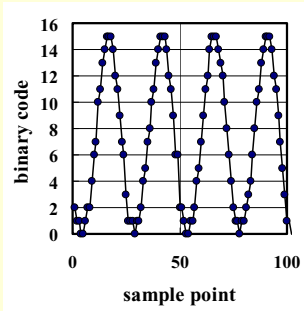
Regenerated Waveforms





(a) 2.015 GSample/s and 2.0-MHz input frequency at Vdd=0.9 V.

(b) 4.0 GSample/s and 5.0-MHz input frequency at Vdd=1.2 V.

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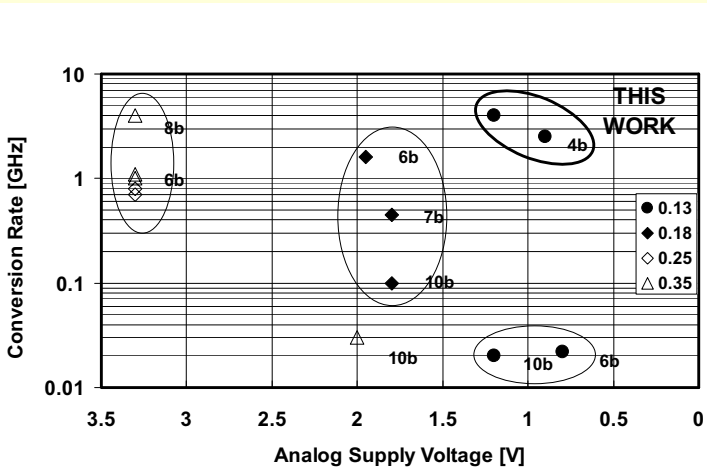
Position of ADC



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Device Model Issues

- Digital Circuit
  - Leak Model
  - Substrate bias effect
    - Forward body bias
    - Diode model for forward body bias
  - Expansion of parameter set
  - Best and worst model
- ADC
  - Accuracy in triode and saturation, and their boundary region
  - High speed simulation(After LPE)

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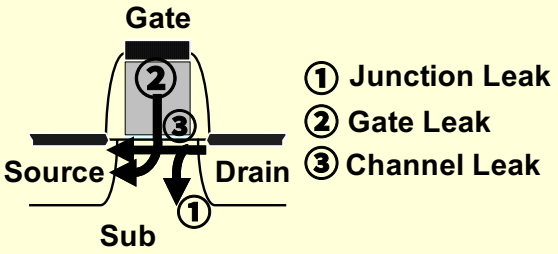
Leak Model

- Channel Leakage
- GIDL (Gate Induce Drain Leakage)
- Gate Tunneling Current



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Substrate Bias Effect

- Necessary model for SAFBB technique

- Accurate transistor model at forward body bias condition
- Accurate source and drain diode model including forward direction

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Argument

- Which approach is better for high speed and low power operation

- Low substrate bias constant MOSFET without body bias technique
- High substrate bias constant MOSFET with body bias technique

- Scalable MOS parameter helps to solve the argument

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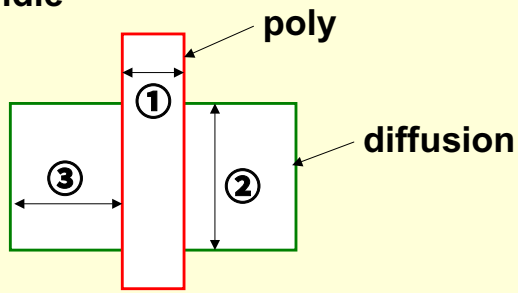
Expansion of parameter set

- Each device model is assigned

  depending on L and W(130nm),

  and gate - diffusion edge distance (90nm)

- hard to handle



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What are the best and the worst model

- The best and the worst model are depending on circuits

  (Random Logic, Clock Distribution, Memory, and Analog)

- How to handle the distribution of characteristics of MOS transistors

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Accuracy of the model

- Accuracy of model in triode, saturation and their boundary.

- Normally accuracy in saturation region has a priority for logic design.

  Analog designers must first design circuits using inaccurate model for triode region.

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High Speed Circuit Simulation

- ADC was designed first by Hspice simulation
- Layout - LPE - fast circuit simulation
- High speed simulation is necessary
- Usage of Hsim (Nassda)

  two days simulation for 116K Tr. 4bit ADC

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Conclusions

- **Low Power SoC in Project ASUKA**

  - Low voltage Logic, Analog, and Memory

- **Low Power Techniques**

  - SA-FBB Technique
  - Body gating
  - High-speed ADC

- **Various Device Model Issues at design**