MOSFET Modeling for RF-CMOS Design

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1 Introduction

Though the RF MOSFET circuit is becoming realistic, the RF-circuit simulation is still a challenge due to many reasons. One important reason is the lack of model accuracy required for the simulation [1]. Demand for accurate prediction of non-linear device characteristics is also tough due to deficiency of sufficient knowledge including measurements. Another serious reason is that appropriate tools for RF designs are still lagging behind the demand [2]. A lot of progress has been made to catch up the requirements in both the modeling aspect and providing simulation tools. Here our discussion focuses on the modeling aspect.

2 Model Requirements

Accurate circuit simulation is becoming more serious due to two ongoing fabrication-technology developments, namely, the down scaling of MOSFETs into the sub-100nm regime and system integration with many functions on a single chip, which are prerequisite for RF circuits. To assist in the development, the most important issue is to guarantee sufficient simulation accuracy and applicability for any advanced technology. Under high-frequency operation, non-linear phenomena such as distortion as well as carreir response delay become serious for reliable circuit performance prediction. Here all such device phenomena are demonstrated to be determined by carrier dynamics, which are in principle observed in the *I*-*V* characteristics [3]. Thus, the importance of the accurate parameter extraction will be emphasized for accurate circuit simulation.

A better circuit model has less model parameters, without compromising accuracy. The model parameters should be connected to device parameters and should be measurable independently. To realize this concept model development trends to follow the device physics, namely to describe device performances with the potential distribution along the channel instead of applied voltages conventionally done. The self-consistent charge-based model with the surface-potential description will be demonstrated to offer the basis for successful performing the foreseeable challenges. Modeling approach of HiSIM (Hiroshima-university STARC IGFET Model), the MOSFET model has been developed according to this concept for the first time [4].

3 Modeled Phenomena

Phenomena to be modeled and their modeling approaches are described in three groups:

(A) Modeling of Basic MOSFET Characteristics
(B) Large-Signal Analysis
(C) Samll-Signal Analysis

The group (A) includes normal DC and AC characteristics of MOSFET, requires intensive model parameter extraction. The group (B) focuses on carrier dynamics under high-frequency operation in the time domain, which is often transormed to the frequency domain with the harmonic balance analysis. The group (C) is the special case of the group (B). The modeling is done with an equivalent circuit model, which requires extraction of the elements included in the circuit.

3.1 Modeling of Basic MOSFET Characteristics

Requirements for the modeling is that all measured *I*-*V* characteristics have to be well reproduced. Their derivatives are also sensitive for RF applications [5]. Calculated I_{ds} and their derivatives (lines) are shown in Fig. 1 in comparison with measurements (dotted lines). If the model is consistent and all model parameters are accurately extracted from measurements, other measured quantities should be reproduced without any additional model parameters. The harmonic distortion is one of such an object. Fig. 2 demonstrates the proof [6].

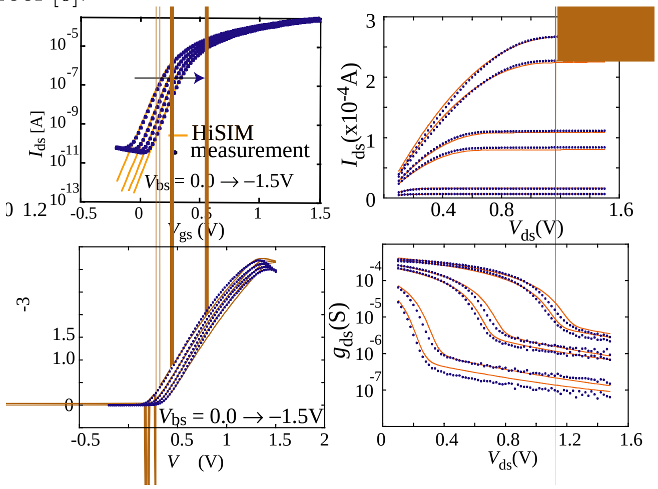

Fig. 1: Comparison of calculated *I*-*V* characteristics and their drivatives with measurements. The gate length is fixed to 10μm.

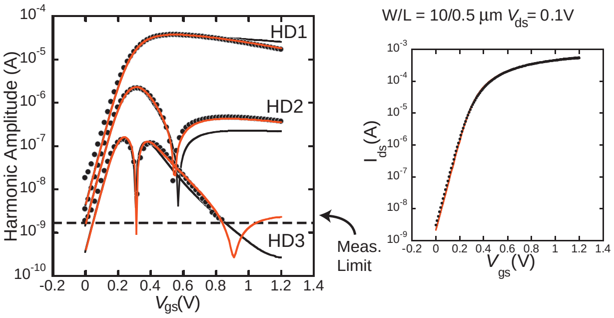

Fig. 2: Comparison of calculated harmonic distortion with measurements (dotted). The thick solid lines are results with a parameter set extracted from measured *I*-*V* characteristics and the grey lines are with tuned mobility parameter. The difference of the parameter values cannot be seen in the *I*-*V* characteristics.

In RF systems, noise is a major issue obstructing circuit performance [2]. There are two important noise mechanisms to be considered for advanced MOSFETs; the $1/f$ noise and the thermal noise. Fig. 3 compares calculated $1/f$ noise characteristics including the trap density as a fitting parameter with measurements at $f = 100$Hz [7].

The thermal noise is determined by the channel conductance. Fig. 4 shows calculation results with HiSIM in comparison with measurements [8].

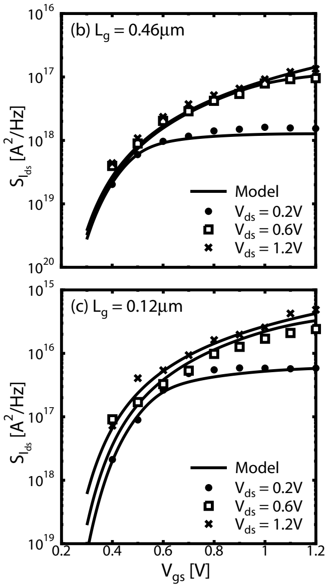

Fig. 3: Calculated $1/f$ noise characteristics in comparison with measurements. Only the trap density is the model parameter, valid for all gate lengths [7].

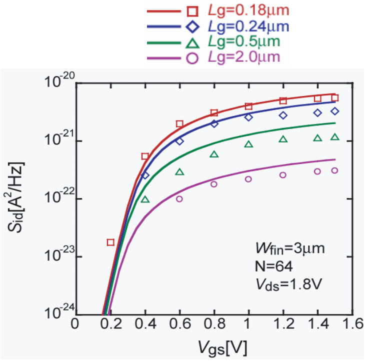

Fig. 4: Calculated thermal noise in comparison with measurements. For the calculation model parameters extracted only from measured I-V characteristics are used [8].

3.2 Large-Signal Analysis

Circuit simulators solve transient characterisitcs of cirucits in the form written as

$$I_a(t) = I_a(0) - \frac{dQ_a}{dt} \tag{1}$$

derived under the quasi-static approximation, ignoring the carrier transit delay along the channel. $I_a(0)$ denotes the spontaneous current response to the applied voltage on node a without delay. The main effort is given to modify Q_a in Eq. (1) including the carrier deficit caused by the carrier transit delay. A model suitable for circuit simulation has been developed as demonstrated in Fig. 5 [9].

3.3 Small-Signal Analysis

The small-signal analysis investigates the high frequency characteristics considering the case where input simusoudal voltage variations are sufficiently small so that the small output current variations can be expressed by a linear relation as [5]

$$\Delta I_{\rm ds} = g_{\rm m}\Delta V_{\rm gs} + g_{\rm mb}\Delta V_{\rm bs} + g_{\rm ds}\Delta V_{\rm ds} \tag{2}$$

where conductances gs' are derivatives of I_{ds} with respect to corresponding node voltages. The characterization is done with y parameters, the admittance matrix representing the carrier response. Calculation reuslts with the improved equivalent circuit (NQS) are demonstrated in Fig. 6 [10] in comparison with the conventional equivalent circuit (QS).

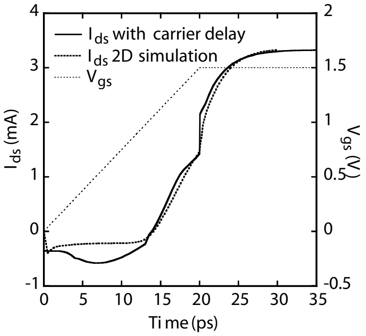

Fig. 5: Comparison of a calculated transient $I_{\rm ds}$ behavior to a 2D simulation result under high switching operation [9].

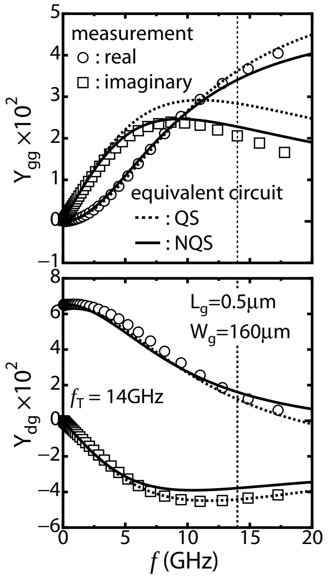

Fig. 6: Measured (open symbols) and calculated y parameters with the non-quasi-static model (solid curves) and the quasi-static model (dashed curves) for the gate length of 0.5μm. The vertical dotted lines denote the cut-off frequency of the device studied.

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