A Multi-chip Vision System with a PWM-based Line Parallel Interconnection

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1 Introduction

The vertebrate visual system processes huge visual information in real-time by massively parallel neural networks arranged hierarchically and adapts to a rapidly changing visual environment by an adaptive mechanism. Inspired by the unique architecture and algorithm of the vertebrate visual system, the neuromorphic vision chips, novel analog Very Large Scale Integrated (VLSI) circuits, have been fabricated ([4, 6] for outlines). These neuromorphic chips, however, encounter a serious problem, namely, the trade-off between the resolution and the computational complexity of the chip. To solve the problem, multi-chip systems have been fabricated previously[1, 5]. In these multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. On the other hand, a 3-Dimensional Custom-Stack System (3DCSS) has been proposed by our 21st Century COE program. In the 3DCSS, multiple chips fabricated by various technologies and arranged hierarchically are connected by two types of wireless connections, which are a local connection and a global connection. Due to the wireless connections, the 3DCSS overcomes a wiring complexity that is the demerit of the multi-chip system generally. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system. In the present study, a visual processing system using the 3DCSS configuration is proposed. And as a preliminary step toward fabrication of the visual processing system, we have fabricated a prototype visual processing chip with a PWM-based line parallel interconnection.

2 Visual processing system using the 3DCSS configuration

We propose a visual processing system using the 3DCSS configuration. Fig.1(A) shows a design of the visual processing system. The system consists of an image sensing chip, a visual processing chip and an adaptive control chip. Fig.1(B) illustrates the block diagram of the image sensing chip. In the image sensing chip, an image obtained by photo sensors is processed by massively parallel arrays of processing circuits. The outputs of the image sensing chip are transferred to the visual processing chip using a local connection. The local connection are formed by a line parallel inductive coupling on spiral inductor pairs between a transmitter of the image sensing chip and a receiver of the visual processing chip[8]. Due to the line parallel method, the 2-dimensional huge visual information is transmitted very quickly. Fig.1(C) illustrates the block diagram of the visual processing chip. The input to a pixel of the visual processing chip from a corresponding pixel of the image sensing chip is memorized in an analog memory. The memorized data is processed by massively parallel arrays of processing circuits, too. The outputs of the visual processing chip are transferred to another visual processing chip using a local connection. As shown in Fig.1(A), on a surface of a system base, A power supply line, a control signal bus and output signal bus are arranged. A direct contact between these processing chips and the system base makes a power supply, an input of basic control signals and a readout output by wired connection possible. Fig.1(D) il-

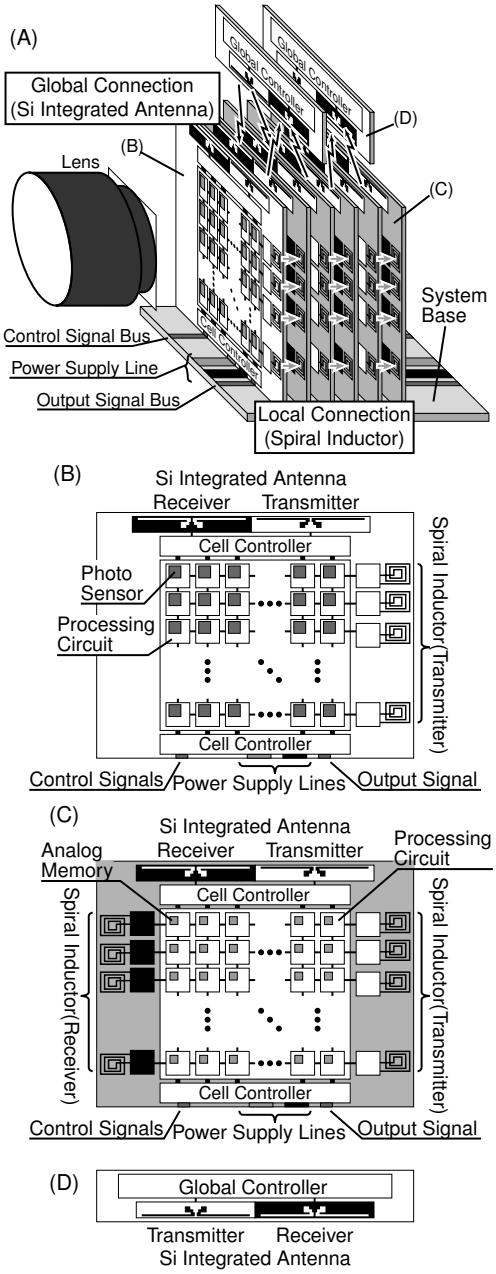

Figure 1: Visual processing system using the 3DCSS configuration. (A)System design, (B)block diagram of the image sensing chip, (C)the visual processing chip and (D)the adaptive control chip.

lustrates the block diagram of the adaptive control chip. The adaptive control chip receives processing data from the image sensing chip and the visual processing chip, and controls these chips using a global connection. The global connection between the adaptive control chip and the processing chip are realized by a microwave communication utilizing integrated dipole antennas, which are integrated on these chips for a transmitter and receiver circuits[7]. The adaptive control chip can control multiple chips at once since the integrated dipole antenna is able to transmit a data whose bandwidth is 10G - 20GHz at a distance of a few cm in air. If these chips are arranged as shown in Fig.1(A), the image sensing chip and different varieties of the visual processing chips realize hierarchical and massively parallel image processing, and the adaptive control chips adapt to the visual environment and control the whole system immediately as found in the vertebrate visual system.

3 Prototype visual processing chip with a PWM-based line parallel interconnection

A prototype visual processing chip has been fabricated as a preliminary step toward fabrication of the visual processing system using the 3DCSS configuration. In our first attempt, the line parallel spiral inductor module was separated from the prototype visual processing chip. Namely, combining the prototype visual processing chip and independently-developed spiral inductor module chip makes possible a experiment of data transfer using the local connection. Fig.2(A) shows a block diagram of the prototype chip. The prototype chip consists of a cell array and a line parallel input and output units. In the cell array, processing circuits included an analog memory are arranged in a 44 x 40 matrix. In the line parallel input and output units, an input and output units are arranged every 4 column of the cell array in a line (1 x 10) respectively. The memorized data in the analog memory is smoothed by the resistive network since the processing circuit is similar in structure to the pixel circuit of the multi-chip silicon retina[3]. In the prototype chip, a pulse width modulation (PWM)-based data transfer method was adopted in order to fit a transmitter/receiver using the spiral inductor. In the transmitter/receiver, because a data format must be digital due to a constraint of the spiral inductor, an analog processed data must be converted into a digital data. In the PWM method, an analog voltage data is converted into a width of digital pulse in time domain[2]. The PWM method is suitable for the 3DCSS because the PWM and PWD (pulse width demodulation) circuits are realized simpler structure than a standard A/D and D/A converters. Fig.2(B) and (C) show a circuit design of the input unit and the output unit respectively. The input unit is the PWD circuit consisted of a sample/hold circuit (Nbuf)[3]. In the input unit, if the sample/hold circuit is input into a ramp voltage and held by the PWM input, the analog voltage is proportional to the pulse width of the input. The output unit is the PWM circuit consisted of a clocked CMOS comparator[2]. In the output unit, if a pulse has been generated until a ramp voltage is equal to the output voltage, the pulse width is proportional to the output voltage. A wired-interconnection between two prototype chips is also possible. Therefore, it is possible to check the operation as multi-chip configuration without the spiral inductor module chip. The chip was implemented with a 0.35 um, double-poly, three metals, standard CMOS technology and the die size was 4.5 x 4.5 mm^2.

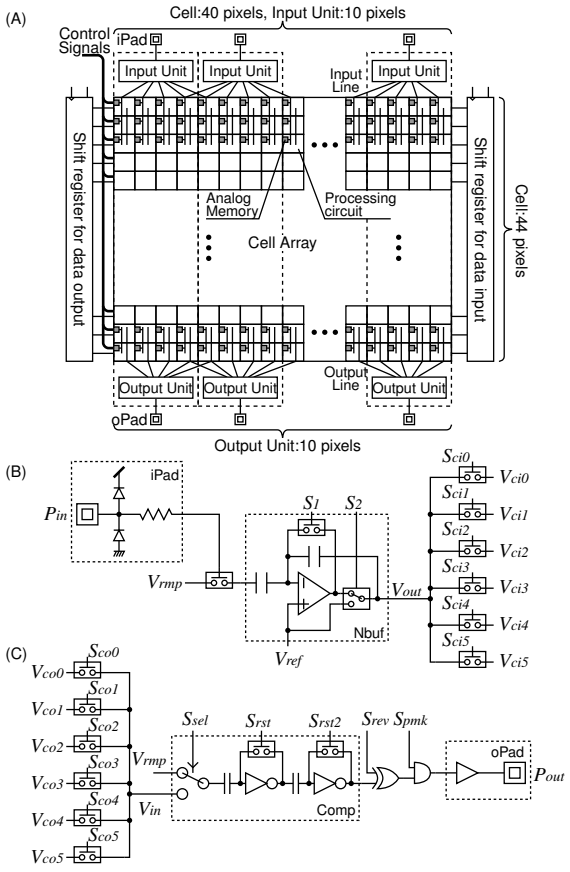

Figure 2: The prototype visual processing chip. (A)Block diagram of the chip, (B)circuit design of the input unit and (C)the output unit.

4 Conclusion

In the present study, we have fabricated the prototype visual processing chip for the system using the 3DCSS configuration. In the next step, we will have to verify the operation of the multi-chip system with wireless interconnection combining the spiral inductor module chip.

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