Study in Structure and Fabrication Process of 3-Dimensional CMOS Transistor

K. Okuyama, K. Kobayashi, S. Matsumura, and H. Sunami

Research Center for Nanodevice and Systems, Hiroshima University
Phone: +81-824-24-6265, Fax: +81-824-22-7185,
E-mail: okuyama@sxsys.hiroshima-u-ac.jp

1 Introduction

It is becoming difficult to control the short channel effect in conventional bulk devices up to date. To overcome this problem, three-dimensional (3-D) device structures, such as FinFET, have been proposed [1]. The aim of this study is to establish fabrication processes of these 3-D CMOS for the next generation. During the course of the study a multi-gate 3-D NMOS transistor, beam channel transistor (BCT) [2] was successfully fabricated as shown in Fig. 1. Since the BCT has higher-aspect ratio than any other 3-D devices, it provides higher drive current per planer area.

2 Fabrication processes of BCT

2-1 High aspect ratio fabrication technique

To realize the BCT, fabrication processes for high-aspect ratio Si-beam and gate electrode are key techniques. With respect to the Si-beam formation, an anisotropic wet etching using TMAH (tetra methyl ammonium hydroxide) is utilized, which can etch {110} at least 30-times faster than {111} has been proposed [2].

Furthermore, it is difficult to form the gate-sidewall spacer same as conventional planer devices. In this study, we have proposed the use of impurity-enhanced oxidation(IEO [3]). Oxidation thicknesses of phosphorous doped n^{+}poly-Si and Si substrate (boron doped, $1x10^{15}/cm^{3}$) are shown in Fig. 2. The ratio of oxidation exceeds almost 10 at 700℃ [4]. Thus the sidewall spacer is formed on the gate electrode surrounding on high aspect ratio Si-beam (Fig. 3).

2-2 Source / drain formation processes

Source and drain (S/D) of the BCT are formed on sidewalls of Si-beams, therefore it is rather difficult to carry out uniform doping on steep and dense beams. Although one way to form the S/D is the phosphorous diffusion by $POCl_3$ gaseous doping, controlled doping is rather difficult as compared to ion implantation. Therefore, ion implantation and/or plasma doping are applied to the BCT. It is important to adjust an angle of inclination with the ion implantation. In plasma doping, relatively isotropic doping can be realized. From this point of view, this may be suitable for 3-D device fabrication, despite its wide distribution of doping energy.

2-3 Silicidation of source and drain

A beam width dependence of the drain on-current, as shown in Fig. 4, may imply that parasitic series resistance of S/D causes the drain current decrease in previous devices [4]. This estimation is supported by experimental results shown in Figs. 5 and 6. Figure 5 shows that rapid increase in series resistance at less than beam width of 300 nm. The spacing between gate to contact dependence of drain current is shown in Fig. 6. From these experimental results, it is inevitable to reduce the S/D parasitic resistance in the BCT fabrication.

Thus, silicidation process of source and drain is planned to be utilized along with gate sidewall spacer formed by IEO.

3 Conclusion

Fabrication processes of BCT are presented. The main goal of this study is to establish compromising of fabrication processes for 3-D CMOS transistor with very high-aspect ratio Si beams.

4 Acknowledgements

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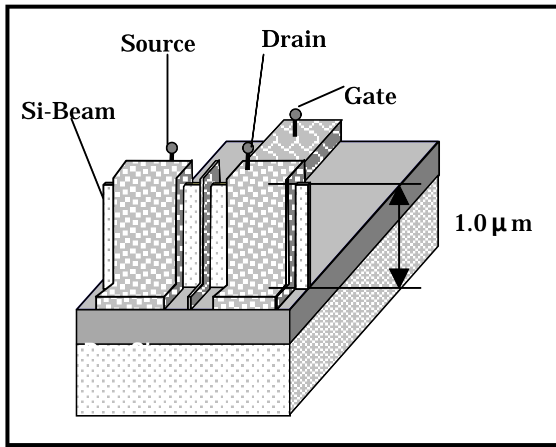


Fig. 1 Schematic diagram of 3-D transistor having beam channel which is 1.0 μm in height and 40 nm in width.

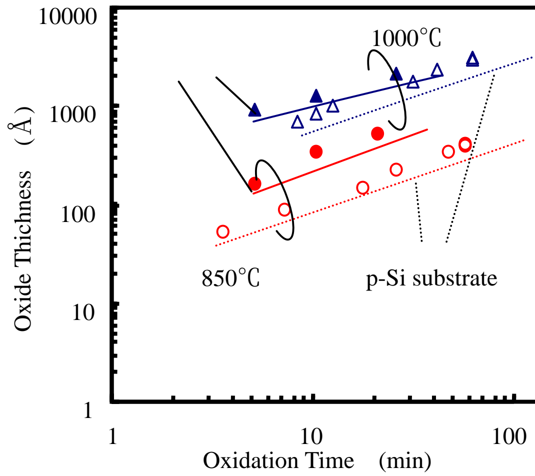


Fig. 2 Oxidation thicknesses of P doped n⁺poly-Si and Si substrate.

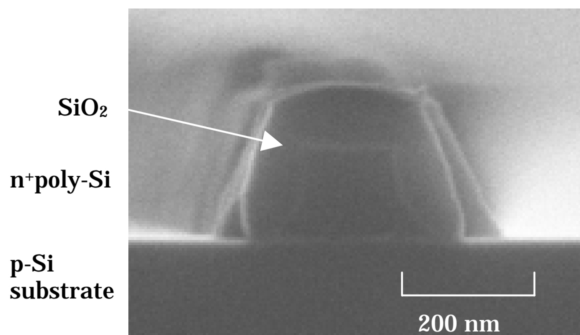


Fig. 3 Cross-sectional SEM photograph for obtained gate structure.

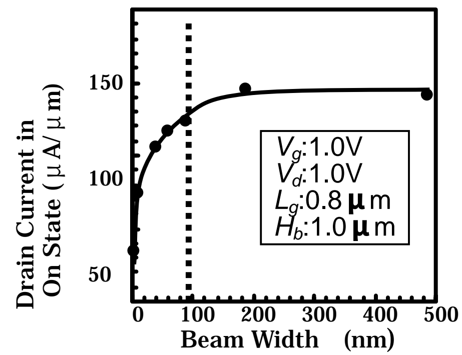


Fig. 4. Dependence of I_d on W_b in on state.

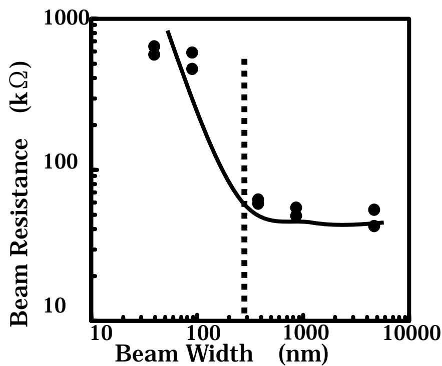


Fig. 5 Parasitic series resistances of S/D depending on beam width.

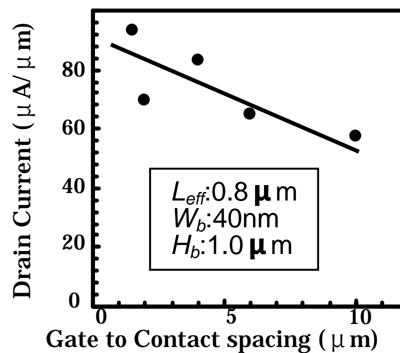
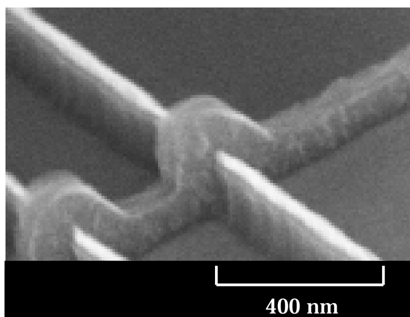
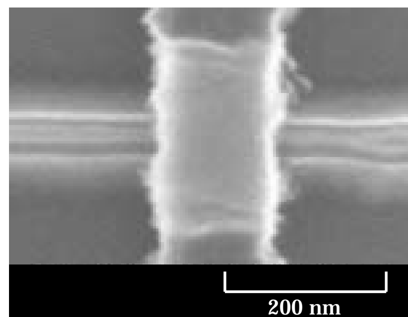


Fig. 6 Drain current decrease due to parasitic resistance of S/D.



(a) Bird's eye view



(b) Plan view

Fig. 7 SEM photographs of a Si-beam of 120 nm in height and 60 nm in width and a poly-Si gate electrode overlaying the beam.