Study in Structure and Fabrication Process of 3-Dimensional CMOS Transistor

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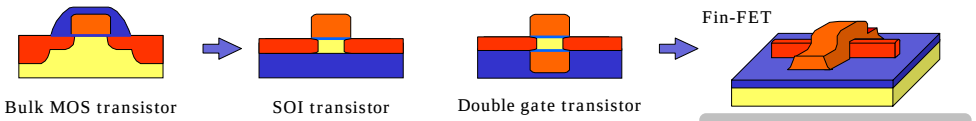
1 Introduction

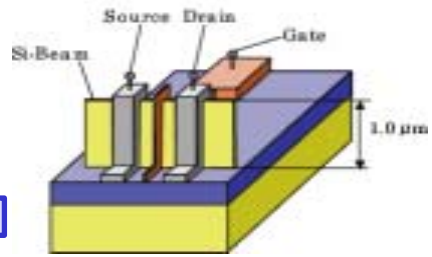
It is becoming difficult to control the short channel effect in conventional bulk devices up to date.

To overcome this problem, three-dimensional (3-D) device structures, such as Fin-FET, have been proposed.



The aim of this study is to establish fabrication processes of these 3-D CMOS for the next generation.

During the course of the study a multi-gate 3-D NMOS transistor, **beam channel transistor (BCT)** was successfully fabricated.



Beam Channel Transistor

Beam channel transistor :

Higher aspect ratio rather than any other 3-D devices

Higher drive current per planer area

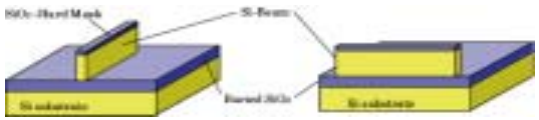
2 Process sequence of BCT

To realize the BCT, fabrication processes for high-aspect ratio Si-beam and gate electrode are key techniques.

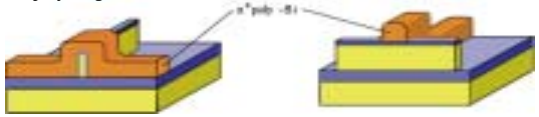
A gate sidewall formation by anisotropic dry etching is difficult for 3-D devices.

A sidewall formation utilized the impurity enhanced oxidation (IEO) has been proposed.

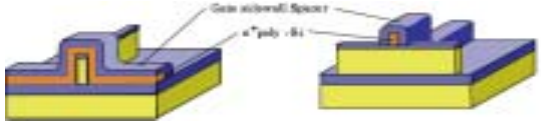
Si-beam formation on a SOI wafer



n^+ poly-Si gate electrode formation

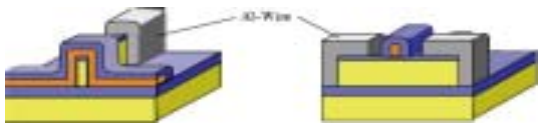


Gate sidewall fabrication by impurity enhanced oxidation (IEO)



Source / drain formation

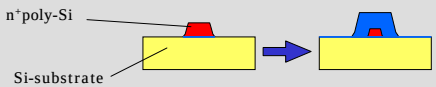
Contact hole etching



3 Formation of a gate sidewall spacer by impurity enhanced oxidation (IEO)

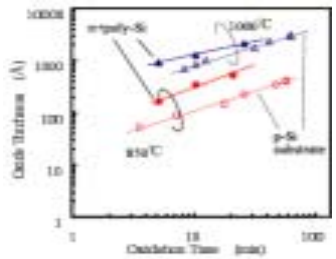
Ratio of oxidation

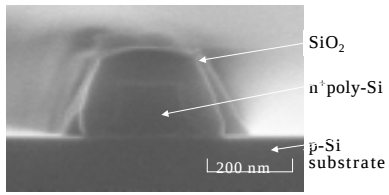
n^+poly-Si gate electrode (phosphorous doped , ～10^{20}/cm^3)	:	Si-substrate (boron doped 1×10^{15}/cm^3)
1000℃ Wet 1.2～1.3	:	1
850℃ Wet 2～3	:	1



The ratio of oxidation exceeds almost 10 at 700℃.

Utilizing this property, a gate sidewall spacer on the gate electrode surrounding on high aspect ratio beams was successfully formed.





Cross-sectional SEM photograph for obtained gate structure

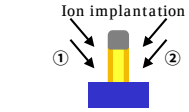
4 Source / drain formation processes

4.1 Source / drain doping

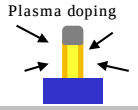
Source and drain (S/D) of the BCT are formed on sidewalls of Si-beams.

It is rather difficult to carry out uniform doping on steep and dense beams.

Ion implantation with inclination and/or plasma doping are applied to the BCT.



・Adjustment of inclination angle is needed.

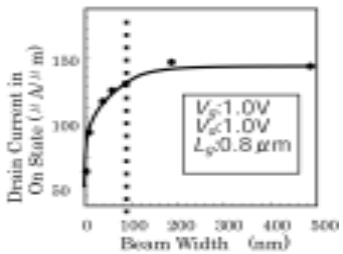


・Relatively isotropic doping is realized.

4.2 Silicidation of source and drain

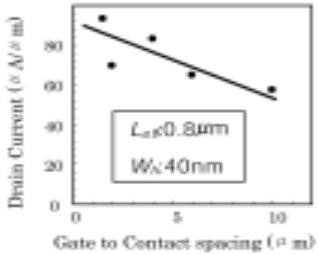
The effect of parasitic resistance of source and drain

i) Dependence of drain current on beam width in on-state



The drain on-current decreases rapidly at less than beam width 100 nm.

ii) Dependence of drain current on gate to contact spacing

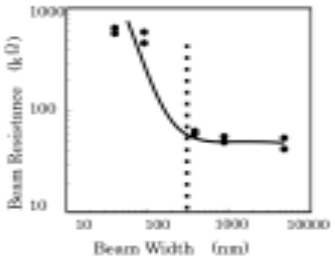


The gate to contact spacing strongly affects drain current at narrow beam width W_b.

Resistance of Si-beams increase rapidly when its width become smaller than 300 nm.

Parasitic series resistance of source and drain causes decrease in drain current.

Resistance of phosphorous doped Si-beams



It is inevitable to reduce the parasitic resistance of the source and drain in the BCT fabrication.

A silicidation process of source and drain that utilizes gate sidewall by IEO.

5 Conclusion

Fabrication processes of BCT are presented. The main goal of this study is to establish compromising of fabrication for 3-D CMOS devices.

- Gate sidewall formation on the gate electrode surrounding on high aspect beams was successfully formed by IEO.
- Parasitic series resistance of source and drain strongly affects the drain current. → Reduction of the parasitic resistance is needed for The BCT fabrication.

→

- A silicidation process of source and drain is planned to be utilized gate sidewall formed by IEO.