Workfunction Tuning for Single-Metal Dual-Gate CMOS with Mo and NiSi Electrodes

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1. Introduction

Dual-workfunction gates with single metal are expected to replace dual-poly-Si gates that accompanies a depletion effect problem. For that purpose metal workfunction tuning must be accomplished maintaining compatibility to conventional CMOS fabrication process.

We have reported the workfunction tuning of Mo with N and its side effects caused by nitrogen implantation [1]. In this paper, application of this technique to MOSFETs and found issues are described. In addition, preliminary results of the workfunction tuning with NiSi that was formed with fully silicided poly-Si are reported.

2. Mo Gate MOSFETs

The workfunction shift of Mo is first achieved with N^+ implantation [2]. However, we have fabricated MOSFETs [3] with solid phase N diffusion from TiN deposited on Mo [4], because N^+ implantation causes damages to gate oxides [5]. Though expected V_{th} shift due to the N diffusion was 0.45 V that is equal to V_{FB} shift of MOS diodes, the V_{th} shift of fabricated MOSFETs was 0.1 V, as shown in Fig. 1. Nitrogen depth profiles in Mo MOS structure was evaluated to discuss reason why the V_{th} shift was shrunk (Fig. 2). N pileup at the Mo/SiO_2 interface for the diode process reduces by adding source and drain (S/D) activation annealing, in other words, by changing fabrication process to FET process. Nitrogen concentration in Mo was also decreased by the annealing. These results indicate that the nitrogen pileup reduction due to the nitrogen out-diffusion through a Mo film is the origin of reversible workfunction behavior [3]. In the case of the fabricated MOSFETs, Mo gates are surrounded by CVD grown SiO_2 during the S/D activation annealing. N atoms located at the Mo/gate SiO_2 interface are considered to redistribute to other CVD SiO_2 interfaces, as shown in Fig. 3. Figure 4 shows modified MOSFET fabrication process to prevent the N redistribution problem.

3. Workfunction Tuning of NiSi Gate

Workfunction shift of fully silicided poly-Si gate with Ni, in other words, NiSi gate is recently reported [6,7]. NiSi will be adopted as a material for salicide process for 65-nm technology-node CMOS. Impurities implanted into the poly-Si gate prior to the silicidation, are swept out towards the oxide interface by snowplow effect [8]. As a result, impurity pileup is formed at the NiSi/SiO_2 by full silicidation of poly-Si (Fig. 5). The workfunction shift with B, P, As, and Sb were reported to date. We have investigated how silicidation condition affects the workfunction shift and the pileup formation with Sb. MOS diodes are fabricated with the process step shown in Fig. 6. C-V characteristics of the MOS diodes show large V_{FB} shift for the silicidation temperature of 450°C and 400°C, however that for 500°C is nearly zero, as shown in Fig. 7. By lowering silicidation temperature, silicidation rate is also lowered. The snowplow effect is considered to be enhanced by slowing down silicidation rate. Sb depth profiles shown in Fig. 8 support this idea showing pileup peak height change. Since silicidation process is usually carried out after high temperature annealing process, redistribution of impurities in the pileup will not be a problem for integrating the full silicidation into device fabrication process.

4. Summary

Workfunction tuning utilizing impurity pileup at the metal/SiO_2 interface has been investigated. In the case of N in Mo-gate, it showed reversible redistribution by additional thermal treatment. This caused difficulties in application of the workfunction tuning to Mo-gate MOSFET. In the case of Sb in NiSi gate, silicidation temperature that affects silicidation rate and the snowplow effect was the key to obtain workfunction shift.

Acknowledgements

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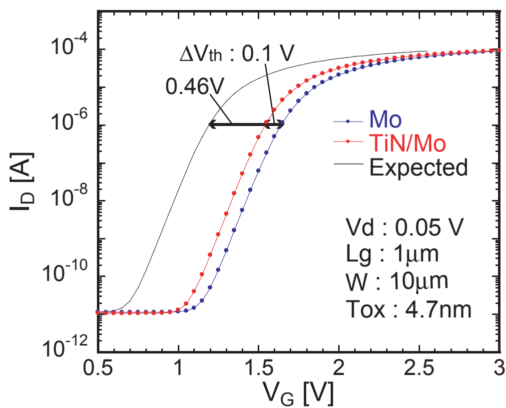

Fig. 1 I_D-V_G characteristics of TiN/Mo and Mo gate MOSFETs. V_{th} shift due to workfunction change is smaller than the value expected from V_{FB} obtained with MOS diodes.

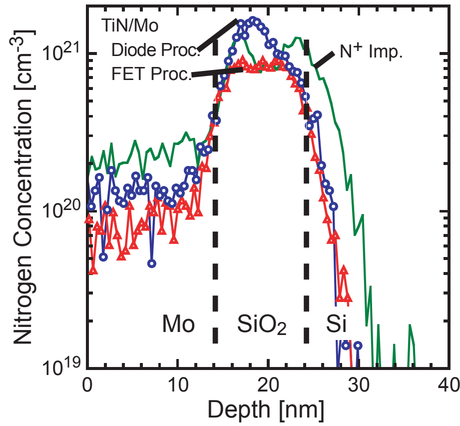

Fig. 2 Nitrogen depth profiles obtained by back-side SIMS technique. Nitrogen pileup formed at the Mo/SiO_2 interface reduces by the FET-like process that includes an RTA step after TiN stripping for S/D activation.

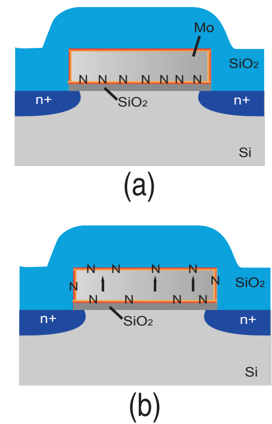

Fig. 3 Nitrogen re-distribution during Mo-gate MOSFET fabrication. (a) befor and (b) after S/D activation annealing.

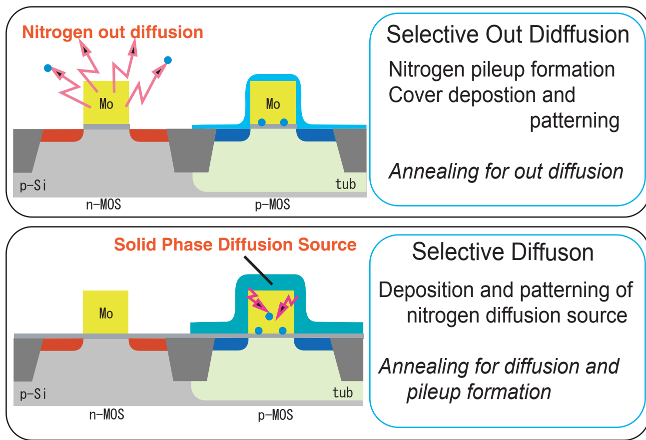

Fig. 4 Workfunction adjustment methods for CMOS fabrication. (a) selective out diffusion method and (b) selective diffusion method. Annealing is originally necessary for S/D activation.

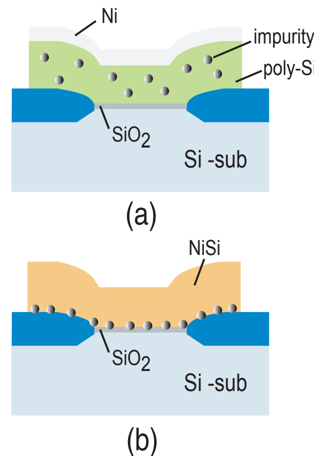

Fig. 5 Pileup formation during NiSi full-silicidation by snowplow effect. (a) before and (b) after full silicidation

- p-Si(100)
- LOCOS Isolation
- gate oxidation 10nm

- 100 nm poly-Si deposition
- impurity implantation (Sb^+, B^+, P^+ etc.)
- 60 nm Ni sputter-deposition
- NiSi full silicidation (130 nm) 400°C 32 min, 450°C 25 min, 500°C 5 min
- unreacted Ni removal
- post metallization annealing

Fig. 6 Fabrication process flow of NiSi-gate MOS diodes for workfunction evaluation.

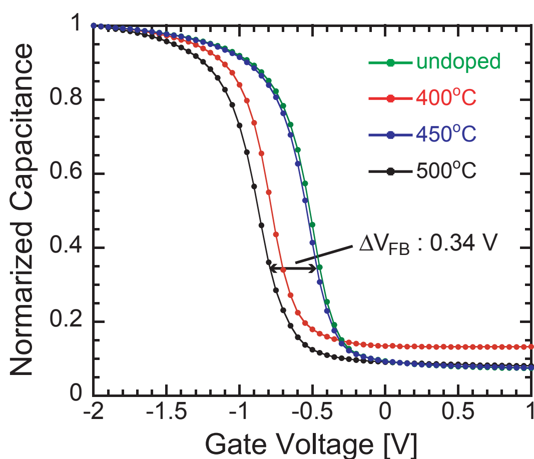

Fig. 7 C-V characteristics of NiSi-gate MOS diodes. Sb pileup was formed with the snowplow effect. V_{FB} shift is increased by decreasing silicidation temperature.

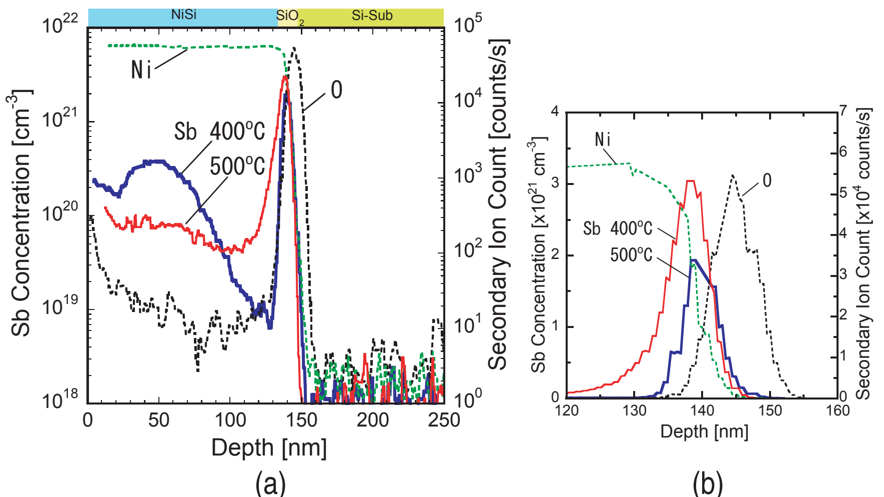

Fig. 8 (a) Sb depth profiles in NiSi-MOS structure obtained with back-side SIMS technique (a) and its closeup around the MOS interfaces. The snowplow effect and pileup formation is prpmoted by lowering silicidation temperature.