Workfunction Tuning for Single-Metal Dual-Gate With Mo and NiSi Electrodes

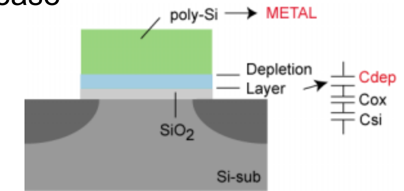
K.Sano, M.Hino, and K.Shibahara

Research Center for Nanodevices and System

Hiroshima University

Motivation

- poly-Si Gate
  - Gate depletion effect
  - -Effective oxide thickness increase
- Metal Gate
  - No gate depletion effect



Issue

Dual Metal CMOSFET ⇨ Complicated fabrication process

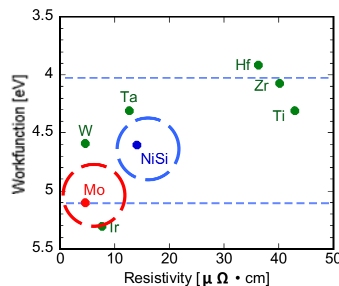
Solution

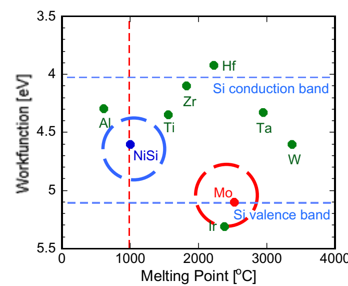
Dual-workfunction gates with single metal

Properties of Metal Materials

Required Properties

- High melting point (>1000°C)
- Low resistivity
- Suitability for the conventional processes





Mo and NiSi match the requirement

→ Possibility of Workfunction Tuning ?

Workfunction Tuning Techniques

- Mo Gate
  - -N⁺ Implantation
    - T.Amada et al., Mat.Res.Soc. 2002
    - Q.Lu et al., Symp. on VLSI 2001
    - K.Shibahara, 2003 COE Workshop
  - -Solid phase diffusion from TiN Film
    - R.J.P. Lander et al., Mat.Res.Soc. 2002
    - M.Hino et al., SSDM 2003
- NiSi Gate
  - -Impurity pileup by snowplow effect
    - W.P.Maszara et al., IEDM 2002
    - J.Kedzierski et al., IEDM 2002 & 2003
- Targets

Mo : Integration into MOSFET fabrication

NiSi : Optimization of silicidation condition for pileup formation

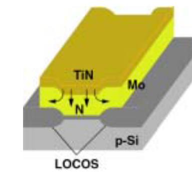
Mo Gate

Solid-Phase Diffusion from TiN Film

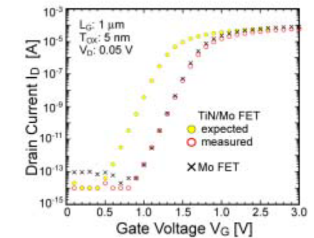
- Workfunction shift

Diode	MOSFET
-0.46eV	～0eV

- Nitrogen out-diffusion from Mo gate?



RTA : Solid-phase diffusion
Temperature : 800°C
Time : 1 min

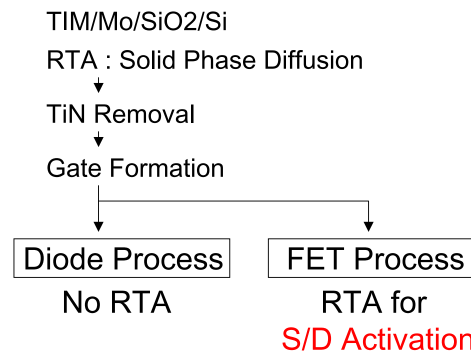


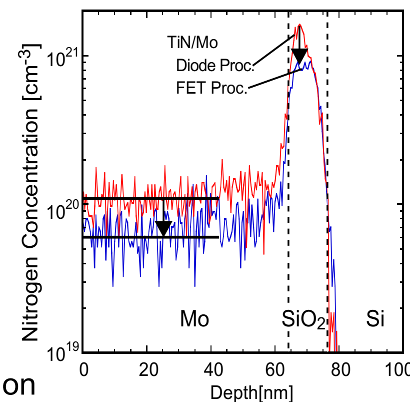
This Work

- Nitrogen Profile in Mo MOS structure
- FET fabrication with modified process steps

[K.Shibahara, 2003 COE Workshop]

Nitrogen Profiles in Mo MOS structure (back-side SIMS)





- Nitrogen reduction by S/D activation at Mo/SiO2 interface in bulk Mo

→ Nitrogen out-diffusion by S/D Activation

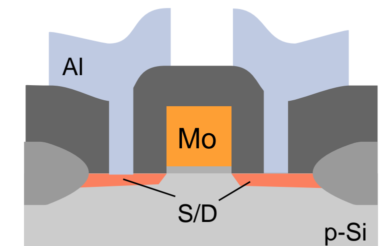
Countermeasure

Deposition SiO_2 before S/D Activation

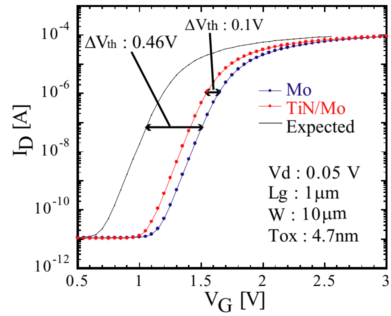
Modified Mo Gate MOSFET Fabrication Process

- P-Si (100)
- Isolation
- Mo and TiN sputter
- Solid-phase diffusion 800°C 1min
- TiN removal
- Gate, patterning and S/D formation
- Interlayer SiO_2 CVD
- RTA : 900°C 1min
- SiO2 CVD@previous
- Al wiring

→ Cover to prevent nitrogen out diffusion



MOSFET I_D-V_G Characteristics

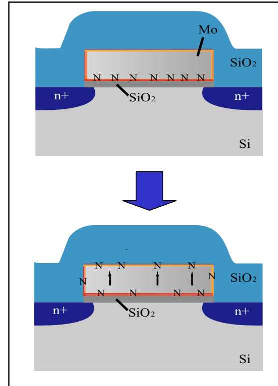


- Fabricated MOSFET

  ΔV_{th} : -0.1V

  (< Diode ΔV_{FB} : -0.46V)

- Improved,but still smaller ΔV_{th}



Speculation

Pileup formation at upper Mo/SiO_2 interface

Decrease in nitrogen concentration at lower interface

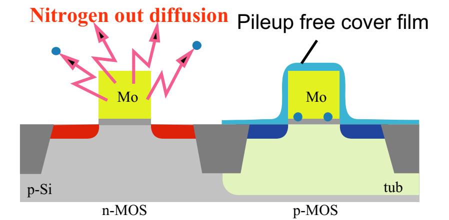
Workfunction adjustment methods for CMOSFET

- Selective Out Diffusion

  Nitrogen pileup formation

  Cover deposition and patterning

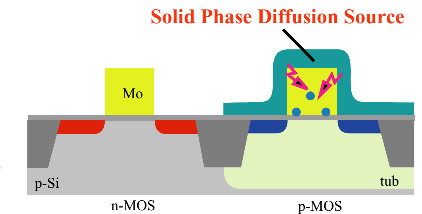
Annealing for out diffusion



- Selective Diffusion

  Deposition and pattering of nitrogen diffusion source

Annealing for diffusion, pileup formation and S/D activation



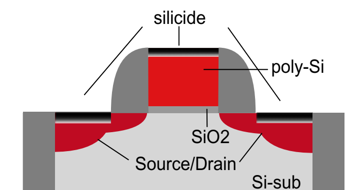
NiSi Gate

Comparison of silicide materials

- $TiSi_2$··· Original salicide material
  Replaced by $CoSi_2$ because of severe narrow line effect
- $CoSi_2$···Currently most popular for salicided CMOS
  Superior thermal stability than NiSi
- NiSi··· Small Si consumption
  Lower contact resistance
  Poor thermal stability
  Suitable for sub-90nm CMOS with low temperature BEOL

and

Candidate for workfunction tunable gate metal



Impurity pileup by snowplow effect in Full-NiSi Gate

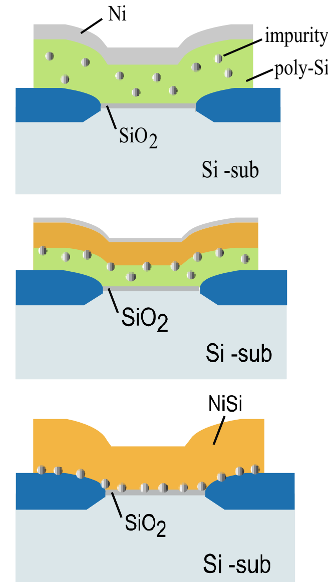
Introduction of impurities in poly-Si

↓ full-silicidation

Pileup at NiSi/SiO_2

⇩

Workfunction shift

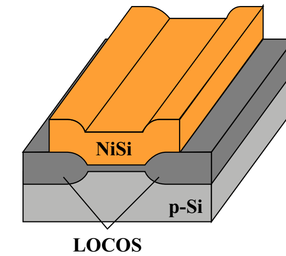


- Snowplow effect

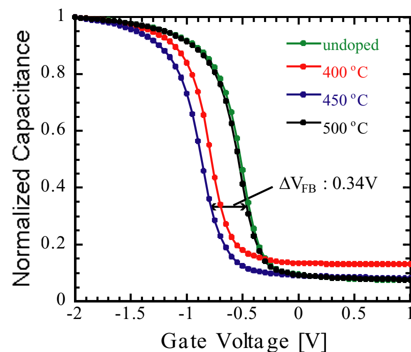
Drive away impurities in Si downward when full-silicidation

NiSi Gate MOS diodes Fabrication Process

- P-Si (100)
- Gate oxidation
- poly-Si deposition
- Impurity implantation
  (Sb^+, B^+, P^+, etc.)
- Ni deposition
- NiSi full-silicidation
  400°C 32min, 450°C 25min
  500°C 5min
- Unreacted Ni removal
- Post metallization annealing



NiSi Gate MOS Diode C-V Characteristics

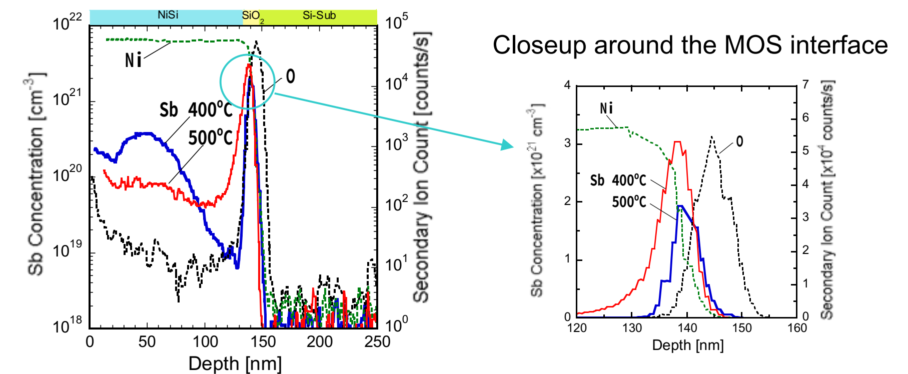


	Silicidation temperature	
	400,450°C	500°C
ΔV_{FB}	0.34V	~0V

- ΔV_{FB} increase by lower silicidation temperature

⇨ Key parameter to snowplow effect

Sb depth profiles in NiSi MOS structure



- Lower silicidation temperature
  → Lower silicidation rate

⇩

Enhancement of snowplow effect by slowing down silicidation

Conclusions

- Nitrogen solid-phase diffusion into Mo gate from TiN
  - Nitrogen pileup and workfunction shift were reversible process.
  - Additional thermal treatment gave rise to nitrogen redistribution.

  MOSFET fabrication :
  - Procedure must be constructed to avoid the pileup deformation.
- Impurity pileup by snowplow effect in NiSi gate
  - Snowplow effect was enhanced by lower temperature at silicidation.

Acknowledgements

This work is partially supported by STARC(Semiconductor Technology Academic Research Center)