A Single Chip UWB Transmitter Based on 0.18μm CMOS Technology for Wireless Interconnection

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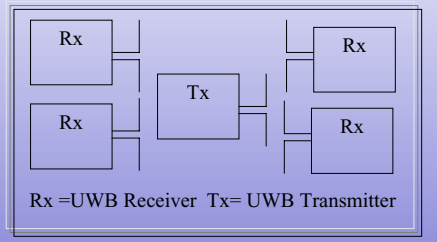
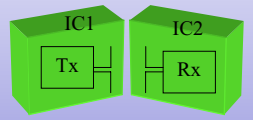
MOTIVATION

⇨ Require **advanced wireless interconnect system to overcome interconnect delay problem in future ULSI**



Intrachip wireless Interconnect



Interchip wireless Interconnect

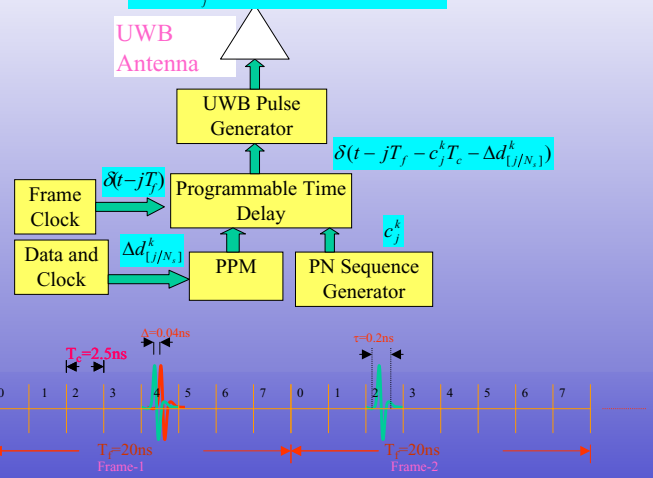
Shannon's Theory

$$C = B\log_2\left(1+\frac{S}{N}\right)$$

High capacity wireless interconnect system requires wide bandwidth Transmitter, Receiver and Antenna.

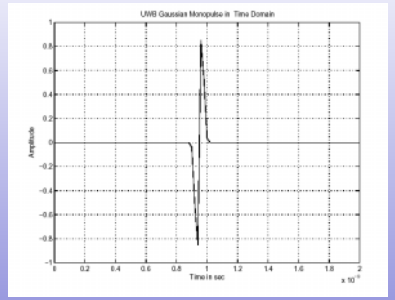
UWB TRANSMITTER

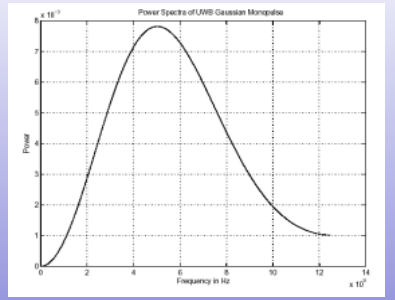
$$s^k(t) = \sum_j w\left(t - jT_f - c_j^k T_c - \Delta d^k_{[j/N_s]}\right)$$



Transmitted pulse.

UWB PULSE





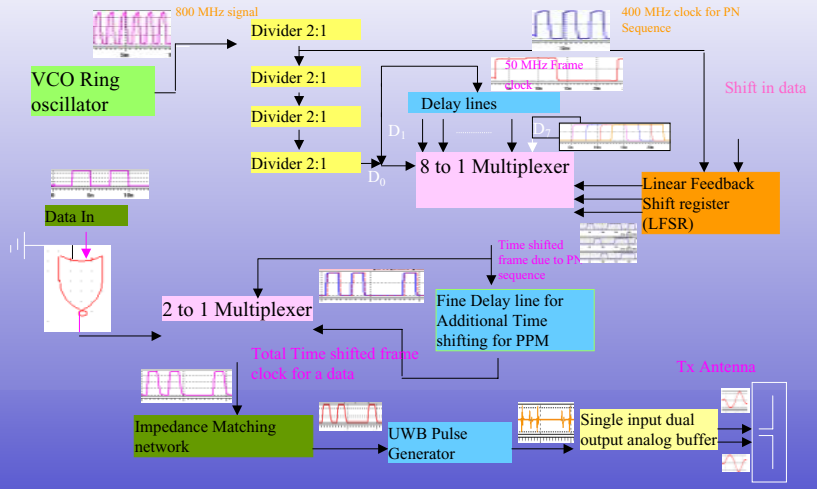
$$w(t) = 2A\sqrt{\pi}\, e\, \frac{t}{\tau} e^{-2\pi\left(\frac{t}{\tau}\right)^2}$$

τ- Pulse Width

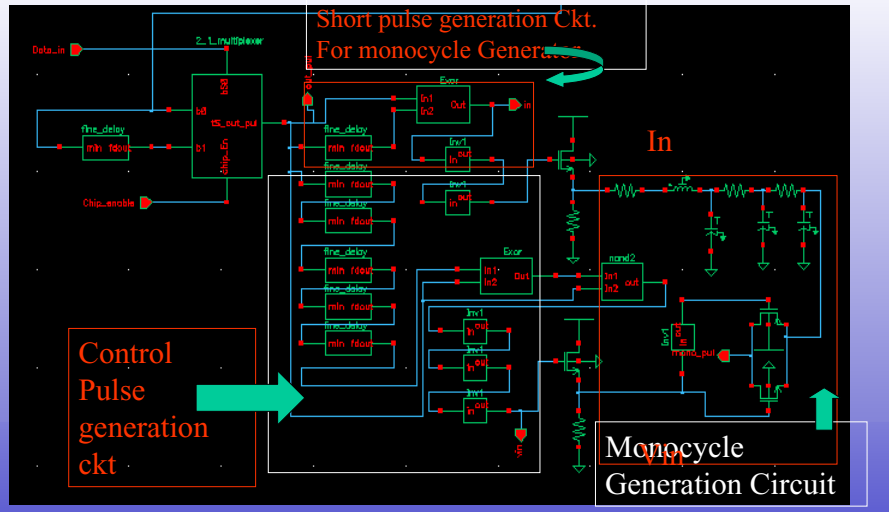
A – Pulse Amplitude

- Monocycle is used as UWB pulse because of no dc component and widebandwidth.
- Halfpower bandwidth is about 116% of monocycle center frequency.

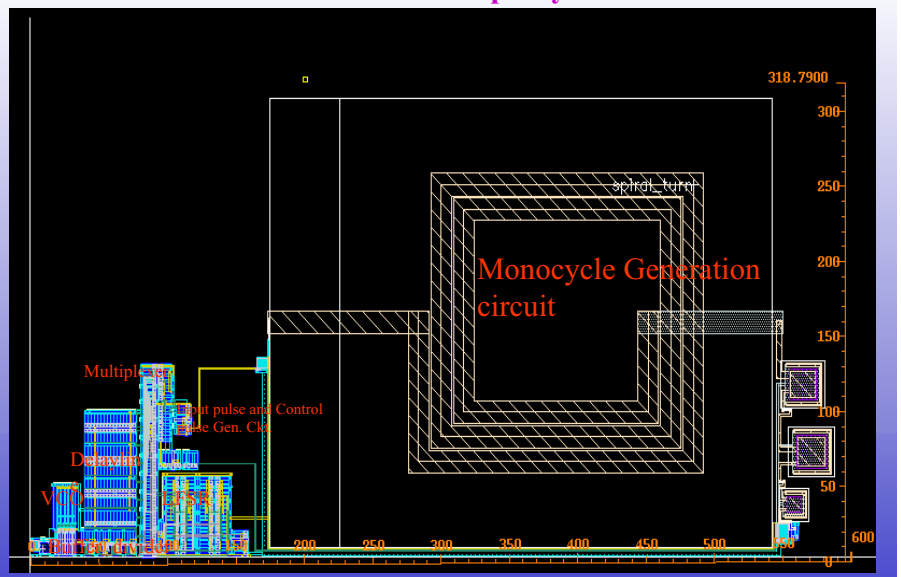
SINGLE CHIP UWB TRANSMITTER CIRCUIT



UWB Pulse Generator



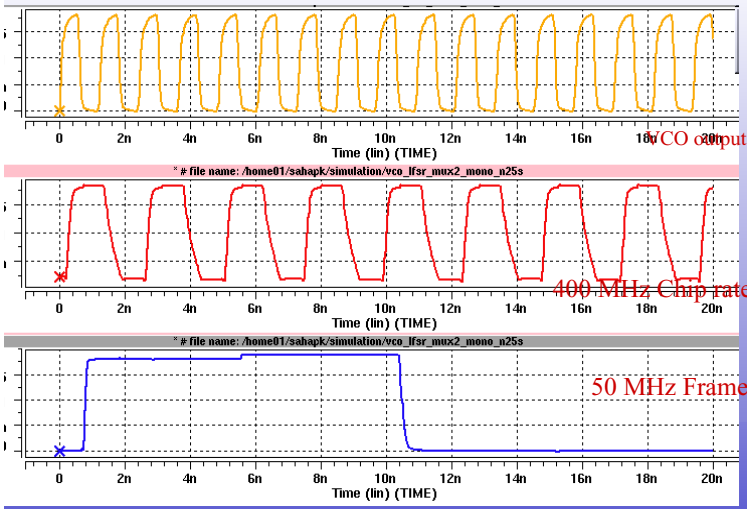
Transmitter Chip Layout



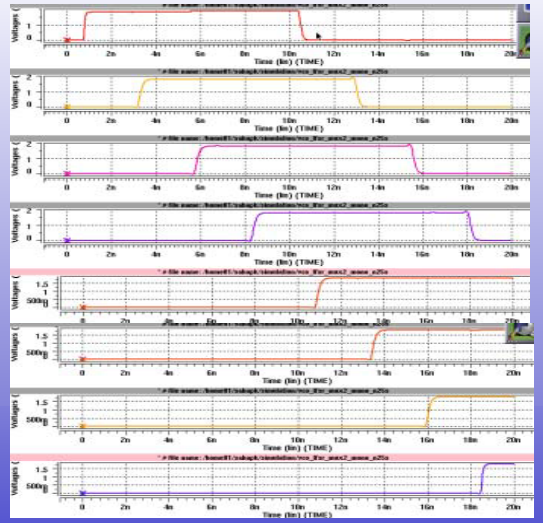
CIRCUIT DESCRIPTION

- Five stage current straved inverter with transmission gate at each stage in series are used to form a voltage controlled ring oscillator to produce frame clock via divider circuit.
- Linear feed back shift register is implemented using clock controlled D-type flip-flop with Exclusive-or (EXOR) as Feedback logic for PN sequence generation.
- Eight to 1 multiplexer is implemented using NAND and NOR gate to select time shifted frame in accordence with PN sequence.
- Time shifted frame is generated using delay generation circuit based on a delay line which consists of a number of buffer stages connected in series.
- The pulse generator circuit which consists of LC oscillator with RC filter produces damped sinusoidal like wave from short pulse (In) generated from the time shifted signal. This signal is then passed through transmission gate which is controlled by control pulse (Vin) of desired width generated from the same time shifted pulse to pass the first cycle of the generated signal at the output.

Simulation Results

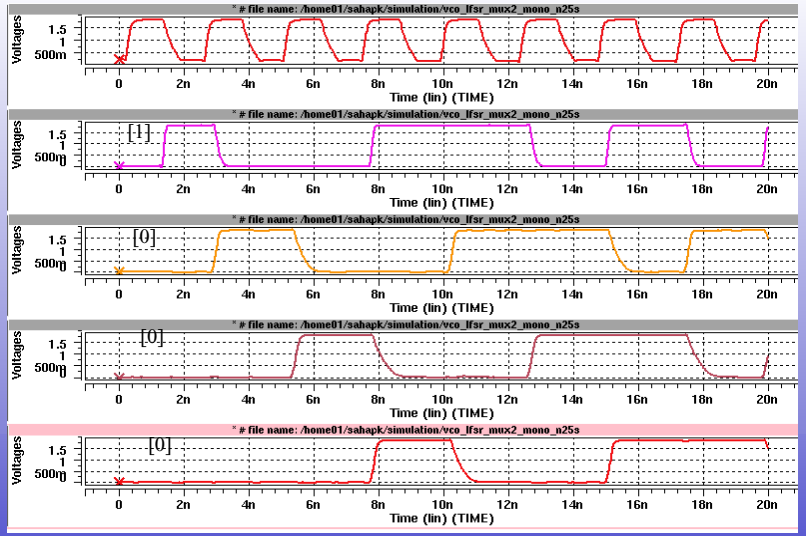


Simulation Results (contd.)



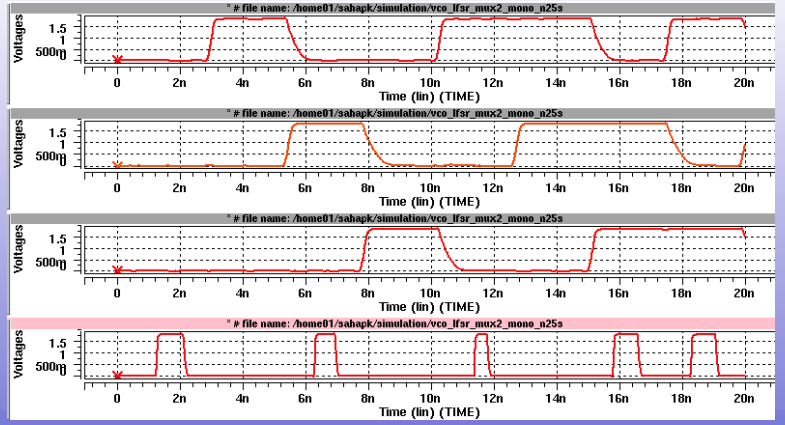
Time shifted frame from 2.5ns to 17.5 ns generated from delay line.

Simulation Results (contd.)



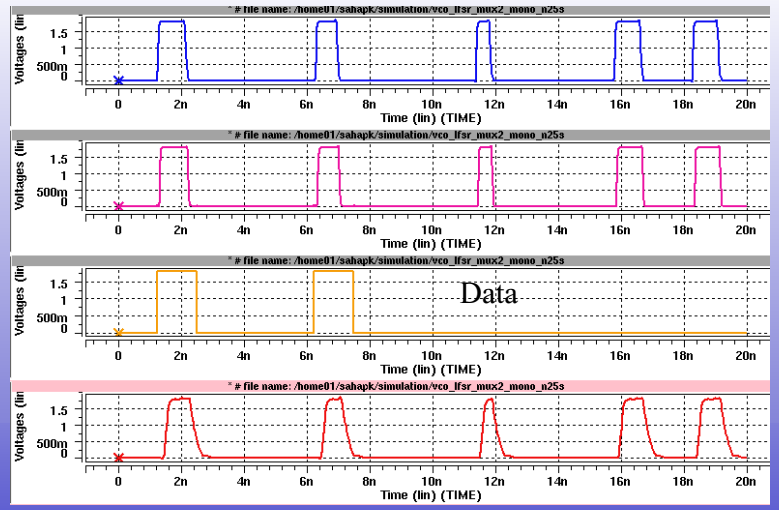
PN sequence from LFSR for initial loading of [1000] and chip rate of 400 MHz.

Simulation Results (contd.)



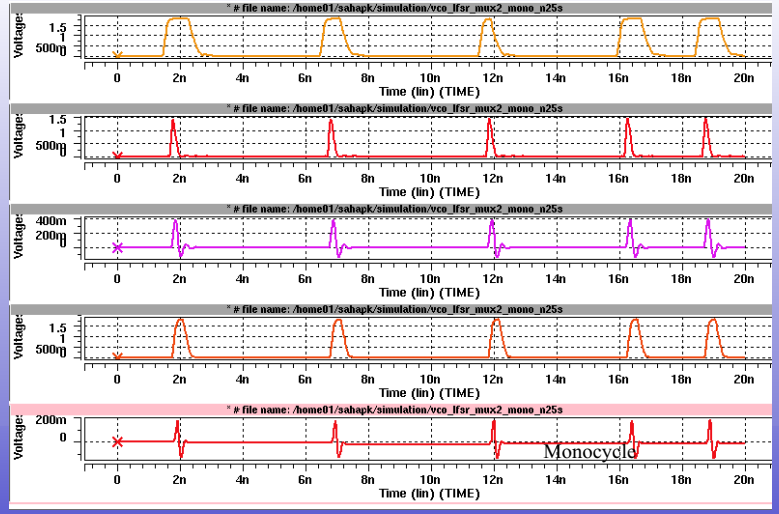
Time shifted signal from Eight to 1 multiplexer output according to PN sequence.

Simulation Results (contd.)



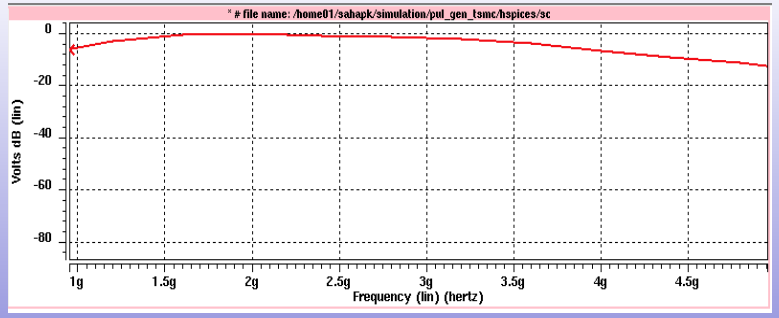
Two to 1 multiplexer output containing data generated from time shifted pulse after shifting due to PPM.

Simulation Results (contd.)



Proposed UWB transmitter output is a Monocycle containing data.

Simulation Results (contd.)



FFT of the generated monocycle pulse having halfpower bandwidth of 2 GHz.

CONCLUSION

- Proposed UWB transmitter circuit is almost digital architecture except monocycle pulse generation circuit.
- Monocycle pulse which will contain information can be generated from the time shifted pulse using the current CMOS technology
- Since the monocycle is generated from the time shifted pulse, it is only necessary to keep constant gate delay with any variation of vdd and substrate voltage.
- Monocyle pulse bandwidth can be increased by changing the inductance or capacitance and control pulse width which is equal to monocyle pulse width.