A Single Chip UWB Receiver based on 0.18-μm CMOS Technology for Wireless Interconnection

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1. Introduction

Although metal wiring is used for signal transmission of conventional integrated circuit, signal delay will become serious for future ULSI because of an increase of parasitic capacitance and resistance. To solve this problem, wireless intra-chip global clock transmission using integrated antenna have been proposed [1][2]. Recently, UWB (Ultra Wide Band) technology [3] has been developed for short distance communication. In this paper, a wireless inter-chip data communication system using UWB is presented. Here, a single chip UWB receiver based on 0.18-μm CMOS technology is studied, and results of HSPICE simulation are presented.

2. Circuit design

The functional circuit block diagram of UWB receiver is shown in Fig. 1. The receiver receives the pulse train with pulse position modulation (PPM) and time hopping spread spectrum (THSS)

$$s(t) = \sum_j \omega(t - jT_f - c_j T_c - \delta d_j), \quad (1)$$

where, $s(t)$, $\omega(t)$, T_f, c_j, T_c, δ and d_j are received pulse train, monocycle pulse, frame time, time hopping sequence, chip rate, a unit time shift of pulse position modulation and a binary data, respectively. In the case of data d_j=1, the arrival of the pulse is delayed for a short time δ. Here $\omega(t)$ is given as the 2nd derivative of Gaussian pulse

$$\omega(t) = 2\sqrt{e}A\{1 - (\frac{\pi t}{\tau})^2\}e^{-2(\pi t/\tau)^2}. \quad (2)$$

Impedance matching circuit is inserted to suppress the reflection of the signal. After amplification by low noise amplifier (LNA), mixer multiplies the received signal by the template signal to perform demodulation

$$v(t) = \omega(t) - \omega(t - \delta), \quad (3)$$

where, $v(t)$ is a template signal.

The mixer output is integrated by time, and S/H circuit holds the value of integration. Finally, Comparator distinguishes d_j=0 or d_j=1. The receiver circuit design is performed using TSMC 0.18-μm mixed signal design rule (V_{dd}=1.8V). Figure 2 shows the layout of an analog part (impedance matching - mixer) of the receiver. The differential implementation is adopted to reduce the common mode noise.

3. Results of HSPICE Simulation

The 2nd derivative Gaussian pulse (center frequency = 7GHz, 3dB bandwidth = 5.8GHz) is given as an input of the receiver. Figure 3 shows a schematic diagram of the impedance matching circuit. Frequency response of the magnitude of input impedance is shown in Fig. 4. It shows almost a flat response above 4GHz. Resulting value of input impedance is 123Ω at 4GHz, and 107Ω at 10GHz. The voltage gain of impedance matching circuit is low (2dB at 4GHz and 1dB at 10GHz), because it cannot decrease the common mode noise. The schematic diagram of differential LNA is shown in Fig. 5. The voltage gain of the amplifier is 10dB at 4GHz, and 5dB at 10GHz. This low gain is improved using two-stage common source amplifier. However, a simple connection between the same amplifiers caused a decrease of high frequency gain because of the gate-source coupling capacitance of the 2nd stage amplifier. Thus the smaller size transistor is used for the input of 2nd stage amplifier. Figure 6 is the frequency response of the voltage gain after (a) impedance matching circuit (b) 1st stage amplifier (c) 2nd stage amplifier. Obtained voltage gain after 2nd stage amplifier is 18dB at 4GHz, and 9.3dB at 10GHz. Figure 7 show results of time domain analysis for (a) input (b) after impedance matching circuit (c) after 1st stage amplifier (d) after 2nd stage amplifier. Obtained voltage gain after 2nd stage amplifier is 13dB.

4. Summary

A single chip UWB receiver based on TSMC 0.18-μm CMOS technology is studied and results of HSPICE simulation are presented. Input impedance shows almost a flat frequency response, and the value is 123Ω at 4GHz, and 107Ω at 10GHz. For the 2nd derivative Gaussian input pulse (center frequency = 7GHz, 3dB bandwidth = 5.8GHz), LNA obtained the voltage gain of 13dB.

References

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[2] A. B. M. H. Rashid, S. Watanabe and T. Kikkawa Jpn. J. Appl. Phys. Part 1, 4B, 42(2003)2204.
[3] M. Z. Win and R. Scholtz, IEEE Trans. on Communication. 48 (2000) pp679-691.

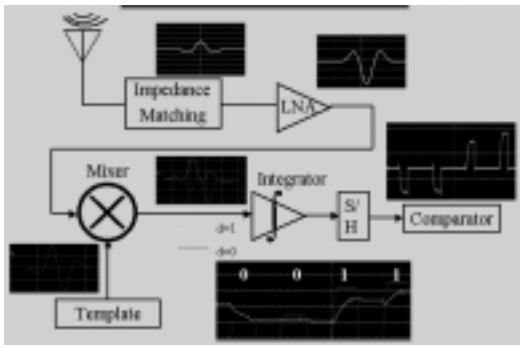

Fig. 1 Functional block of UWB receiver.

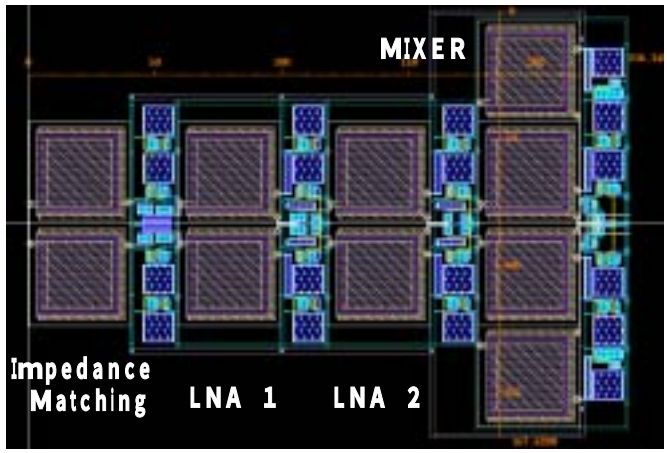

Fig. 2. Receiver layout design.

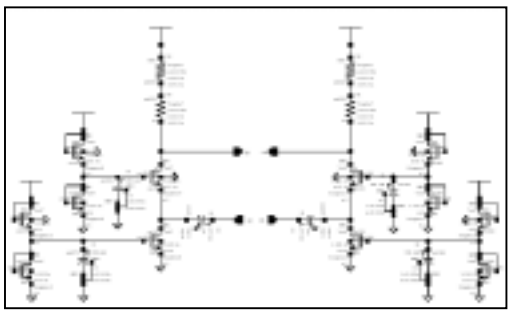

Fig. 3. Schematic diagram of impedance matching circuit.

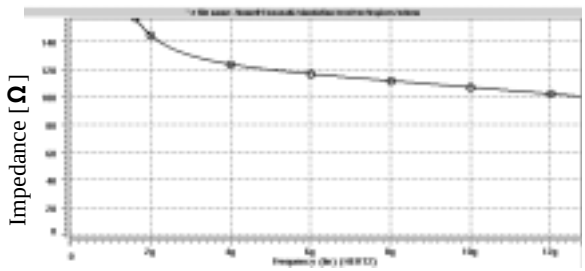

Fig.4. Frequency response of input impedance.

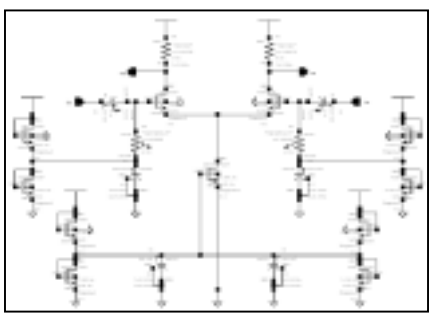

Fig. 5. Schematic diagram of LNA.

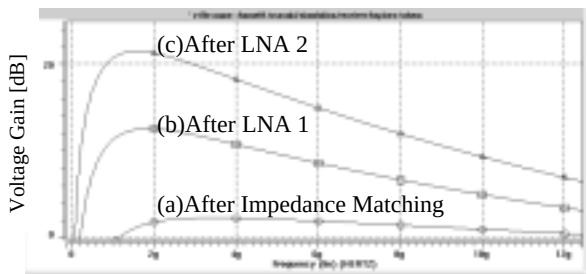

Fig.6. Frequency response of voltage gain.

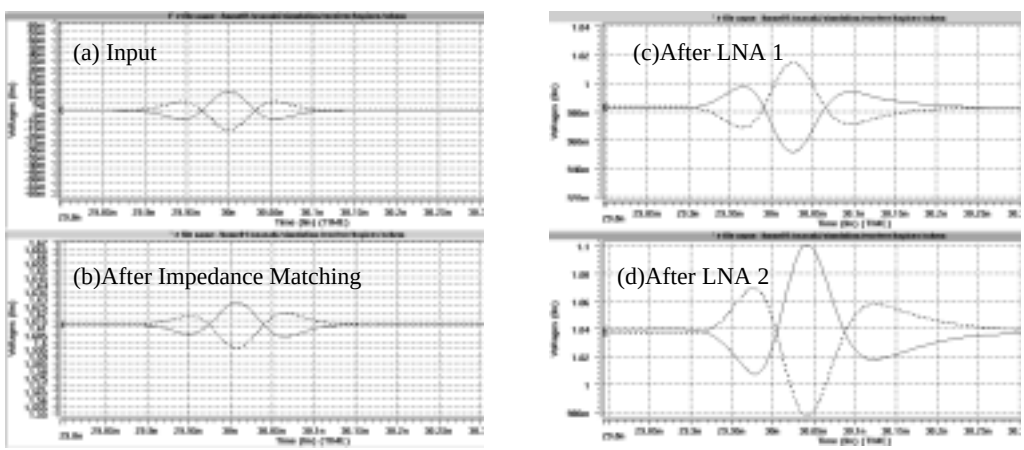

Fig.7. Time domain analysis of UWB receiver.