A wireless chip interconnect using resonant coupling between spiral inductors

Mamoru Sasaki, Daisuke Arizono and Atsushi Iwata
Hiroshima University
Kagamiyama 1-4-1
Higashihiroshima-shi, Hiroshima, Japan
Phone 0824-24-7686, Fax 0824-24-7686, E-mail sasaki@dsl.hiroshima-u.ac.jp

1. Introduction

With the continuous downsizing of CMOS technology, various components such as processors, memories, analog circuits, RF interface, are integrated in a single chip. It is called a system LSI. However, it takes considerable time to develop system LSIs, and the integration of a wide variety of system functions on a single chip invites considerable low yield. As an alternative, attention has been drawn to the System-in-Package. Also in our COE program, development of the 3-Dimensional Custom-Stack System (3DCSS) is one of the significant themes. In conventional 3D IC fabrication technique, vias with large aspect-ratio are required, in order to connect the stacked chips. A wireless interconnect utilizing capacitor coupling has been proposed and it may avoid forming the vias [1]. However, the distance between the stacked chips can not be extended so as cool the internal circuits, because of the capacitive coupling. Thus, the heat dissipation issue is still unsolved. Two types of wireless connection are studied in our COE program. One is global connection, which communicates beyond neighboring chips using microwave [2]. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. The global connection is useful for broadcasting, global control, etc. On the other hand, the local connection can handle huge data volumes due to the massive parallel structure, and it is useful for communication of 2D vision information. In this manuscript, we propose a wireless interconnect for the local connection utilizing resonant coupling between spiral inductors (see Fig.1).

2. Analysis and modeling of spiral inductor pair

In order to utilize circuit simulators for the design, we introduce an equivalent circuit of the spiral inductor pair. Fig.2 shows the simple equivalent circuit. L, C, and R are the self-inductance, parasitic capacitance and loss resistance of the spiral inductor, respectively. M and k are the mutual inductance and the coupling coefficient between the spiral inductor pair. 2-port S-parameter data has been obtained from FDTD 3D electromagnetic-field analysis. Then, the element values in Fig.2 were decided by data-fitting to the 2-port S-parameter data. The result is shown in Fig.3. In layout of the spiral inductor, line width and space were 10 μm and 2 μm, respectively. The shape was square and the outer diameter was fixed at 300 μm. As parameters, the number of turns and distance between the spiral inductor pair were selected. Fig.3 shows the relationship between the self-inductance and the number of turns. It also shows the relationship of the coupling coefficient. The three curves are drawn, when the distance between the spiral inductor pair is 50 μm, 100 μm and 150 μm, respectively.

3. Circuit configuration and SPICE simulations

Figure4 shows a circuit diagram including the model of the spiral inductor pair. Note that capacitors Ca_1 and Ca_2 are connected to the inductors L_1 and L_2, in order to implement resonators in both the transmitter and the receiver. Although the spiral inductor without the additional capacitor has self-resonant frequency, Ca_1 and Ca_2 reduce the resonant frequencies until the convenient frequency for typical communications. A MOSFET M_1 works as driver in the transmitter. A return zero signal shown in Fig.5 is given to the gate of M_1. The resonant frequencies of the resonators in both the transmitter and the receiver are made equal to the transmission frequency of the return zero signal, by connecting the capacitors Ca_1 and Ca_2. The resonance property enlarges the received signal. On the other hand, it causes the excess oscillation due to the resonance phenomenon as shown in Fig.6. In order to suppress the excess oscillation, MOSFETs M_2 and M_3 are employed. Timing signals t_1 and t_2 in Fig.6 control the M_2 and M_3, respectively. Thus, they short out L_1 and L_2 at the timing as shown in Fig.6 and can suppress the excess oscillation.

The transmitter circuit and the receiver circuit including spiral inductors have been implemented in TSMC 0.25 μm mixed CMOS technology and they were simulated by SPICE. In the simulation, the equivalent model of the spiral inductor pair is used. The supply voltage VDD is 2.5V, in all simulations. Fig.6 shows the simulation results. As shown in the lowest stage of Fig.6, the excess oscillation can be successfully suppressed, although the leakage of the timing signal t_2 through the parasitic element of M_3 causes a slight oscillation. The resonance property can enlarge the amplitude of the received signal and it results in lower power consumption. In fact, an average of the current flowing into the driver M_1, which consumes the most power, can be reduced down to 2.4mA.

The distance between stacked chips should be varied due to system level restrictions such as heat dissipation. It affects especially the amplitude of the received signal. In order to suppress the affection, a reference-voltage generator is proposed. Fig.7 shows the circuit diagram. It can generate a reference voltage for the comparator from the amplitude of the current received signal. A source follower buffers the received signal. Simultaneously, the voltage level is shifted down by the threshold voltage of the MOSFET M_4. Moreover, a peak voltage is detected by a MOSFET M_5 which operates as diode. Because the level-shift voltage of the source follower is equal to the threshold voltage of M_5 working as diode, a peak voltage of the received signal can be obtained at the node A. The reference voltage for the comparator is generated by dividing the peak voltage into 1/2. The simulated results are shown in Fig.8 and a proper reference voltage can be obtained. A simulation result of the whole circuit including the output of the comparator is shown in Fig.9.

4. Conclusions

We have presented an interconnect scheme between the stacked chips based on resonant coupling. The performance, 1Gb/s/channel at 9mW/channel, has been confirmed by SPICE simulation. Phase control of the timing signal, size-reduction of the spiral inductor and less power consumption are future researches for multi-channel implementation.

References

[1] K.Kanda et al., ISSCC Digest of Tech. Papers, pp.186-187, Feb. 2003.
[2] A.B.M.H.Rashid, et al., IEEE Electron Device Letters, Vol.23, No.12, pp.731-733, Dec. 2002.

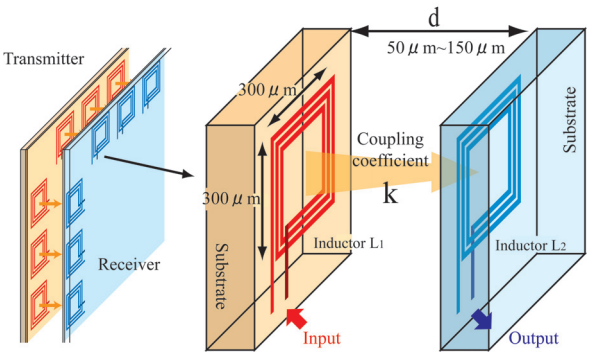

Fig.1 Spiral inductor based wireless interconnect.

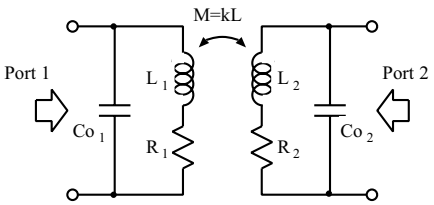

Fig.2 An equivalent model of spiral inductor pair.

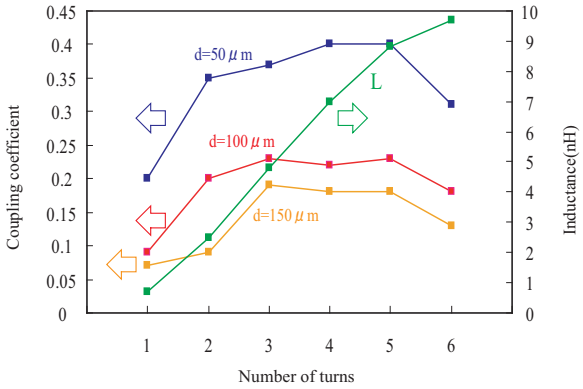

Fig.3 Results of 3D electromagnetic-field simulation.

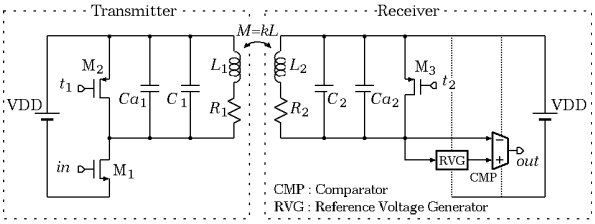

Fig.4 A circuit diagram.

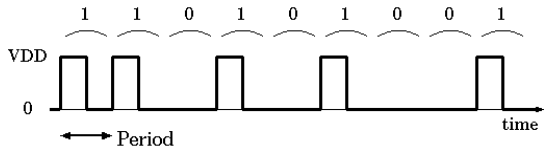

Fig.5 A return zero signal.

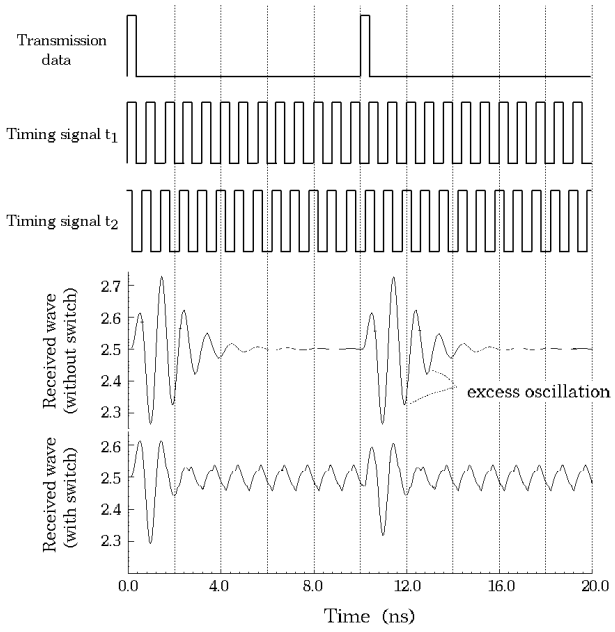

Fig.6 Simulation results.

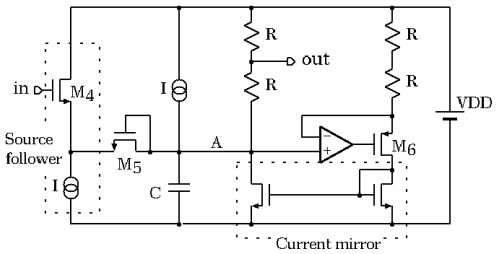

Fig.7 A reference-voltage generator.

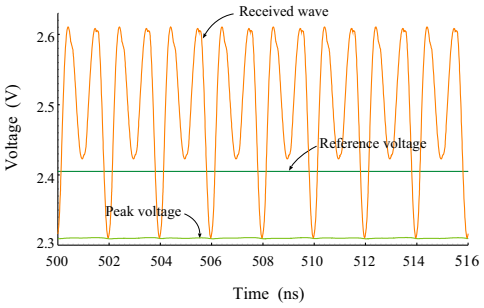

Fig.8 Simulation result of the reference-voltage generator.

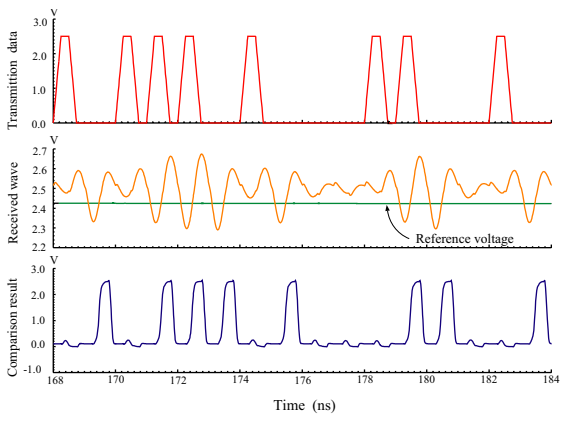

Fig.9 Simulation result of the whole circuit.