# A wireless chip interconnect using resonant coupling between spiral inductors

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- processors
- memories
- analog circuits
- RF interface

→ System LSI

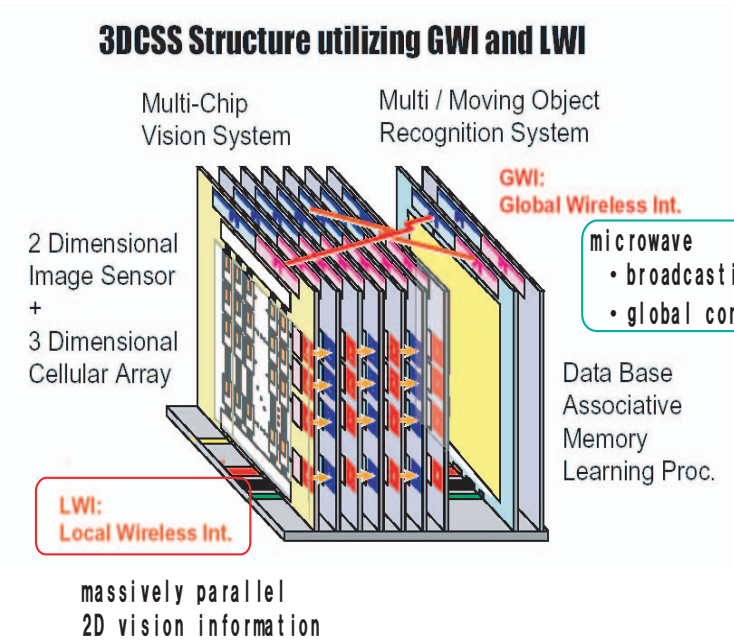
However,
- considerable time to develop
- considerable low yield

System-in-Package

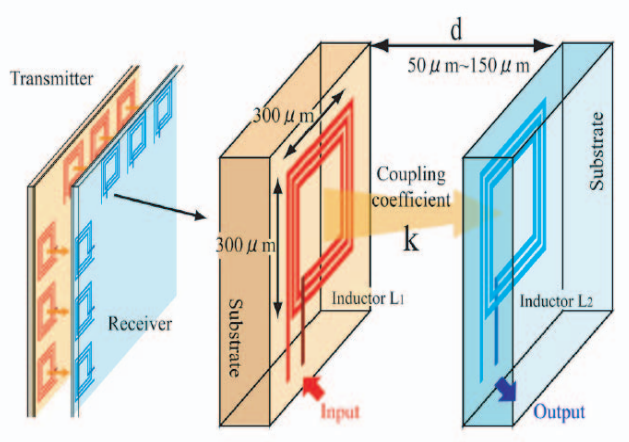
large aspect-ratio vias

Capacitor coupling Wireless interconnect

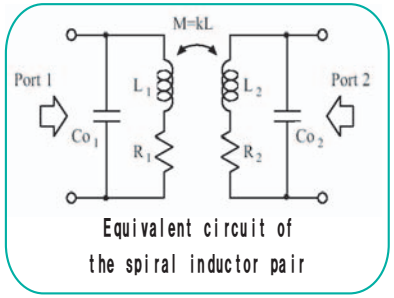
heat dissipation issue




LWI : Local Wireless Interconnect




- spiral inductors
- resonant coupling

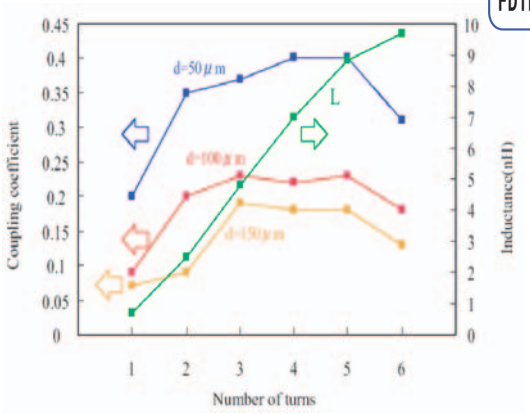


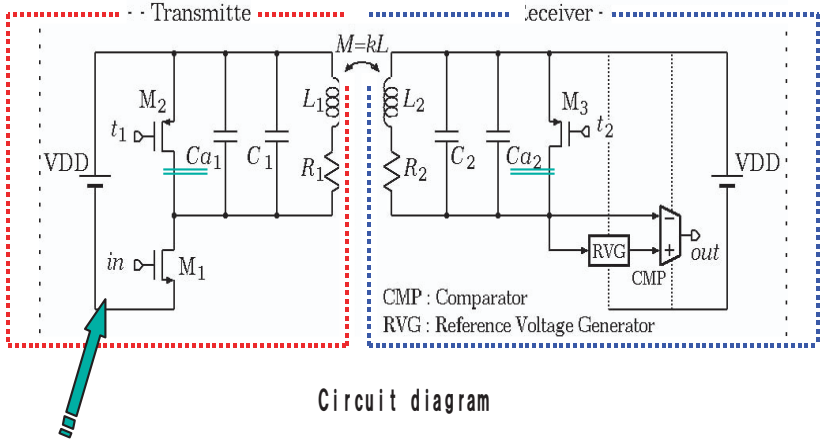

Equivalent circuit of
the spiral inductor pair

L: self-inductance
C: parasitic capacitance
R: loss resistance
M: mutual inductance
K: coupling coefficient

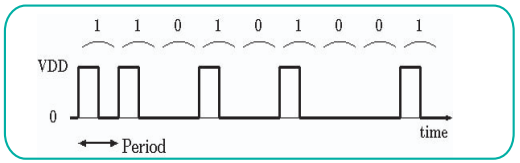
2-port S-parameter
FDTD 3D electromagnetic analysis

data-fitting




Circuit diagram




return zero signal

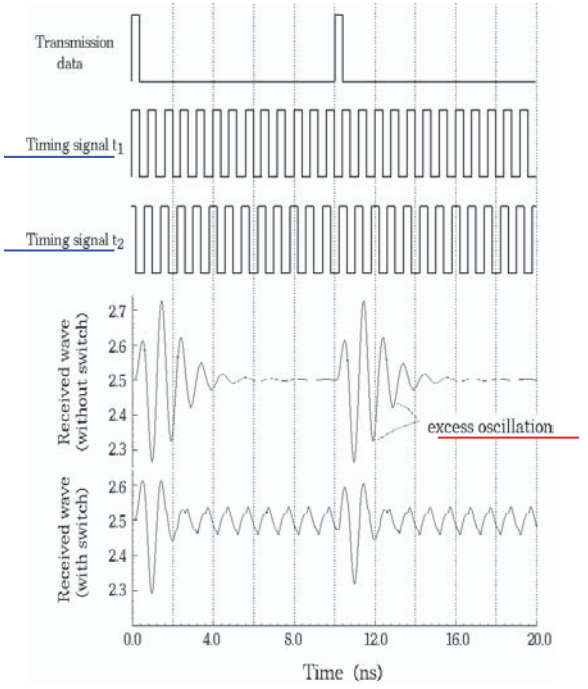
Resonant frequencies
in both transmitter and receiver

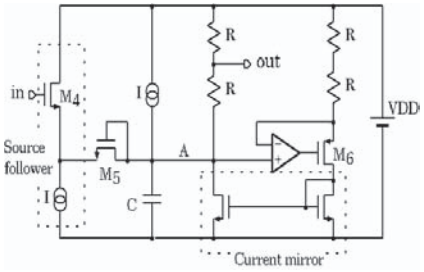
By connecting $Ca_1$ and $Ca_2$

Transmission frequency
of the return zero signal

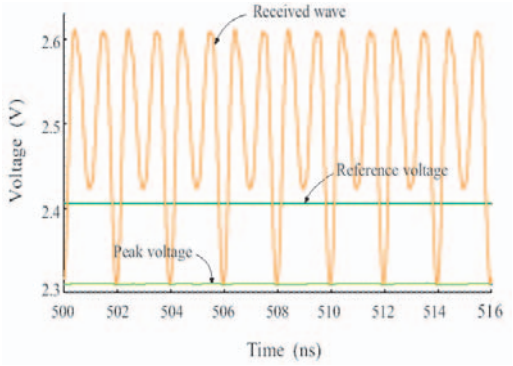
Resonance property enlarges received signal

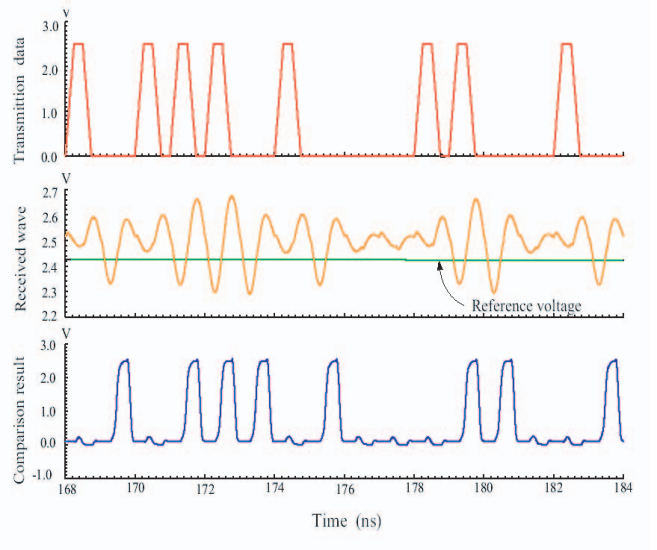
However, · · ·






Reference-voltage generator




Simulation result of the whole circuit

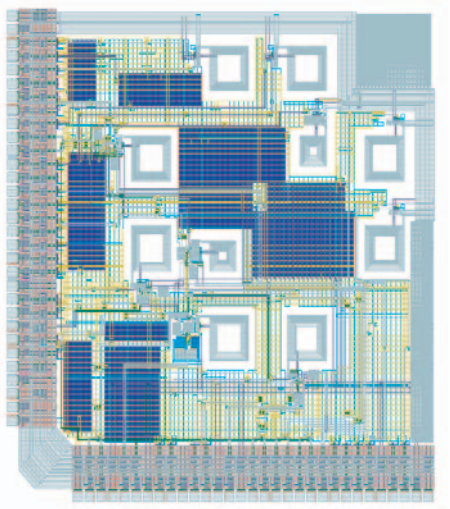
TSMC 0.25 μm mixed CMOS technology

Options: Thick top metal
MiM capacitor

Supply voltage VDD : 2.5V

1Gb/s/channel at 9mW/channel

Transmitter:6mW/channel
Receiver :3mW/channel



Chip layout

## Conclusions

- Interconnect scheme between the stacked chips based on resonant coupling
- 1Gb/s/channel at 9mW/channel from SPICE simulation

Future researches for multi-channel implementation

- phase control of the timing signal
- size-reduction of the spiral inductor
- less power consumption