# Low-Power Digital Image Segmentation of Real-Time VGA-Size Motion Pictures

Hiroshima University
Research Center for Nanodevices and Systems (RCNS)
System Design and Architecture Research Division

T. Morimoto, Y. Harada, O. Kiriyama, H. Adachi, T. Koide, and H. J. Mattausch

## Introduction


(1) Important information must be extracted from natural complex images
(2) Low-power, compact and real-time processing are indispensable

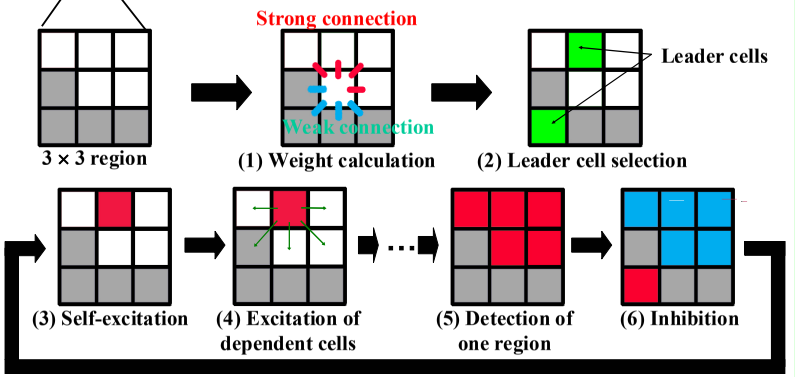
**(1)Image-Segmentation Purpose**
- Partitioning of natural images into meaningful regions
- Initial task for enabling higher-level image processing

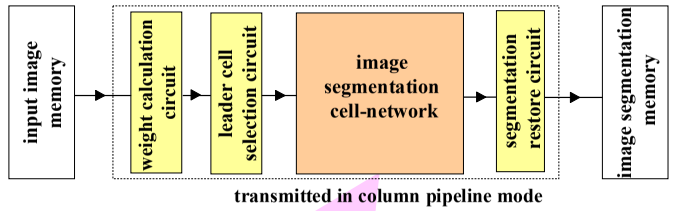
**(2) Necessary Hardware-Implementation Features**
- Low-power-dissipation circuitry for mobile applications
- Pixel-parallel processing for real-time segmentation of motion pictures



## Outline of Digital Segmentation Algorithm

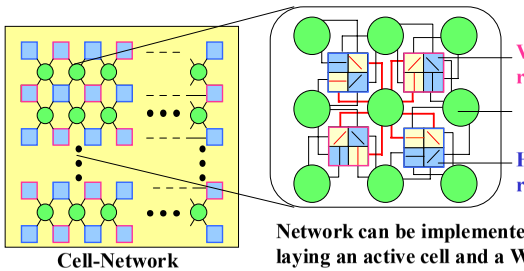
1. **Weight calculation:** Difference of luminance between pixels
2. **Leader cell selection:** Sum of weights with neighboring pixels has to be larger than a threshold
3. **Segmentation:** Repeat self-excitation, excitation, and inhibition



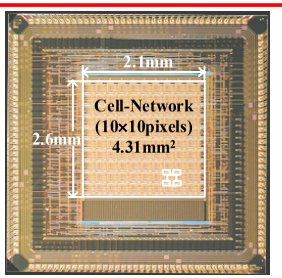

**Cell :** Consists of registers and adders/subtractors
Changes its state $x_k \in \{1,0\}$ depending on $\sum W_{ik} \times x_k$ of 8 neighbors

**Weight-register block (WRB) :** Two register-block types (horizontal/vertical)
Store the 4 connection-weights between the adjacent active cells
Output weights $W_{ik} \times x_k$ to adjacent active cells



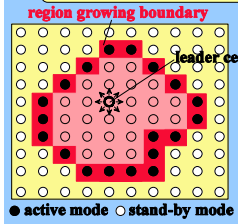

Network can be implemented by alternately laying an active cell and a WRB

- Area minimization with effective sharing of WRBs among neighboring cells
- High speed execution by pixel-based fully parallel processing



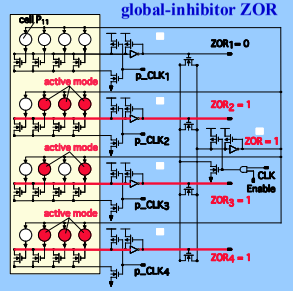

| | |
|---|---|
| Technology | 0.35μm 2-Poly 3-Metal CMOS |
| Measured Max Frequency | 25MHz |
| Power Dissipation (3.3V) | 24.4mW@10MHz (ave.) |
| | 36.4mW@10MHz (worst) |
| Segmentation Time | 9.5μsec (worst) |
| Transistors | 249,810 |
| Pixel Integration Density | 19.6pixel/mm² |

## Boundary-Active-Only Scheme (BAO)

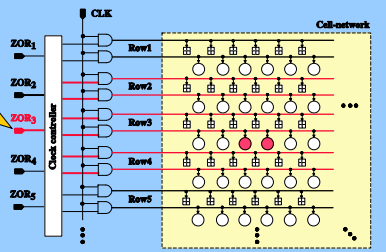



- State-transition evaluation is only necessary for the grown regions boundary cells (Only boundary cells are in active mode and other cells are in stand-by mode)
- More than 75% power reduction is achieved for the 10×10 pixel cell-network

| | Without BAO | With BAO | Reduction |
|---|---|---|---|
| Average | 24.4mW | 5.80mW | 76.2% |
| Worst | 30.9mW | 6.81mW | 78.0% |




- Calculates an OR function of the active-mode-status signals of all cells
- If there are cells in active mode, this circuit outputs a "1" ($ZOR_i = 1$)
- The region-growing boundary is partly determined by $ZOR_i$ for each row

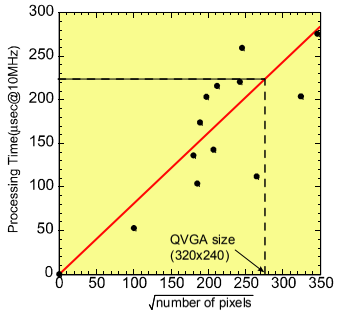


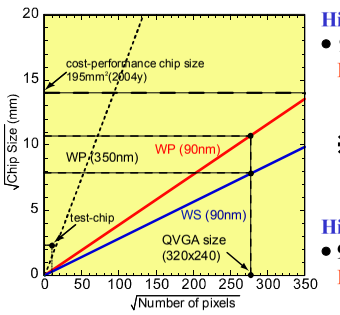

There are state transitions in row 3. During the next clock-cycle, rows 2, 3, 4 have possibilities that state transition cells exist !

**Clock control for each row :**
- Only region-growing boundary rows are activated by gated clock signal
- The activated rows are determined from the $ZOR_i$ signals

## Chip-size estimation

( Estimated from full-custom layout with 3 metal layers 350nm CMOS technology )



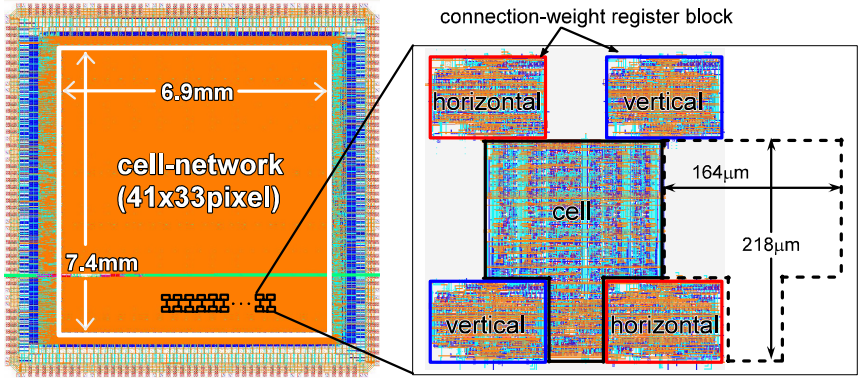

**High-Speed Architecture (Weight Parallel, WP)**
- 90nm CMOS with 5 routing layers

For 320 × 240 (QVGA) image
- Processing Time: < 250μsec at 10MHz
- Chip-size: < 116mm² (11mm×11mm)

※Typical chip-size for cost-performance market in 2004 is expected at 195mm² from ITRS2002 Update

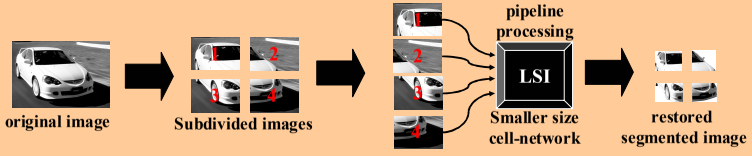
**High-Density Architecture (Weight Serial, WS)**
- 90nm CMOS with 5 routing layers

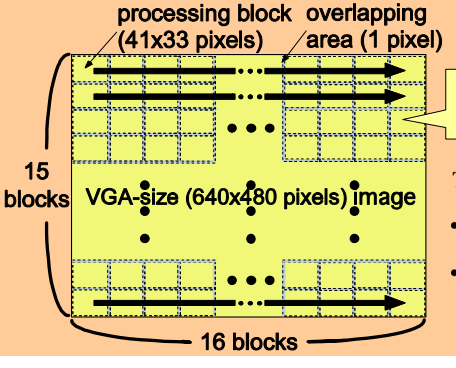
For 320 × 240 (QVGA) image
- Chip-size: < 62mm² (8mm×8mm)




## Subdivided-Image Approach (SIA)

**Segmentation time of the proposed segmentation architecture is much faster than required, so sequential processing becomes possible**




**A 41×33 cell-network**

pixel block
- Estimated segmentaion time : 23μsec
- Estimated power dissipation : 28.0mW

**Total processing time : 7.49msec**
- Segmentation : (16×15) blocks × 23μsec = 5.52msec
- Data in/out : (16×15) blocks × 0.1μsec × 82cycles = 1.97msec (at 10MHz clock frequency)