

CONTENTS

PLENARY SESSION 9:00 – 15:20

Reception Hall, Faculty Club

- 9:00 **Welcome Remarks**
- 9:20 **Opening Address**
Taizo Muta, President, Hiroshima University
- 9:40 **Recent Progress of the COE** 2
Atsushi Iwata, COE Leader, Graduate School of Advanced Sciences of Matter, Hiroshima University
- 10:00 **[Invited] Characterization and optimization of Cu-Low k for 45nm and beyond** 6
Karen Maex, IMEC, Katholik University, Leuven, Belgium
- 10:40 **[Invited] Design with On-Chip Interconnect Inductance** 8
S. Simon Wong, Stanford University, CA, USA
- 11:20 **[Invited] Recent Advances of Diagnoses and Therapeutics in Practical Medicine**..... 10
Nobuoki Kohno, Graduate School of Biomedical Sciences, Hiroshima University

12:00 – 13:30 Lunch Break

- 13:30 **[Invited] Advanced RF/Baseband Interconnects for Future ULSI Communications**..... 14
Mau-Chung Frank Chang, University of California, Los Angeles, CA, USA
- 14:10 **[Invited] Wireless Communications Using Integrated Antennas** 16
Kenneth K O, University of Florida, FL, USA
- 14:50 **ULSI Wireless Interconnection using Integrated Antennas for UWB Signal Transmission** 18
Takamaro Kikkawa, Research Center for Nanodevices and Systems, Hiroshima University

POSTER SESSION 15:30 – 17:00

Lounge, Faculty Club

- P-01 Three Dimensional Integration Architecture for Tera-bit Information processing** 24
A. Iwata, M. Sasaki, T. Yoshida, S. Kameda, H. Ando, M. Shiozaki, M. Ono and K. Sasaki
- P-02 A Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors** 26
Mamoru Sasaki, Daishuke Arizono and Atsushi Iwata
- P-03 A Low-Noise Circuit Technique for Sensing the Nerve Signals** 28
T. Yoshida, T. Mashimo, A. Iwata, M. Yoshida and K. Uematsu
- P-04 A Brain-type Multi-chip Vision System with a PWM-based Line Parallel Interconnection** 30
Seiji Kameda, Masaki Odahara and Atsushi Iwata
- P-05 A Prototype Software System for Multi-object Recognition and its FPGA Implementation** 32

	H. Ando, N. Fuchigami, M. Sasaki and A. Iwata	
P-06	A 2.7Gcps and 7-multiplexing CDMA Serial Communication Chip for Real-time Robot Control ...	34
	Mitsuru Shiozaki, Toru Mukai, Masahiro Ono, Mamoru Sasaki and Atsushi Iwata	
P-07	A Module based Robust Learning System to Environmental Change for Robot Brain	36
	Masahiro Ono, Mamoru Sasaki and Atsushi Iwata	
P-08	A Stereoscopic System with Integration of Multiple Features	38
	Kan'ya Sasaki, Seiji Kameda, Hiroshi Ando, Mamoru Sasaki and Atsushi Iwata	
P-09	Associative Memory-Based Systems with Recognition and Learning Capability	40
	H. J. Mattausch, T. Koide	
P-10	Real-Time Character Recognition System Using Associative Memory Based Hardware	42
	A. Ahmadi, Y. Shirakawa, M. A. Abedin, K. Takemura, K. Kamimura, H. J. Mattausch, and T. Koide	
P-11	Low-Power Video Segmentation by Pipeline Processing of Tiled Images	44
	T. Morimoto, H. Adachi, O. Kiriya, Z. Zhu, T. Koide, and H. J. Mattausch	
P-12	Efficient Object Tracking Algorithm using Image Segmentation and Pattern Matching	46
	O. Kiriya, T. Morimoto, H. Adachi, Z. Zhu, T. Koide, and H. J. Mattausch	
P-13	Multi-view Face Detection and Recognition using Haar-like Features	48
	Z. Zhu, T. Morimoto, H. Adachi, O. Kiriya, T. Koide, and H. J. Mattausch	
P-14	Unified Data/Instruction Cache with Bank-Based Multi-Port Architecture	50
	K. Johguchi, Z. Zhu, H. J. Mattausch, T. Koide, and T. Hironaka	
P-15	Multi-bank based Switch Architecture with Flexible Scheduled Buffering of Packets	52
	T. Fujii, K. Kobayashi, T. Koide, H. J. Mattausch, and T. Hironaka	
P-16	A Carrier Transit Time Delay-Based Non-Quasi-Static MOSFET Model for Circuit-Simulation	54
	Dondee Navarro, N. Nakayama, Y. Takeda, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi and S. Miyamoto	
P-17	Frequency-Domain-Based Carrier Transport Model for a Lateral p-i-n photodiode	56
	Kohkichi Konno, Osamu Matsushima, Kiyohito Hara, Gaku Suzuki, Dondee Navarro and Mitiko Miura-Mattausch	
P-18	Fully-Depleted SOI-MOSFET Model for Circuit Simulation and its Application to 1/f Noise Analysis	58
	N. Sadachika, Y. Uetsuji, D. Kitamaru, L. Weiss, U. Feldmann, S. Baba, H. J. Mattausch and M. Miura-Mattausch	
P-19	A TH-UWB Transmitter and its Pulse Generation Circuit for Intra/Interchip Wireless Interconnection	60
	Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa	
P-20	Design and Measurement of On-Chip CMOS UWB Receiver	62
	Nobuo Sasaki, Pran Kanai Saha and Takamaro Kikkawa	

P-21	Transmission characteristics of Gaussian monocycle pulse for inter-chip wireless interconnection using integrated antenna	64
	K. Kimoto and T. Kikkawa	
P-22	RF Measurement of Permittivity of Low-k films on Si	66
	K. Isari and T. Kikkawa	
P-23	Photosensitive porous low-k interlayer dielectric film	68
	Shin-Ichiro Kuroki and Takamaro Kikkawa	
P-24	Effect of Hexamethyldisilazane on Moisture Adsorption of Porous Silica Films	70
	Shin-Ichiro Kuroki and Takamaro Kikkawa	
P-25	Single-Metal Tunable-Workfunction Technology with NiSi and Mo Gate Electrode	72
	T. Hosoi, K. Sano, M. Hino, N. Ooishi and K. Shibahara	
P-26	Green laser annealing with metal absorber	74
	K. Shibahara, A. Matsuno, E. Takii, K. Kurobe and T. Eto	
P-27	Low-Resistive and Low Leak Current Ultra-Shallow n+/p Junction Formed by Heat-Assisted Excimer Laser Annealing	76
	Ken-ichi Kurobe, Yoshinori Ishikawa, Takanori Eto, Akira Matsuno, and Kentaro Shibahara	
P-28	Study in 3-D MOS Transistor Formation	78
	Kiyoshi Okuyama, Kei Kobayashi, Shunpei Matsumura, Koji Yoshikawa and Hideo Sunami	
P-29	Novel Doping Profile Evaluation for 3-D MOS Transistor	80
	Kei Kobayashi, Takanori Eto, Kiyoshi Okuyama, Kentaro Shibahara, and Hideo Sunami	
P-30	Characterization of 1.55-μm Infrared Light Propagation in SOI Waveguide	82
	Masato Kawai, Tetsuo Tabei, and Hideo Sunami	
P-31	Characterization of Charged States of Silicon-Based Quantum Dots and Its Application to Floating Gate MOS Memories	84
	S. MIYAZAKI	
P-32	Characterization of Atom Diffusion in Polycrystalline Si/SiGe/Si Stacked Gate	86
	H. Murakami, Y. Moriwaki, M. Fujitake, D. Azuma, S. Higashi and S. Miyazaki	
P-33	Crystallization of Amorphous Si films on Glass Substrate Using Plasma Jet and Its Application to Thin Film Transistor Fabrication	88
	S. Higashi, H. Kaku, T. Okada, H. Taniguchi, H. Murakami and S. Miyazaki	
P-34	Local Electronic Transport through Si Dot with Ge Core as Detected by AFM Conductive Probe	90
	Yudi Darma and Seiichi Miyazaki	
P-35	Fabrication of Multiply-Stacked Structures of Si Quantum-Dots Embedded in SiO₂ by Combination of Low-Pressure CVD with Remote Plasma Treatments	92
	K. Makihara, H. Nakagawa, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki	

P-36	High-Rate Growth of Highly-Crystallized Si Films from VHF Inductively-Coupled Plasma CVD ..	94
	Nihan Kosku and Seiichi Miyazaki	
P-37	Electrical characterization of HfAlO_x/SiON dielectric gate capacitors	96
	Yanli Pei, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki	
P-38	Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on NH₃-nitrided Si(100)	98
	H. Nakagawa, A. Ohta, F. Takeno, S. Nagamachi, H. Murakami, S. Higashi and S. Miyazaki	
P-39	Charging and Discharging Characteristics of Stacked Floating Gates of Silicon Quantum Dots ...	100
	T. Shibaguchi, M. Ikeda, H. Murakami and S. Miyazaki	
P-40	Photo-Induced Electron Charging to Silicon-Quantum-Dot Floating Gate in Metal-Oxide -Semiconductor Memories	102
	T. Nagai, M. Ikeda, H. Murakami, S. Higashi and S. Miyazaki	
P-41	Technology for Optical Interconnection in LSI	104
	Shin Yokoyama, Yuichiro Tanushi, Zhimou Xu, Masato Suzuki, and Keita Wakushima	
P-42	Simulation of Ring Resonator Optical Switches	106
	Yuichiro Tanushi and Shin Yokoyama	
P-43	Effect of annealing on the structural properties of spin-coated Ba_{0.7}Sr_{0.3}TiO₃ films	108
	Zhimou Xu, Yuichiro Tanushi, Masato Suzuki, Keita Wakushima and Shin Yokoyama	
P-44	Effect of H₂ adding and substrate bias to Cu sputtering	110
	Masahiro Ooka and Shin Yokoyama	
P-45	Anomalous Behavior of Interface Traps of Si MOS Capacitors Contaminated with Organic Molecules	112
	Masato Suzuki and Shin Yokoyama	
P-46	Development of nano-size mask for diamond emitter	114
	Tetsuo Tabei, Tomihito Miyazaki, Yoshiki Nishibayashi and Shin Yokoyama	
P-47	Interface Trap Generation on MOSFETs with Thin SiO₂ and Plasma-Nitrided SiO₂ Gate Dielectrics under Static and Dynamic Stresses	116
	Shiyang Zhu, Anri Nakajima, Takuo Ohashi and Hideharu Miyake	
P-48	Room Temperature Operation of an Exclusive-OR Circuit Using a Highly-Doped Si Single-Electron Transistor	118
	Tetsuya Kitade, Kensaku Ohkura and Anri Nakajima	
P-49	Atomic-layer deposition of ultrathin gate dielectrics and Si new functional devices	120
	Anri Nakajima	
P-50	[Invited] Non-Contact Impedance Sensor	122
	Makoto Kaneko, Tomohiro Kawahara and Yukio Hosaka	