Design with On-Chip Interconnect Inductance (Invited)

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Abstract

The detrimental effects of interconnect inductance on signal propagation have been widely discussed. This papers describes innovative design concepts that utilize the interconnect inductance to benefit the design of high-speed circuits. Specific examples are illustrated.

I. Introduction

As the operational frequency of an integrated circuit increases beyond GHz, the inductive impedance associate with an on-chip wire becomes comparable or dominant over the resistive component. This could result in additional signal distortion, propagation delay, and cross-talk noise [1, 2]. Hence, the general belief is that inductance, *L*, is detrimental to interconnect performance, and should be minimized.

Although the extraction of *L* associated with a wire randomly placed in a chip is complicated by many factors [3]. *L* can be controlled if there is a dedicated current return path as in co-planar strip line, or micro-strip line. In such an environment, the wire *L* can actually provide a new design dimension. This paper describes specific examples of applying wire *L* in high-speed circuits.

II. Near Speed-of-Light Propagation of Electrical Signal

As a digital signal propagates down a long wire, the quality of the signal is degraded resulting in excessive delay or inter-symbol interference. To understand the reasons, the power spectral density of a 500 ps digital pulse is compared with the intrinsic frequency characteristics of a minimum-sized wire in Fig. 1. The digital signal is broadband in nature, while the wire characteristic changes dramatically over this frequency band. At lower frequencies, the wire behaves as a distributed *R-C* network. In this regime, signals travel very slowly by diffusion and undergo frequency dispersion. As the frequency increases, *L* begins to dominate over *R*, and the wire behaves more as a *L-C* waveguide. The high-frequency *L-C* regime allows for propagation of an electromagnetic wave; consequently, the peak velocity is the speed-of-light in the dielectric surrounding the wire.

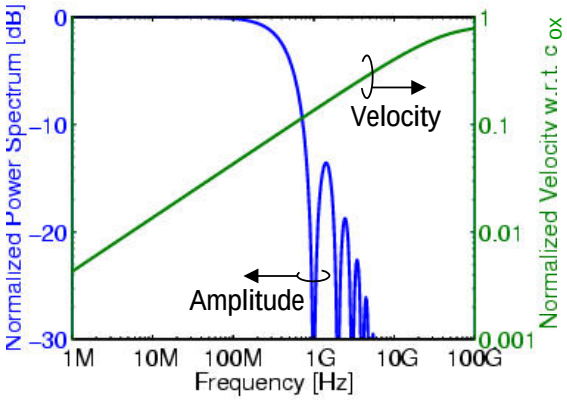

Figure 1 – Spectral power density of a typical digital pulse, and the signal propagation velocity versus frequency along a minimum-sized wire.

Fig. 1 suggests that a high-speed system can be built by taking advantage of the wave nature of wire [4]. Firstly, it is necessary to eliminate the low-frequency portion of the signal that lags behind. This can be achieved by modulating the digital data with a sufficiently high-frequency carrier, and as a result, concentrating all the signal power in the *L-C* regime. Secondly, the crossover frequency between the *R-C* and *L-C* regimes can be shifted into the single GHz range by explicitly emphasizing *L* and reducing R. In this frequency range, simple RF circuits can be designed to transmit and receive these modulated signals. Fig. 2 illustrates the impact of using modulated signaling in combination with an optimized low-loss wire to support high-speed transmission. The signal spectral components now lie predominantly in the high-speed *L-C* regime. This system has been demonstrated in a TSMC 0.18-µm CMOS technology with six levels of Al/Cu wiring and SiO_2 dielectric. The transmitter, receiver, and all other components are integrated on-chip. Fig. 3 shows as-measured input and output waveforms propagating over a distance of 2 cm. Excluding the delay needed for driving signals on and off the chip for testing and measurement., an average delay of 283ps is obtained, which corresponds to an effective signal propagation speed of nearly one-half the speed of light in SiO_2.

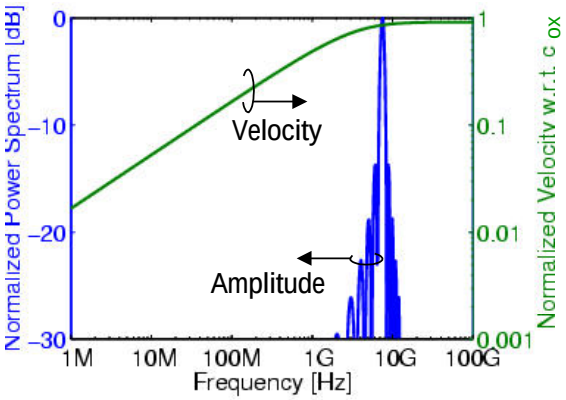

Figure 2 – Spectral power density of a modulated digital pulse, and the signal propagation characteristic of an optimized low-loss wire.

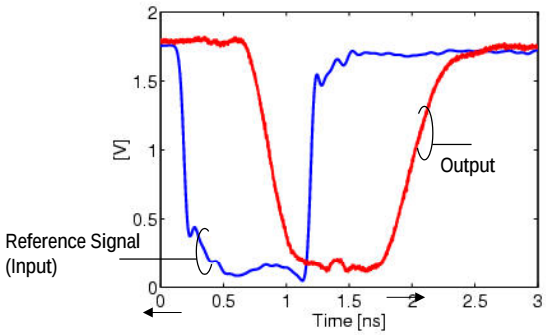

Figure 3 – Measured input and output waveforms of the modulated signal transmission system.

III. 10 GHz Standing Wave Clock

Global clock distribution has become increasingly difficult for multi-GHz microprocessors. Timing uncertainty must reduce with clock period, but skew and jitter for conventional H-trees are proportional to latency, which does not scale with clock period [5].

The global clock network in Fig. 4 distributes a 10 GHz clock through a grid of coupled standing-wave oscillators (SWOs) [6]. The SWO, as shown in Fig. 5, is analogous to a differential L-C oscillator where the gain and tank are distributed. These SWOs are coupled together and sustain synchronous, sinusoidal standing waves across the chip. A single clock source coupled into one SWO injection-locks the entire grid. Clock buffers recover a digital clock and drive the local circuits. This coupled SWO clock network has been prototyped in a TSMC 0.18-µm CMOS technology. The test chip integrates eight coupled SWOs. The grid injection locks to an external clock from 9.8 GHz to 10.5 GHz (6.4% locking range). The clock skew and jitter are measured to be less than 1ps.

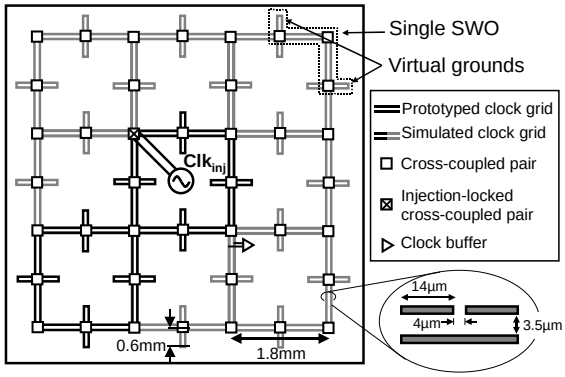

Figure 4 – 10GHz global clock network with coupled standing wave oscillators.

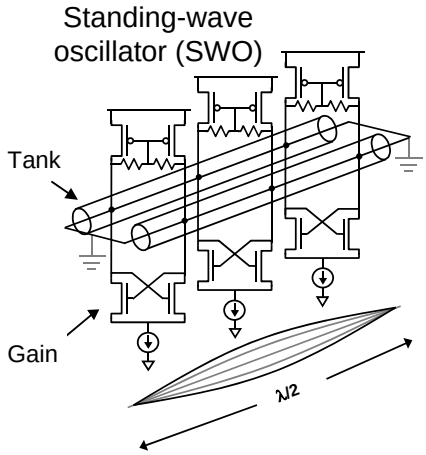

Figure 5 – Schematic of a standing wave oscillator.

5. Conclusions

In high frequency operations, wire inductance is not necessary undesirable, but can be exploited for novel design concepts. Other design examples that exploit the distributive behavior of a wire at high frequencies include a 23 GHz distributed amplifier and a 16 GHz distributed oscillator [7].

Acknowledgments

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References

[1] Restle, et al, IEEE JSSC, Apr 1998.
[2] Deutsch, et al., Proc. IEEE, Apr 2001.
[3] Kim, PhD thesis, Stanford University, 2004.
[4] Chang, et al, Sym VLSI Circuits, June 2002.
[5] Restle, et al, IEEE JSSC, May 2001.
[6] O'Mahony, et al, ISSCC, 2003.
[7] Kleveland, et al, IEEE JSSC, Oct 2001.

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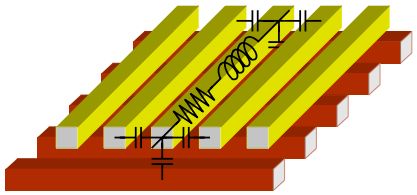
Outline

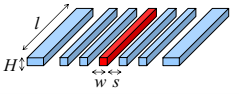
- Detrimental Effects of Interconnect Inductance
- Taking Advantage of Inductance
- Conclusions

Motivation

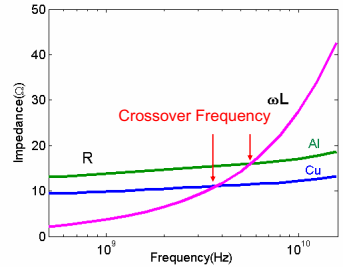


$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC+LG)\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

Line Impedance vs Frequency



$w = 2\mu m, s = 2\mu m, l = 1$ mm



Inductance Screening Example

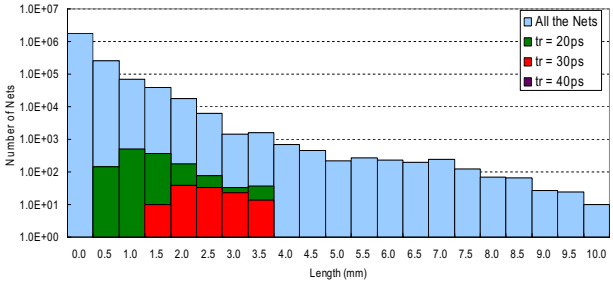
User Input	$t_r = 30ps, \gamma = 0.2$
Screening Criteria	$t_d(RLC) - t_d(RC) > 6ps$
Screening Output	98 nets

Commercial Design

Technology	0.13μm, 8ML
Chip Size (mm × mm)	10.3 × 10.3
No. of Nets	912K
No. of Cells	692K
SPF file size (MB)	808

Inductance Screening Result

$\gamma = 0.2$



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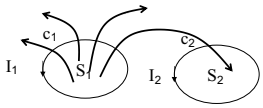
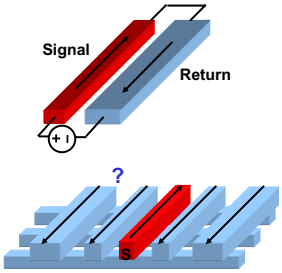
Inductance Definition

Inductance is a property of a **closed current loop**



$$L_{11} = \frac{\Phi_{11}}{I_1} \qquad M_{12} = \frac{\Phi_{12}}{I_1}$$

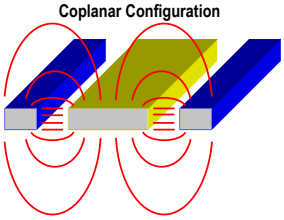
$$\Phi_{11} = \int_{S_1} \vec{B}_1 \cdot d\vec{s}_1 \qquad \Phi_{12} = \int_{S_2} \vec{B}_1 \cdot d\vec{s}_2$$



On-chip environment

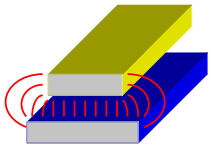
Coplanar versus Microstrip

Coplanar Configuration



- Only Single Metal Level
- Coupling to Substrate/Underlying Wires
- Slow-wave Effects
- Resistance is Independent of Width at High Frequencies

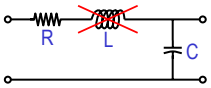
Microstrip Configuration



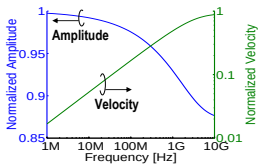
- Multiple Metal Levels
- Shielding from Substrate/Underlying Wires
- Resistance Scales with Width at High Frequencies

Digital Signal over Global Wires

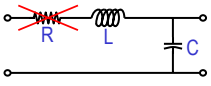
Low Frequencies (R>>ωL).



$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$



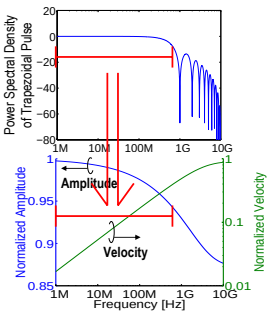
High Frequencies (R<<ωL).



$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$$

Digital Signal over Global Wires

Frequency analysis of digital pulse over interconnect.



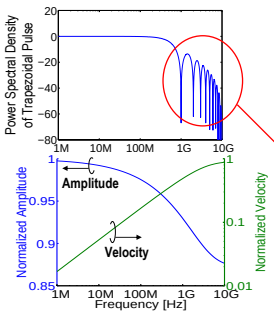
Digital signals are **broadband**.

- Most power of the digital pulse is concentrated in slower, low-frequency regime .

Length of line = 1 mm

Digital Signal over Global Wires

Frequency analysis of digital pulse over interconnect.



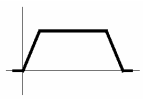
Digital signals are **broadband**.

- Most power of the digital pulse is concentrated in slower, low-frequency regime .
- But, portion of signal that contributes to sharp rise time is in the higher frequency regime.

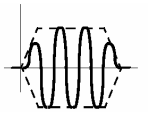
Length of line = 1 mm

Signaling in the LC Regime

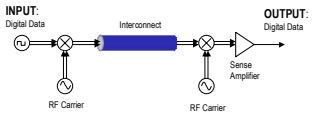
Modulate digital signals with a high-frequency carrier to push signal spectrum into LC-regime.



Normal Digital Pulse.

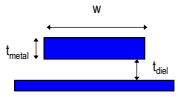


Modulated Digital Pulse.

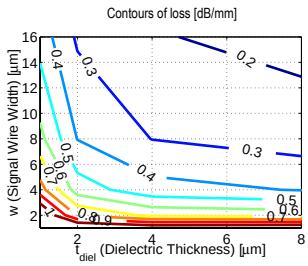


Optimization of Low Loss Wires

Need to minimize loss over interconnect, while using reasonable dimensions.



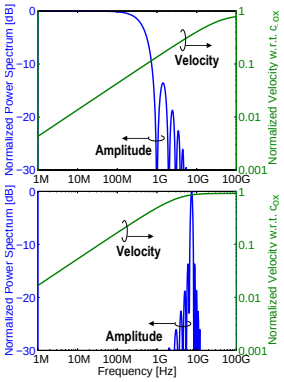
Cross-section:
t_{metal} = 2 µm
frequency = 10 GHz
Composition: Al, SiO_2



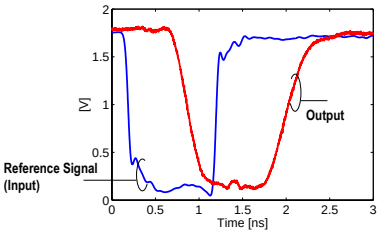
Modulated Signal over Global Wire

Conventional Approach --
Signal power is distributed over slow RC regime.

Modulated Approach --
Signal power is concentrated in fast LC regime with the help of better wires.



Measured Waveforms



20 mm Delay: 283 ps (including modulator and demodulator delays, excluding buffer delay)

1/2 Speed of Light

- Taken with HP54750A digital sub-sampling oscilloscope

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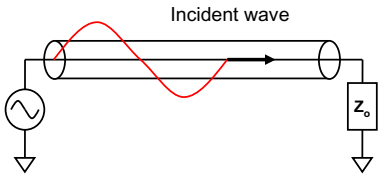
  - 10 GHz Standing Wave Clock
- Conclusions

Travelling Waves



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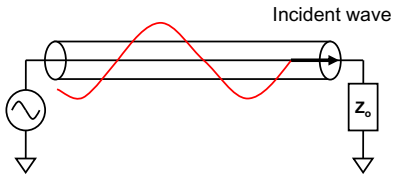

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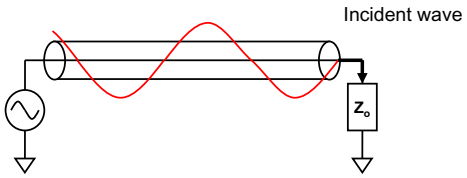
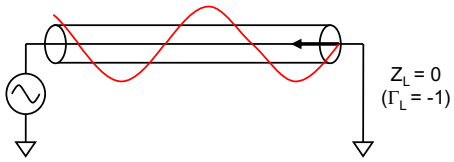
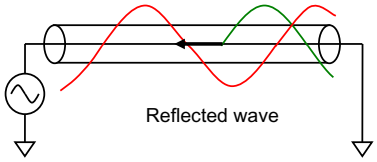


- Wave characteristics
  - Phase varies linearly with position
  - Amplitude is constant with position
- Used in most conventional clock distributions

Standing Waves



Standing Waves



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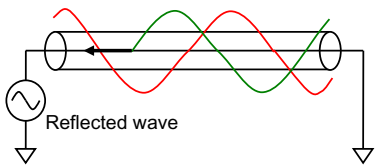
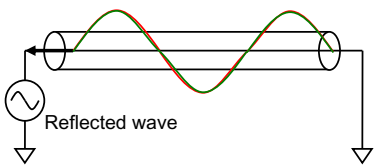
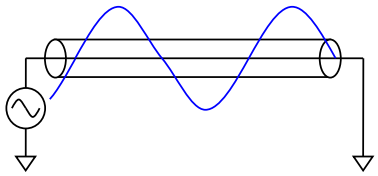


Standing Waves



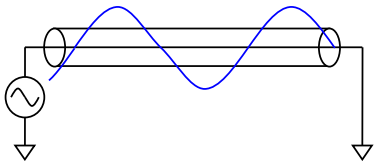
Standing Waves

Standing wave



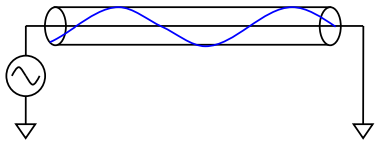
Standing Waves

Standing wave



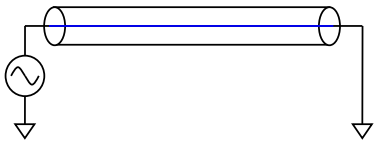
Standing Waves

Standing wave



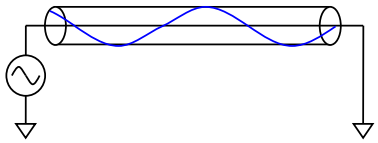
Standing Waves

Standing wave



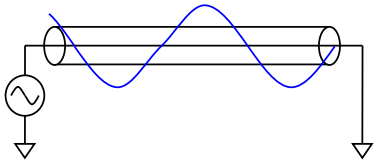
Standing Waves

Standing wave



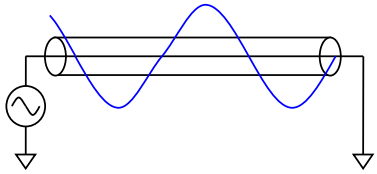
Standing Waves

Standing wave



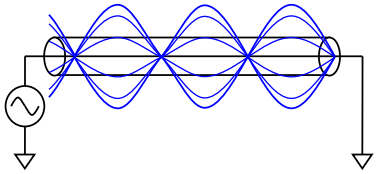
Standing Waves

Standing wave



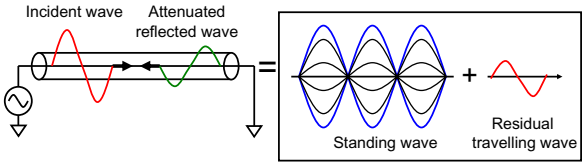
Standing Waves

Standing wave



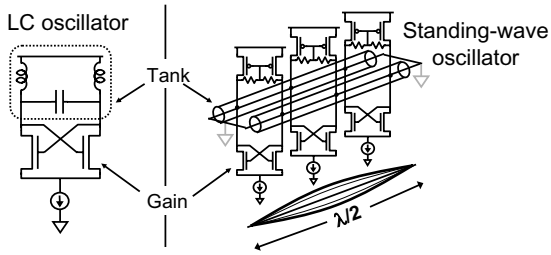
– Wave characteristics
  - Phase is constant with position (with 180º discontinuities)
  - Amplitude varies sinusoidally with position

Standing Waves on Lossy Wires



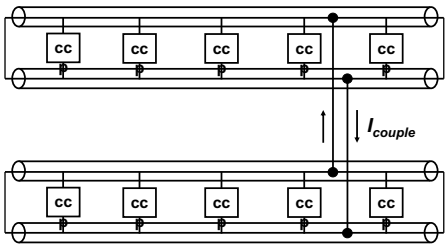
- Wire loss causes skew
- Design using low-loss, inductive wires

Standing-Wave Oscillator (SWO)



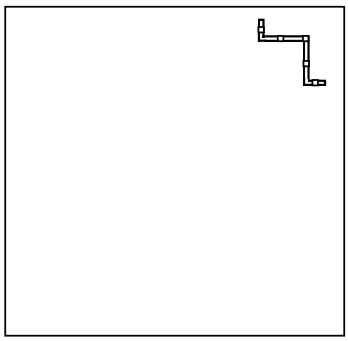
Conditions for oscillation at f_{clk} ⇨ $g_d > \frac{l}{n}\frac{R(C+C_d)}{L}$ and $l = \frac{1}{2f_{clk}\sqrt{L(C+C_d)}}$

SWO Coupling

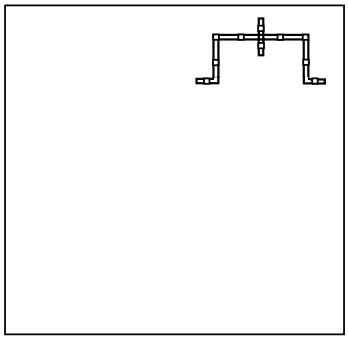


- Couple by directly connecting the wires
- Low-Q oscillators have wide locking range

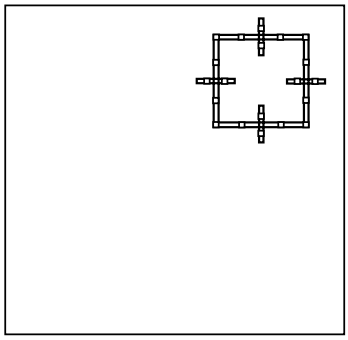
SWO Clock Grid



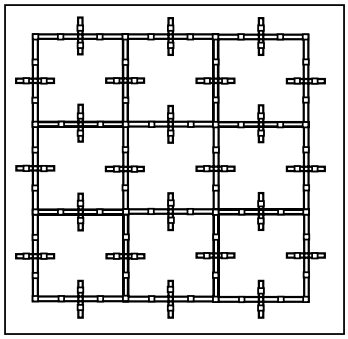
SWO Clock Grid



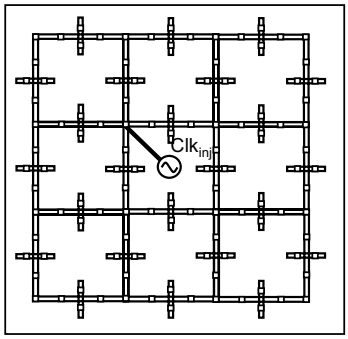
SWO Clock Grid



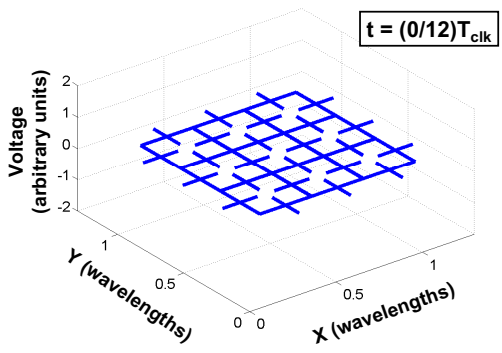
SWO Clock Grid



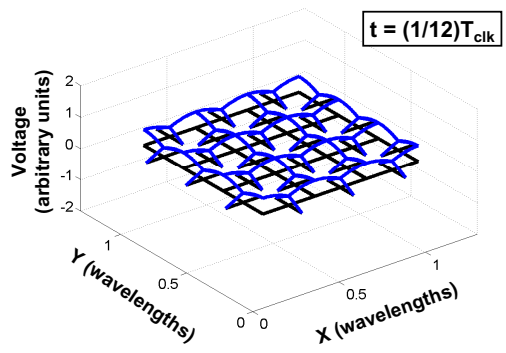
SWO Clock Grid

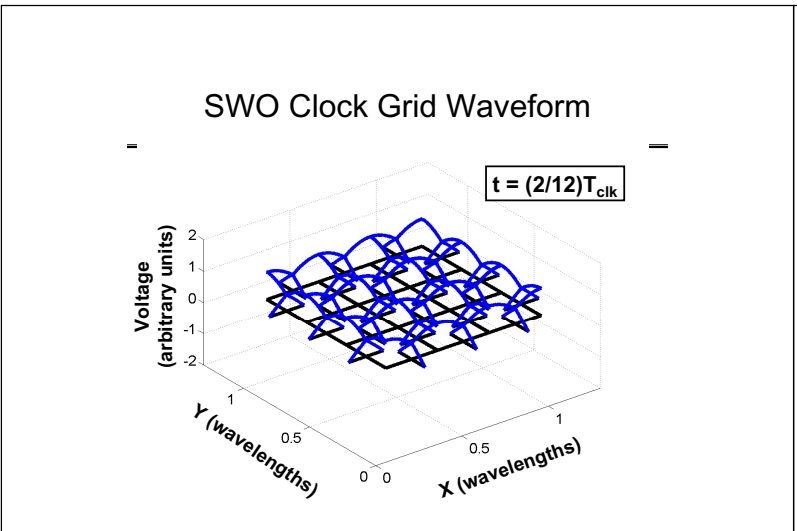


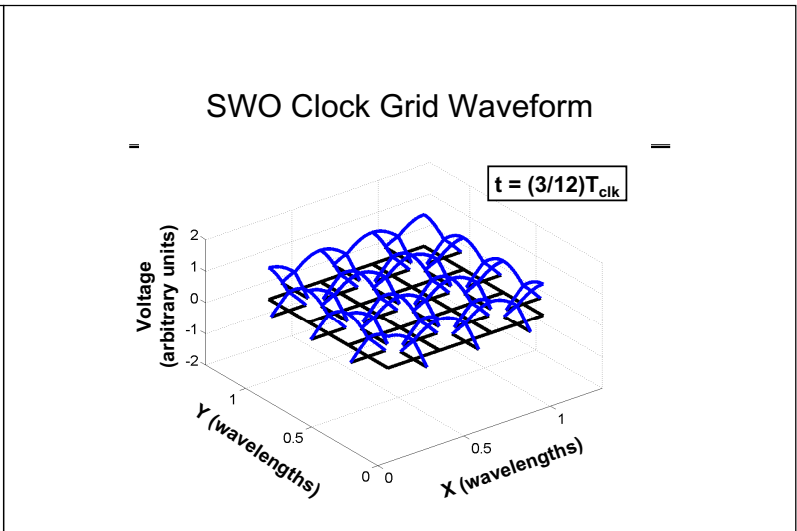
SWO Clock Grid Waveform

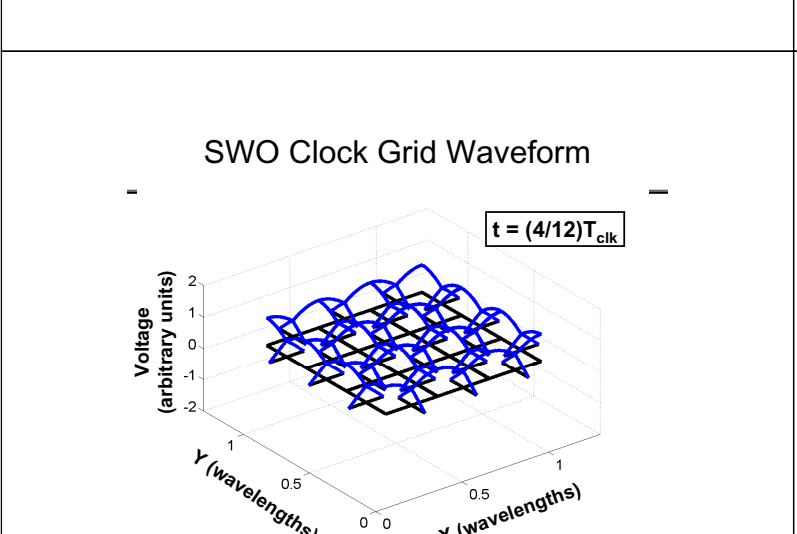


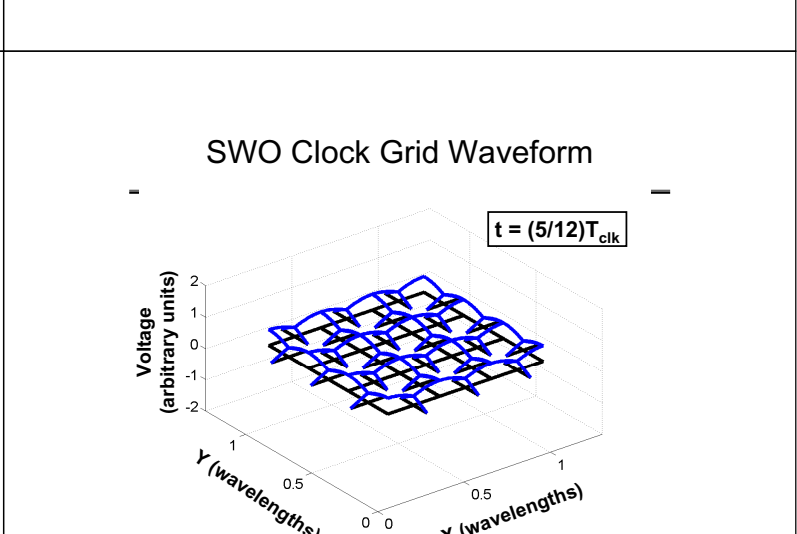
SWO Clock Grid Waveform

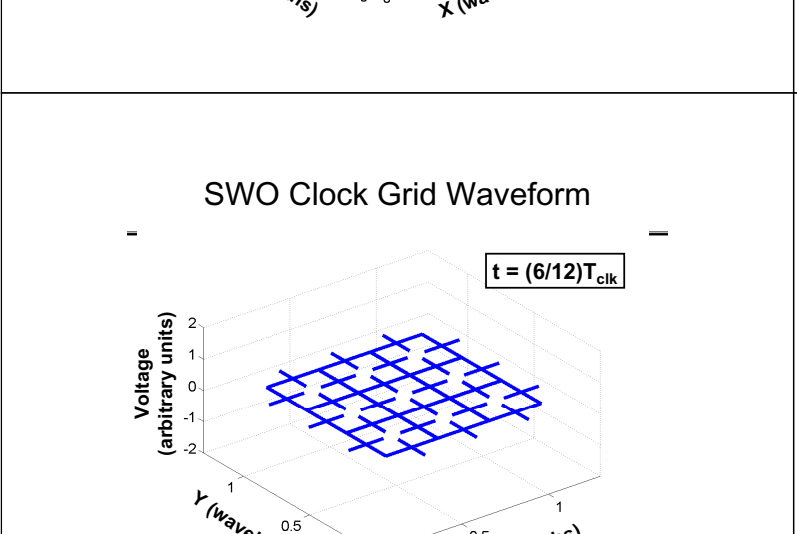


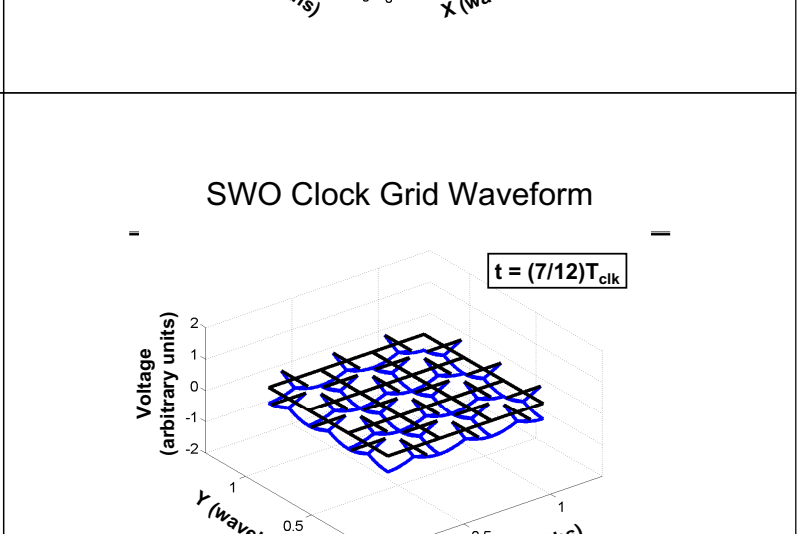

SWO Clock Grid Waveform
t = (2/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)


SWO Clock Grid Waveform
t = (3/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)

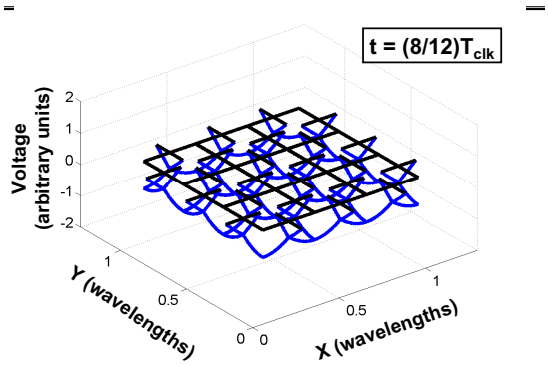

SWO Clock Grid Waveform
t = (4/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)


SWO Clock Grid Waveform
t = (5/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)

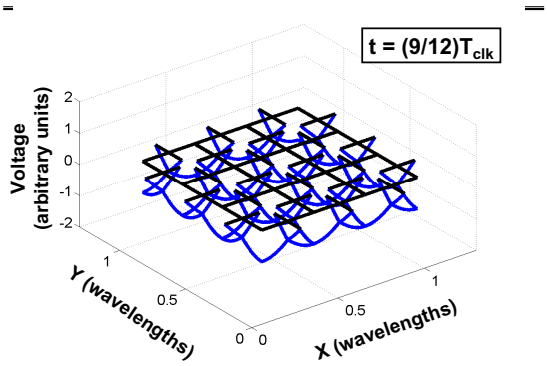

SWO Clock Grid Waveform
t = (6/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)


SWO Clock Grid Waveform
t = (7/12)T_clk
Voltage (arbitrary units)
Y (wavelengths)
X (wavelengths)

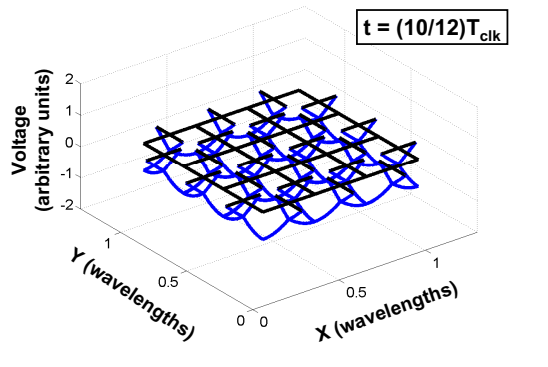
SWO Clock Grid Waveform



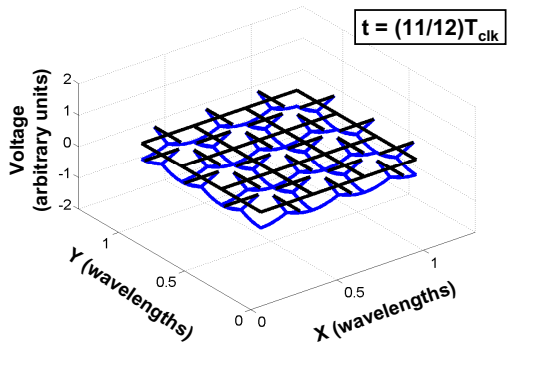
SWO Clock Grid Waveform



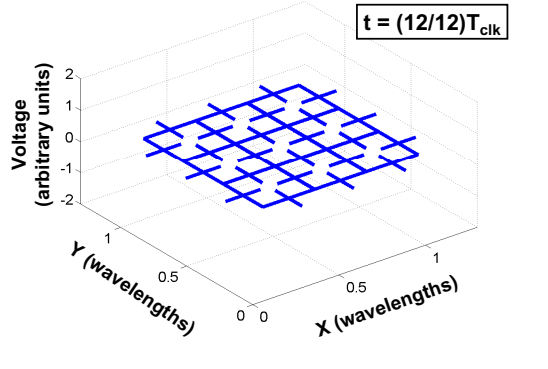
SWO Clock Grid Waveform



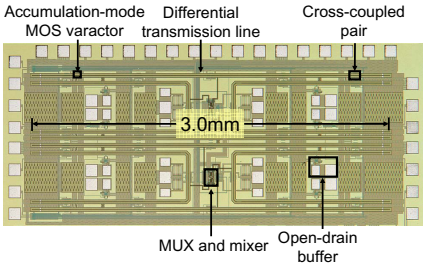
SWO Clock Grid Waveform



SWO Clock Grid Waveform

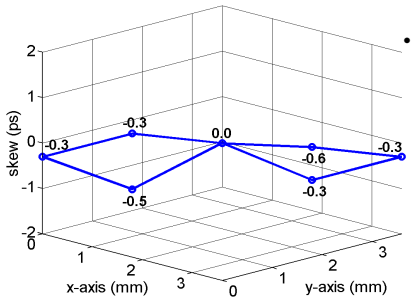


Die Micrograph



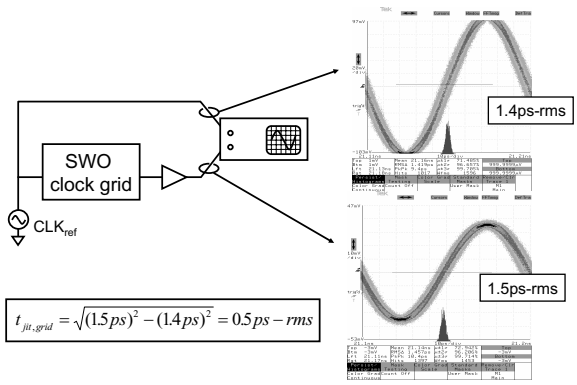
Locking range	9.8 GHz – 10.5 GHz (6.4% range)
Skew	0.6ps
Jitter (added to external source)	<0.5ps rms (1.4ps rms external source)
Power	430mW

Skew Measurements



- Tuned grid
  - 0.6ps global skew

Jitter Measurement

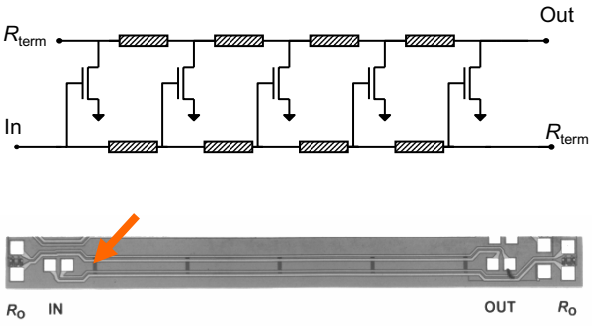


$$t_{jit,grid} = \sqrt{(1.5ps)^2 - (1.4ps)^2} = 0.5ps - rms$$

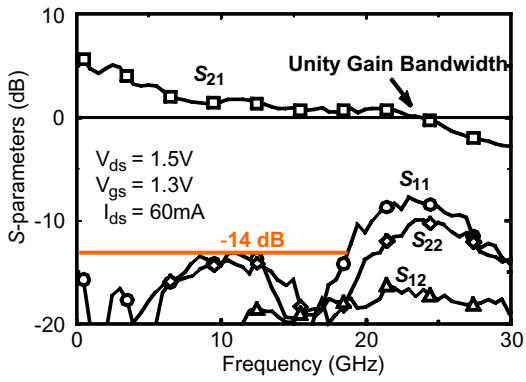
Outline

- Detrimental Effects of Interconnect Inductance
- Taking Advantage of Inductance
  - Near Speed of Light Propagation of Electrical Signal
  - 10 GHz Standing Wave Clock
  - Other Distributed Designs
- Conclusions

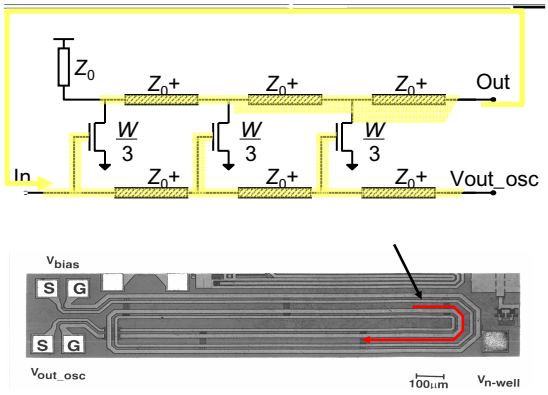
Distributed Amplifier



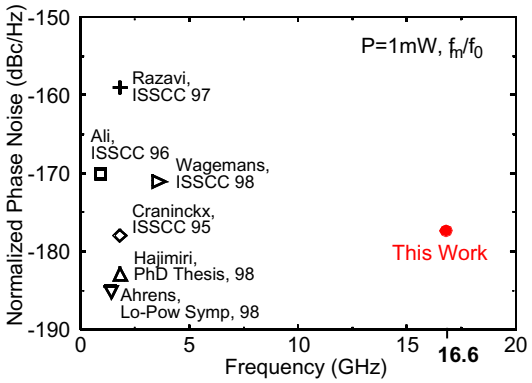
Amplifier *S*-parameters



Distributed Oscillator



Phase Noise Comparison



Conclusions

- At high frequencies, interconnect inductance can no longer be ignored
- Extraction of inductance in a typical IC environment is extremely difficult
- Only a small number of interconnects exhibit inductive behavior
- With dedicated return path, interconnect inductance can be controlled & optimized
- Incorporating inductance into distributed designs offer new opportunities