Advanced RF/Baseband Interconnects for Future ULSI Communications

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Abstract

Future inter- and intra-ULSI interconnect systems demand extremely high data rates as well as bi-directional multi-I/O concurrent service, re-configurable computing/processing architecture, and total compatibility with mainstream silicon SOC (system-on-chip) and SIP (system-in-package) technologies. In this paper, we review recent advances in **CDMA** and **FDMA** interconnect schemes that promise to meet all of the above system requirements. The physical transmission line is no longer limited to a direct-coupled metal wire. Rather, it can be accomplished via either wired or wireless mediums through capacitor couplers that reduce the baseband noise and DC power consumption. These new advances in interconnect schemes would fundamentally alter the paradigm of ULSI data communications and enable the design of next generation computing/processing systems.

Introduction

The system performance of modern ULSI is being limited by its interconnect bandwidth in both on-chip and chip-to-chip communications [1-3]. The rapid evolution of ULSI has demanded that the interconnect system be fast and at the same time be flexible, reliable and low cost. Ideally, future interconnect systems must encompass the following important features:

- Ultra-high data rates (e.g. >100Gbps/pin or 20Tbps aggregate [2], defined as the total sum of data rate for each pin on a chip or within a system of chips)
- Concurrent multi-I/O's service for simultaneous and bi-directional communications on a shared transmission medium
- Realtime re-configurability in connectivity and bandwidth for optimized channel efficiency and fault-tolerance

Additionally, the fabrication of future interconnect systems must be compatible with the mainstream SOC and SIP technologies for low cost system production.

Traditional inter-chip and intra-chip communications are based solely on TDMA (time division multiple access). In a TDMA-interconnect (*TDMA-I*) system, each I/O pair communicates over a shared transmission medium by transmitting only during its scheduled time slot in which no other I/O pair may transmit. In essence, time is being divided or allocated to each individual I/O pair so that a given transmission medium may be effectively shared. Furthermore, advanced *TDMA-I* (bus and links) in recent years has exploited multi-level signaling and dispersive signal equalization techniques to achieve multi-Gbps throughput [4-6]. Nevertheless, this type of system is limited to fixed and non-reconfigurable architecture that has high data transmission latency and cannot support bi-directional and simultaneous transmission of multiple I/Os on the same physical channel.

Advanced Interconnect Schemes

To overcome the limitations of traditional *TDMA-I*, a number of new interconnect schemes have been investigated recently to greatly increase the aggregate data rate and concurrency as well as to reduce latency and power consumption [7-13]. These new schemes permit the use of a combination of other multiple access techniques, namely code division multiple access (CDMA) and frequency division multiple access (FDMA). In CDMA interconnect (*CDMA-I*), each I/O pair is assigned one or more pseudo-noise (PN) codes with near-ideal correlation property so that any other I/O pair assigned with different PN codes will contribute no interference when they are transmitting concurrently onto the same medium. In contrast, *FDMA-I* allows sharing of a transmission medium by assigning I/O's to different frequency channels. I/O's assigned with different frequency channels may communicate concurrently with virtually no interference, provided that undesired frequency channels for a given I/O are filtered out properly. *FDMA-I* and *CDMA-I* may be combined into a *multi-carrier CDMA-I*, whereby concurrent I/O transmissions are accomplished by properly assigning codes and frequencies to each I/O pair.

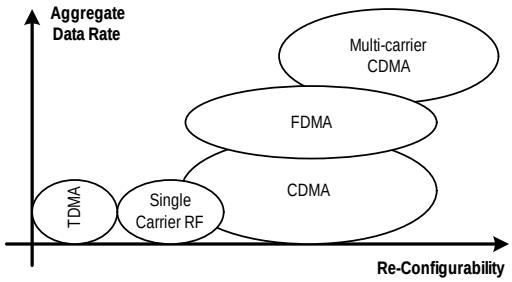

Fig. 1 Comparison of Interconnect Schemes

Figure 1 compares new schemes based on *CDMA-I* and *FDMA-I* against the traditional *TDMA-I* in terms of two critical features for interconnects used in future ULSI systems: namely, aggregate data rate and re-configurability. Interconnect systems based on the *multi-carrier CDMA-I* achieve the highest aggregate data rate and re-configurability. The high aggregate data rate is a result of the increased bandwidth made available through the use of more than one frequency channel. The high re-configurability arises from the increased number of combined code and frequency channels (or N_c and N_f , which denote respectively the number of code channels and the number of frequency channels) now available to the system to dynamically assign based on the specific operation requirement. Note that both *FDMA-I* and *CDMA-I* have similar degrees of re-configurability but *FDMA-I* has higher aggregate data rates than *CDMA-I* due to the additional bandwidth made available through multiple frequency channels. In theory, *TDMA-I* has the same degree of re-configurability as either *FDMA-I* or *CDMA-I* in that a *TDMA-I* scheme can re-configure based on rescheduling and reassigning time slots for a given set of I/O's depending on the operation needs. In principle, the number of time slot N_t can be made equal to N_c or N_f . However, even though an increase in N_t results in proportional reduction in the average data rate per I/O pin, the burst data rate for each I/O pin still remains the same as the aggregate data rate. The high I/O bust data rate makes implementation difficult due to the need for high-order modulation and time-domain equalizers at high operating speed. For *CDMA-I* and *FDMA-I*, on the other hand, the burst data rate per I/O is inversely proportional to N_c and N_f , which simplifies the signal processing required for each I/O. In particular, for *CDMA-I*, Rake receiver architecture may be employed to compensate for time dispersion in the transmission media but it requires much less complexity than a time-domain equalizer [14]. To put this into the perspective of practical implementation, wired *TDMA-I* has limited re-configurability due to difficulty in increasing N_t without excessive complexity and power dissipation in the transceiver system design.

The re-configurability of wired *TDMA-I* may be improved with the single-carrier RF-interconnect scheme (or *SCRFI*) shown in Fig 1. The *SCRFI* uses only one frequency channel and achieves similar throughput as a wired *TDMA-I* system. However, it is able to achieve higher re-configurability than *TDMA-I*, since the transmission medium is no longer limited to fixed wiring but rather may be wirelessly broadcasted through coupling capacitors to communicate with different receivers. Such a scheme not only simplifies the fabrication process by eliminating the vertical metal studs needed in future 3D IC but also reduces the noise and DC power consumption. Transmission through capacitor-coupling can also be applied to *FDMA-I*, *CDMA-I*, and *Multi-Carrier CDMA-I* (or *MCCDMA-I*) as well.

Conclusion

In this paper, we will review recent progress in each of the new interconnect schemes described in Fig. 1 and discuss their applications in future ULSI interconnect implementations and architecture designs of next generation computer/processor systems. We will first describe a wired *CDMA-I* that achieves channel re-configurability while providing simultaneous multi-I/O's services. We will then discuss the wired *FDMA-I* that is able to achieve multi-band (or multi-mode) channel communications. Subsequently, *SC-RFI* specifically designed for 3D IC will be presented. Finally, wireless inter-chip communication based on *MCCDMA-I* will be discussed along with other system applications such as CDMA dynamic random access memory (*CDMA-DRAM*) and re-configurable interconnect for next generation systems (*RINGS*).

References

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Outline

- **Future Interconnect System Requirements**
- **Issues of Traditional *TDMA-Interconnect***
- **Advanced Interconnects**
  - *CDMA-Interconnect*
  - *FDMA-Interconnect*
  - *FDMA/CDMA-Interconnect*
- **New Interconnects System Applications**
- **Comparison of Interconnects**
- **Summary**

Future Interconnect System Requirements

- *Ultra-high data rates (>100Gbps/pin or 20Tbps aggregate, defined as total sum of data rate for each pin or within a system of chips) and low latency*
- *Concurrent multi-I/O's service for simultaneous/bi-directional communications on a shared transmission medium*
- *Realtime reconfigurability in connectivity and bandwidth for optimized channel efficiency and fault-tolerance*
- *Compatible with mainstream SOC and SIP technologies for low cost system insertion*

Issues of Traditional TDMA Interconnect (*TDMA-I*)

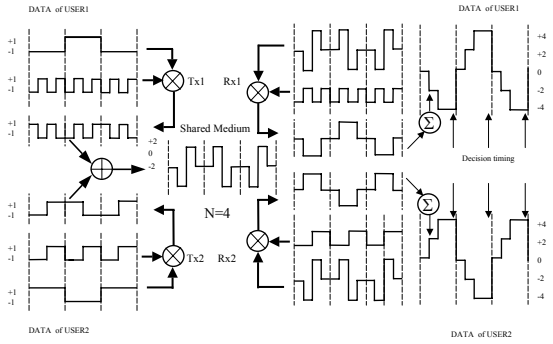
- Space/Time multiplexing only, does not offer concurrent and bi-directional communications for distributed multi-I/Os
- High I/O burst data rate (equals aggregate data rate) demands high-order modulation and time-domain equalization
- Limited reconfigurability because rescheduling or reassigning N_t (number of time slots) inevitably increases the complexity and power consumption of transceiver system
- Difficult to re-allocate bandwidth to each I/O pair in realtime
- Switched by hardware, cannot take full advantage of packet switching
- Poor security, source-destination pairs physically identifiable on wafer
- Large number of I/Os, inefficient use of wafer real estate due to bonding, soldering and packaging constraints
- Inadequate line shielding, vulnerable to noise and interference
- Low dynamic testability for "known-good-die"

Advanced Interconnect Schemes

- *CDMA-I*
  - Code divided channels (N_c) based on direct sequence spread spectrum (DSSS)
  - Flexible in reconfiguration by software code assignment
- *FDMA-I*
  - Frequency divided channels (N_f)
  - Data rate for individual channel proportional to its bandwidth allocation
- *Combined FDMA/CDMA-I (Multi-Carrier CDMA-I)*
  - FDMA/CDMA combined multiple access
  - Reduced burst rate per channel leads to low transceiver complexity and low power consumption
  - Synchronous access can be realized by using orthogonal codes to eliminate the cross channel interference

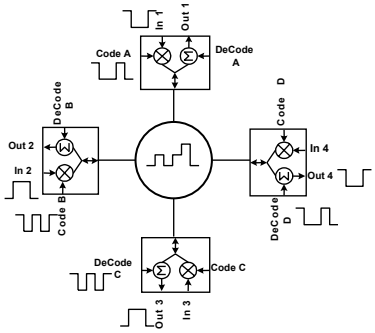
CDMA-Interconnect (*CDMA-I*)

CDMA Based on DSSS

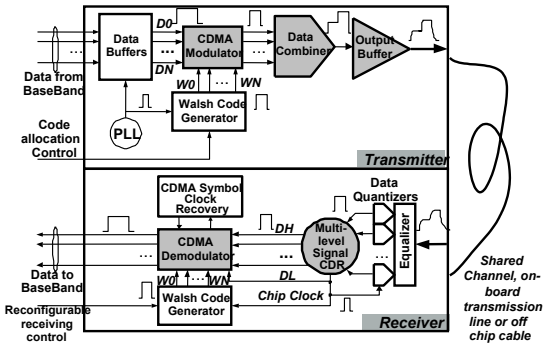


CDMA Interconnect System

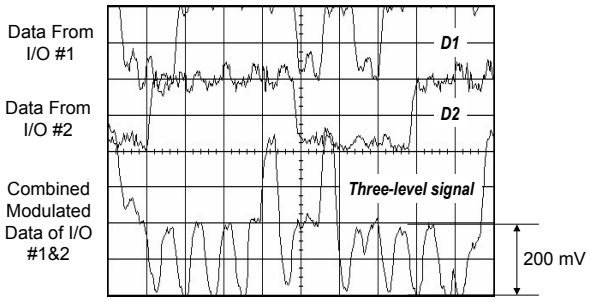
- Allows re-configurability of both connectivity and bandwidth in realtime
- Detects data sequence of different users via firmware coding without hardware retiming/framing
- Enables packet switching in hardware level
- Realizes multi-I/O, multi add/drop and parallel communications with relaxed timing constraints



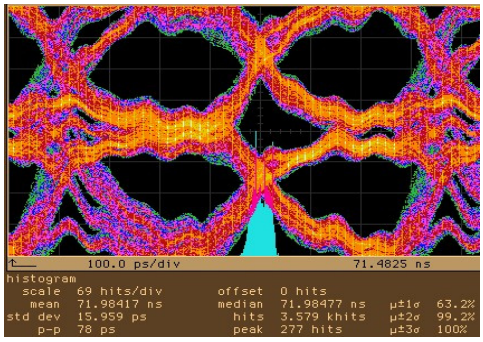
CDMA Transmitter and Receiver



CDMA-I Transceiver Data Waveforms



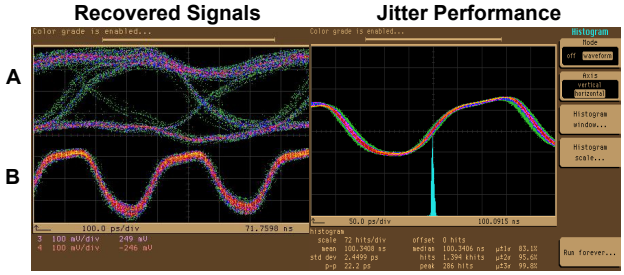
CDMA-I Data Eye Diagram



2.7Gb/s/pin achieved over 2m cable

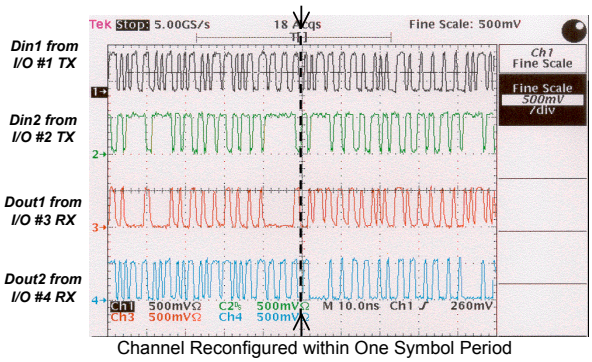
Multi-level CDR Output

Recovered Signals **Jitter Performance**



(A) Data Sequence (B) Clock

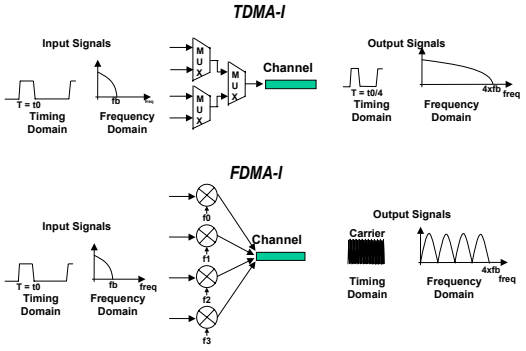
Realtime Channel Re-configuration



Channel Reconfigured within One Symbol Period

FDMA-Interconnect (*FDMA-I*)

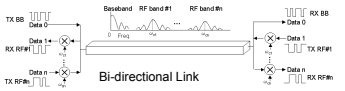
FDMA versus TDMA

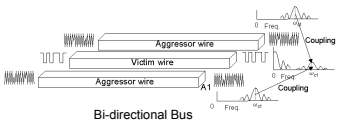


Bi-Directional *FDMA-Link/Bus*

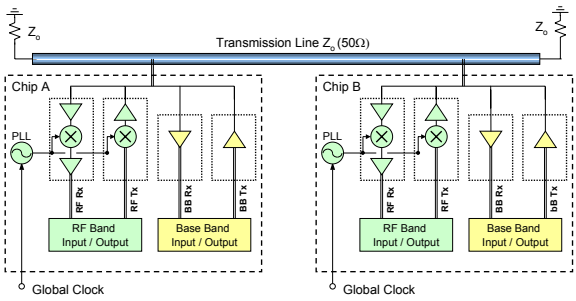
Advantages:

- Higher combined data rate
- Simultaneous, bi-directional communications
- Re-configurable between bands
- Low in-band coupling for parallel bus
- Potentially with fewer I/O pins and smaller routing area

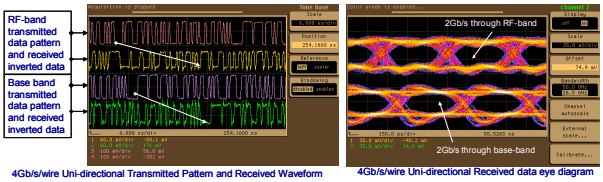




FDMA-Interconnect System

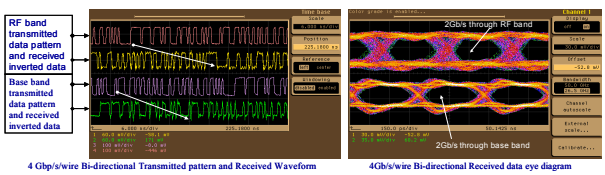


FDMA-I I/O Data Eye Diagram



4Gb/s/wire Uni-directional Transmitted Pattern and Received Waveform

4Gb/s/wire Uni-directional Received data eye diagram

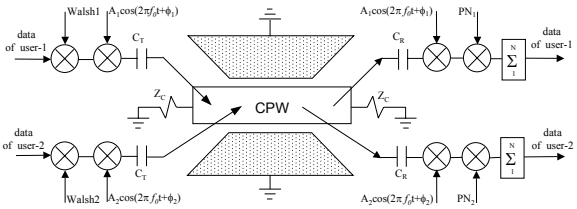


4 Gbp/s/wire Bi-directional Transmitted pattern and Received Waveform

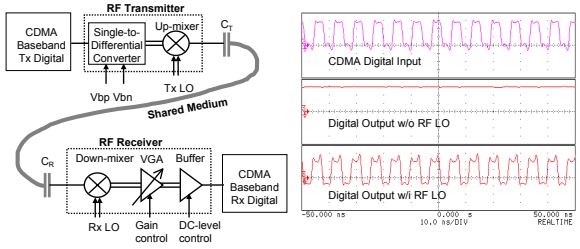
4Gb/s/wire Bi-directional Received data eye diagram

Combined FDMA/CDMA-Interconnect (*Multi-Carrier CDMA-I*)

Combined FDMA/CDMA (Multi-Carrier CDMA) Interconnect



Combined FDMA/CDMA-I System



- Digital Clock = 1.1 GHz
- Data Rate = 275 Mbps
- RF Carrier Freq. = 5 GHz
- Power Consumption = 48 mW per FDMA/CDMA transceiver pair

New Interconnect System Applications (I)

Source Synchronous CDMA Bus Interface

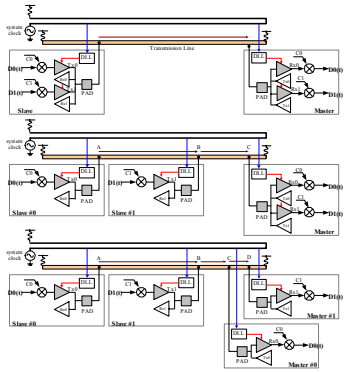
- Conventional *TDMA-I* bus interfaces
  - Designed for fixed & non-reconfigurable system architectures
  - Have extensive data bus latency and limited system performance
- Source Synchronous *CDMA-I* Bus Interface
  - Utilizes DS-CDMA technique + source synchronous clocking
  - Achieves real-time re-configurable I/O + simultaneous multi-chip access capability
  - Increases data channel concurrency and reduces the channel latency

2X2 SS *CDMA-I* Bus Interface Architectures

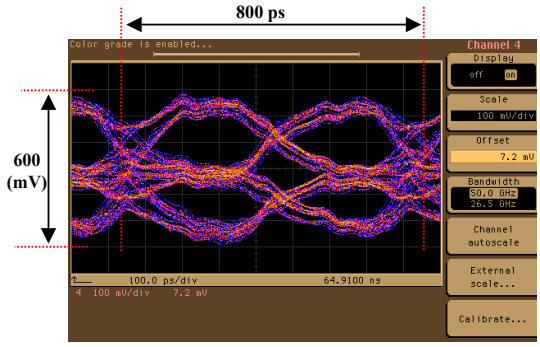
One slave (with 2 Txs) -to- One master (with 2 Rxs)

Two slaves (with 2 Txs) -to- One master (with 2 Rxs)

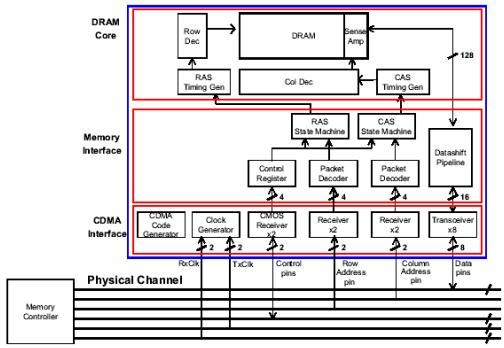
Two slaves (with 2 Txs) -to- Two masters (with 2 Rxs)



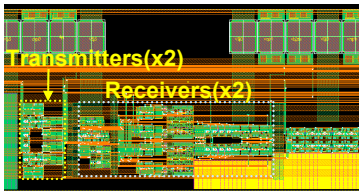
Measured 3-level Eye Diagram at 2.5Gb/s/pin



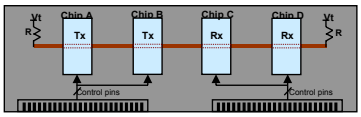
SS-CDMA Interconnect Enabled CDMA DRAM



SS *CDMA-I* Bus Transceiver and Test module



❑ The new chip is being fabricated in SAMSUNG 0.10-um DRAM Process and packaged in a WBGA



❑ Test PCB module with four (2X2) chips

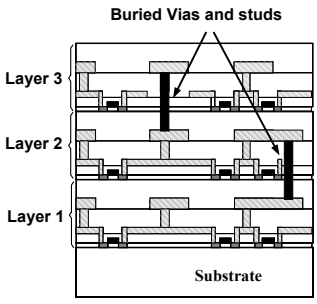
Comparison of DRAM Bus Interface Standard

	# of Parallel high-speed Data Channels	# of Parallel High-speed Address Channels	# of Parallel High-speed Clock Channels	Total # of High-speed Data & Add. Channels	Min. # of Shielding Channels for Data & Add.	Data Rate (Mbps)	Total Data Bandwidth
SDRAM (PC-133)	64	12	1	76	-	133	1.1 Gbyte/s
Rambus DRAM	16	8	2 (differential)	24	24	400 * 2	1.6 Gbyte/s
DDR(SSTL-2)	64	12	8 (data strobe)	76	-	133 * 2	2.1 Gbyte/s
CDMA DRAM	4	2	2 (differential)	6	6	800 * 4	1.6 Gbyte/s

- RDRAM uses 2 differential (CTM/CTMB,CFM/CFMB) clock lines for source synchronous clocking
- DDR uses 8 data strobe (DQS) lines for source synchronous clocking
- CDMA DRAM can use 2 differential clock or CDR for source synchronous clocking
- Both SDRAM and DDR DRAM has some additional command lines which are not listed above.

New Interconnect System Applications (II)

Vertical Interconnect in 3D Integration



Issues:

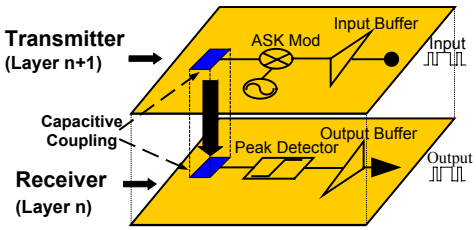
Traditional 3D integration requires complex etching/alignment /metallization for vias and studs

Solution:

Use capacitor-coupled RF-Interconnect to avoid complex processing

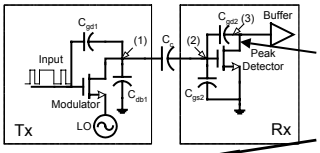
Courtesy: Prof. Jason Woo, UCLA

Self-Synchronized RF-Interconnect (SS RFI)



- ❑ Simple ASK modulation in Tx
- ❑ No synchronization loop in Rx
- ❑ Low power consumption
- ❑ Low output signal jitter

Coupling Capacitance Determination (II)



Detector output signal must exceed output buffer sensitivity S (βV_{dd}) within partial carrier period ($\gamma T_{carrier}$)

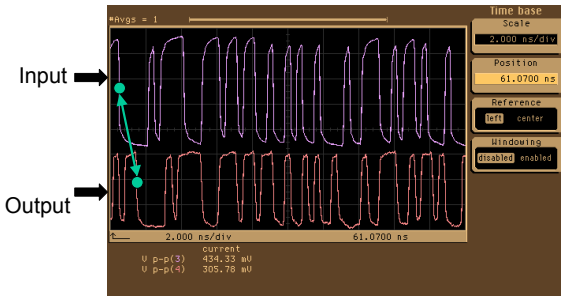
$$\frac{It}{C_3} \geq S = \beta V_{dd} \quad t \leq \gamma T_{carrier} \qquad C_3 \geq C_{ox}(WL)_{buffer}$$

$$\frac{\mu C_{ox}(W/L)_2 V_{eff}^{\ 2} \gamma T_{carrier}}{C_3} \geq \beta \quad \beta = 1/3;\ \gamma = 1/2;\ C_3 = 3fF \Rightarrow W_2 \geq 3\mu m$$

$$C_2 \geq 20\ fF \qquad C_c \geq \frac{\alpha}{1-\alpha} C_2 \quad \alpha = 1/3 \Rightarrow C_c \geq 10\ fF$$

Output/Input Waveforms

Input signal: 3Gbps PRBS, Carrier: 10GHz



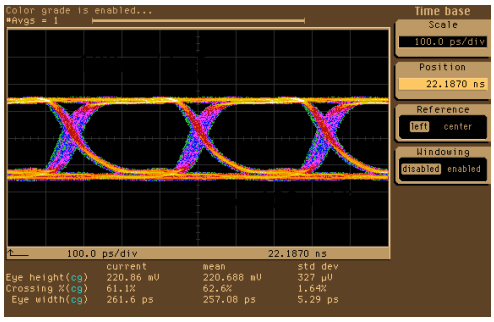
Bit Error Rate: 1.2×10^{-10}

Output Signal Eye Diagram

Input signal: 3Gbps PRBS, Carrier: 10GHz

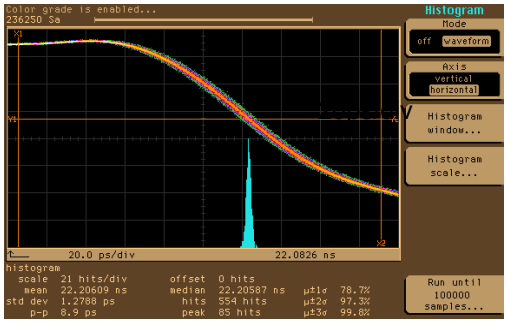
Height: **220mv**

Width: **257ps**



Measured Jitter Result

Input signal: 3Gbps PRBS, Carrier: 10GHz



Jitter: 1.28ps

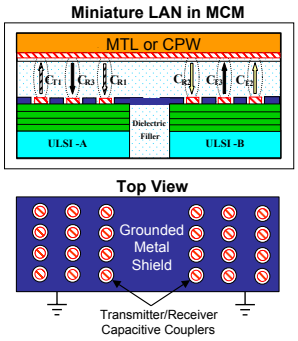
SS RFI Performance

PRBS Input Signal	3Gbps
Carrier	10GHz
Jitter	1.28ps rms
BER	1.2×10^{-10}
Coupling Capacitance	60fF
Active Chip Area	0.02mm^2
Power Consumption	4mW from 1.8V supply

New Interconnect System Applications (III)

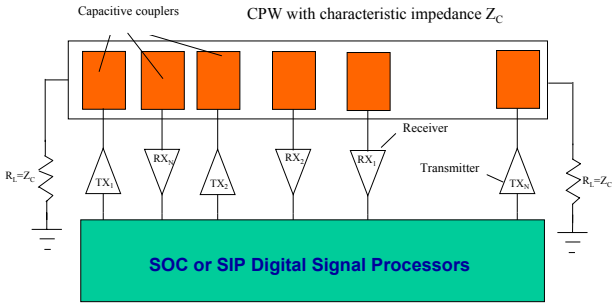
Multi-Carrier Interconnect System

- **System Concept**
  - Transmission medium : Low loss and dispersion-free microwave transmission line
  - Capacitive coupling for multi-I/O's
  - RF-modulation for coupling efficiency
- **System Advantage**
  - Ultra-high bandwidth (**100Gbps/channel** & **20Tbps/chip**)
  - Multi-I/Os per channel, simultaneous communications via shared MTL using FDMA/CDMA multiple access algorithms
  - Reconfigurable network for on-line system-level rewiring (**Architecture reconfigurable on-the-fly**)

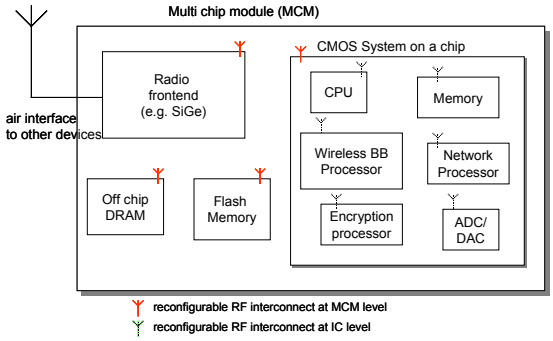


M. Frank Chang *et al*, *Proceedings of the IEEE*, April 2001

Multi-Carrier Interconnect With Multiple I/Os

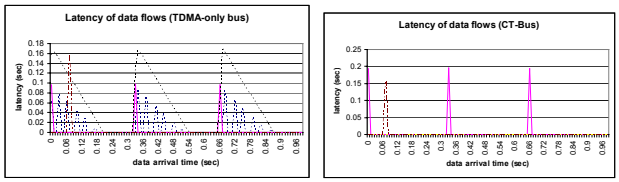


RINGS (Reconfigurable Interconnect for Next Generation System)*



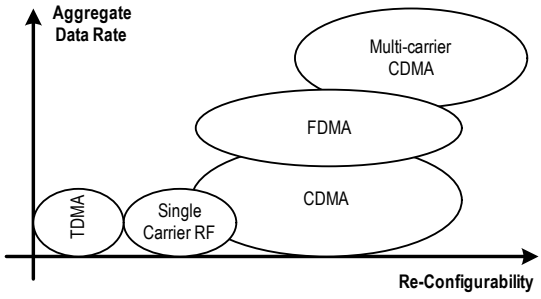
*Ingrid M. Verbauwhede, M.F. Chang etal, "RINGS" 2002 ACM International Workshop

Comparison of Latency *TDMA-I* versus *CDMA/TDMA-I**



*Lai and Verbauwhede "A heterogeneous CDMA/TDMA bus for future SOC" 38 Annual Asilomar Conference on Signals, systems and computers

Comparison of Interconnect Schemes



Summary

- Traditional *TDMA-I* does not meet future SOC/SIP interconnect needs in dynamic channel/bandwidth re-allocation, concurrent simultaneous multi-I/O service and bi-directional communications on shared transmission medium

- New Interconnects based on additional CDMA and FDMA algorithms (*CDMA-I, FDMA-I and Multi-Carrier CDMA-I*) can satisfy the above needs and would alter the paradigm of ULSI data communications and enable reconfigurable architecture designs for future computing/processing systems