Wireless Communications Using Integrated Antennas#

K. K. O, K. Kim, B. Floyd, J. Mehta, H. Yoon, C.-M. Hung, D. Bravo, T. Dickson, X. Guo, R. Li, N. Trichy, J. Caserta, W. Bomstad, J. Branch, D.-J. Yang, J. Bohorquez, L. Gao, A. Sugavanam, J.-J. Lin, J. Chen, S. Yu, M.-H. Hwang, H. Wu and J. Brewer

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***Abstract*- The feasibility of integrating antennas and required circuits to form wireless interconnects in foundry digital CMOS technologies has been demonstrated. This technology can potentially be applied for implementation of wireless clock distribution systems, a true single chip radio for general purpose communication, on-chip and inter-chip data communication systems, RFID tags, RF sensors/radars and others.**

Scaling of MOS transistor length to 0.10 μm and below has made the implementation of CMOS circuits operating at 20 GHz and higher feasible. At 24 GHz, a quarter wave antenna needs to be only ~ 3 and 0.9 mm in free space and silicon. These in conjunction with the increases of chip sizes to ~ 2 cm x 2 cm have made the integration of antennas for wireless communication possible. Integrated antennas could potentially be used to relieve the bottleneck with global signal distribution inside integrated circuits. They could be used to lower clock skew [1] (Fig. 1) and to lower I/O pin counts [1],[2], thus reducing the form factor and packaging costs. When integrated with sensors and a power source, a transceiver with on-chip antennas could provide a communication link for sensor network nodes (μnode) (Fig. 2). The nodes can be the size of a grain of rice (~3mm x ~3 mm x a few mm's) and sufficiently inexpensive that they may be disposable. Such nodes could help to accelerate the realization of the Smart Dust vision [3].

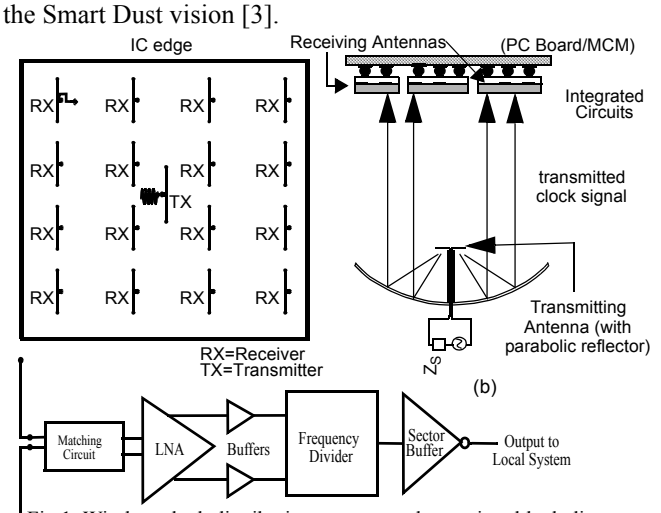
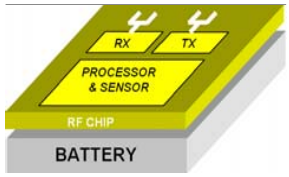


Fig.1: Wireless clock distribution systems and a receiver block diagram

This paper reviews the status of key technologies required to implement these interconnect systems as well as challenges and potential solutions. This paper presents the performance of on-chip antennas on 10-20 Ω-cm silicon substrates commonly used for CMOS technologies [4], circuits which could be implemented in foundry CMOS technologies and wireless interconnects using these [5],[6]. The key challenges including the effects of metal structures associated with integrated circuits [7], heat removal [8] and packaging, as well as, the interaction between transmitted and received signals, and nearby circuits [9] are discussed.

Fig. 3 shows G_a versus frequency plots for varying thicknesses of AlN layer between the silicon and metal chuck of a probe station. The measurements were made using a pair of 2-mm zigzag dipole antennas shown in Fig. 4 and the separation between the antennas was 5 mm. The power transmission gain G_a is defined as



$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}$$

Fig 2, A conceptual diagram of a μ-node.

Dips due to destructive interference effects are observed in the plots. As the AlN thickness is increased, the frequencies at which the dips occur are lowered. This is a clear demonstration of the fact that signal transmission and reception are via wave propagation. The addition of 0.76-mm thick AlN layer improves the power transmission gain by ~10 dB compared to the case when the wafer is in direct contact with the metal chuck. The AlN layer has thermal conductivity comparable to Al, which is critical for efficient heat removal.

These tiny antennas can also be used for communication over air [10]. Fig. 5 shows plots of G_a versus antenna separations up to 10 m for two different substrate thicknesses. The 3-mm on-chip antenna pairs with a 670-μm substrate thickness have ~20 dB more loss compared to the ideal 3-mm dipole pairs, and ~45 dB lower loss than that for a pair of probes. G_a approximately obeys the inverse square law up to 10 m. Fig. 6 also shows the plot for a pair of antennas fabricated on a 20-Ω-cm substrate with thickness of 100 μm. G_a's are improved by ~10 dB due to the reduction of substrate loss

As mentioned, clock distribution can be a potential application for wireless interconnects. On wafer, a 15-GHz transmitted signal 2.2 cm away from a clock receiver with an integrated antenna has been successfully picked up by the receiver and amplified to generate a digital output signal [8] (Fig. 6). Fig. 7 shows the transmitter and receiver fabricated using a 0.18-μm CMOS process [6]. The area including the

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antenna is 5.86 x 10^5 μm^2. The area excluding bond pads is 3.75 x 10^5 or (600 x 600) μm^2. The receiver consumes 40 mW of power. For the clock application, transmission over 2.2 cm is sufficient for the chip with the largest projected size. The power consumption of a system using 16 receivers over the areas projected by the ITRS has been found to be comparable to that of conventional systems [11].On-chip

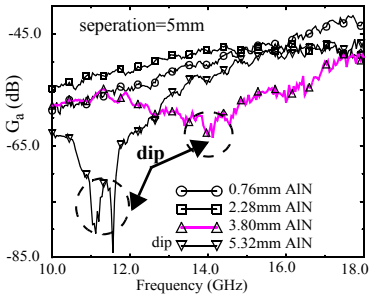


Fig. 3, G_a vs. frequency when the AlN propagating layer thickness is varied.

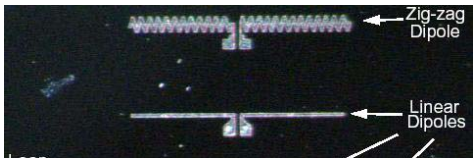


Fig. 4, Integrated antennas fabricated on a 20-Ω-cm substrate.

wireless interconnects have also been demonstrated in a ball grid array package mounted on a PC board (Fig. 8).

Using an external gaussian lens horn antenna (similar to the system in Fig. 1(b)), a clock signal with total skew less than ~14 pS can be provided over an area of 3.8 cm x 3.1 cm. This should be sufficient for a system operating ~3 GHz and this area is ~4X larger than that typically thought possible for synchronization at such frequencies. Furthermore, receiving antennas can be significantly shorter than 1 mm [12].

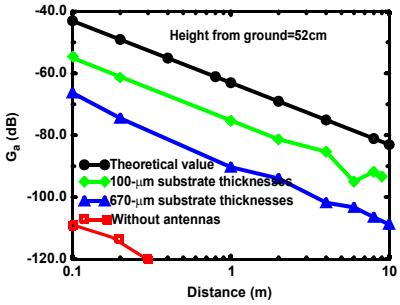


Fig. 5. Antenna gain vs. separation in the outdoor dirt environment for 3-mm zig-zag antennas on 20-Ω-cm substrates with a 3-μm oxide layer and 670 and 100-μm substrate thicknesses.

Metal structures near antennas can change input impedances and phase of received signals. To mitigate this, design guidelines and techniques to correct the phase changes are being developed. Another concern is the interference effects between transmitted signal and nearby circuits, and between the transmitted/received signal and switching noise of nearby circuits [13]. It should be possible to reduce the sensitivity to this by using guard rings and a triple n-well process.

The packaged clock receiver circuit (Fig. 8) has also been utilized to receive a 14.3 GHz clock signal transmitted using a 2-mm long zigzag dipole antenna fabricated on a 20-Ω-cm substrate. The signal is picked up by the receiver which is 40 cm away, amplified and frequency divided by 8 to generate a ~1.79-GHz local clock signal. The range was limited due to the ~-40-dBm sensitivity of clock receiver [6]. This modest demonstration indicates that it is possible to communicate over free space using CMOS radios with integrated antennas

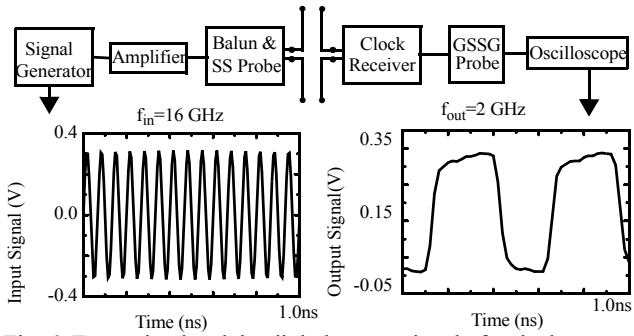


Fig. 6, Transmitted and the digital output signal of a clock receiver 2.2 cm away from the transmitting antenna.

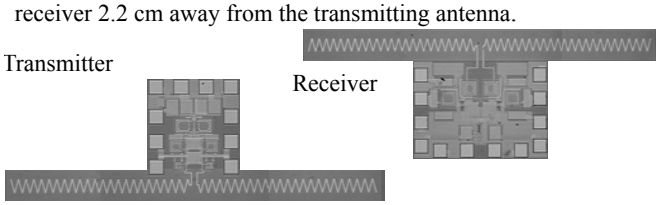
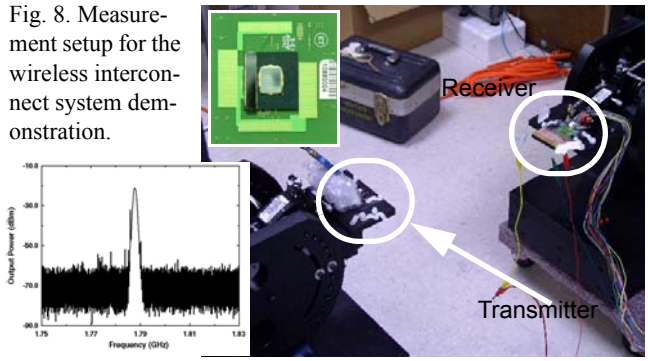


Fig. 7, A TX and RX pair fabricated in a 0.18-μm CMOS process.

Fig. 8. Measurement setup for the wireless interconnect system demonstration.



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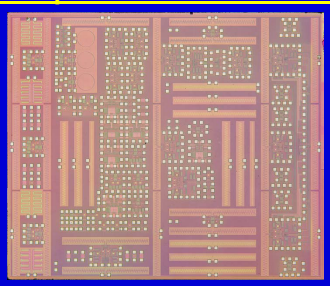
Outline

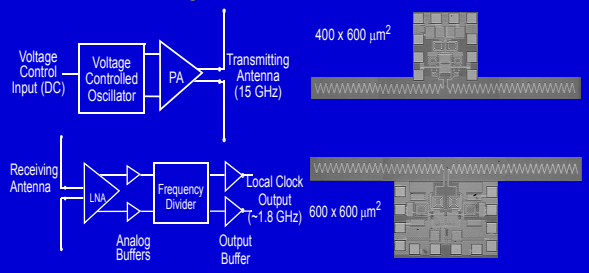
- Recent demonstrations for uses of integrated antennas
  - Intra-chip wireless communication
- Basic technology & challenges
- Other applications
- Conclusions

Intra-chip wireless communication



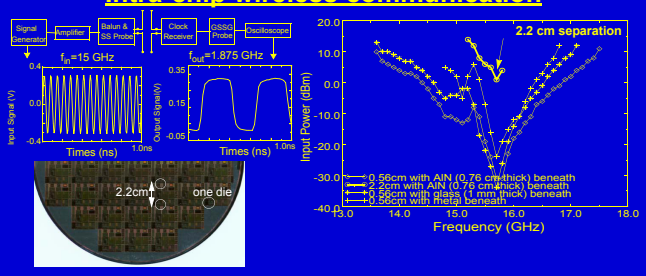
- 6 mm x 7 mm testchip fabricated in the UMC 0.18-μm CMOS process.
- 2-mm long integrated antennas, transmitters and receivers with integrated antennas for clock distribution.
- In between, numerous test structures and dummy fills are present.

Intra-chip wireless communication



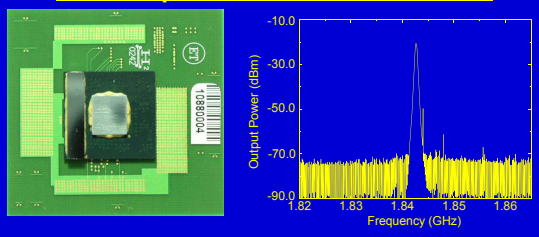
- Transmitter generates a 15 GHz mono-tone sinewave, amplifies and transmits.
- Receiver amplifies, frequency divides, and buffers to provide local clock.
- Transmitter and receiver consume ~ 50 and 40 mW.

Intra-chip wireless communication



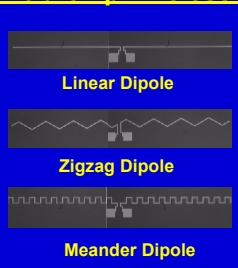
- From an antenna located 2.2 cm away from a receiver, a 15 GHz signal was transmitted and successfully picked up.
- For clock distribution, 2.2 cm is sufficient for the largest chip size projected by International Roadmap for Semiconductors.

Intra-chip wireless communication



- The chip was packaged in a ball grid array package (1.6 cm x 1.6 cm) and mounted on a PC board (3.8 cm x 3.8 cm).
- Transmitter and receiver were separated by ~ 4 mm.
- Testing requires only dc connections except for the ~1.8 GHz frequency divided output signal.
- Wireless interconnection is possible inside a package.

Intra-chip wireless communication (Antennas)

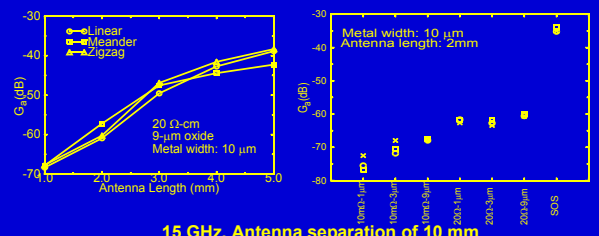


$$G_a = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2$$

$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}$$

- Evaluated linear, meander, zigzag dipole as well as other antennas fabricated on SiO_2/Si using ~ 1.0 to 2.0 μm thick Al lines.
- Power transmission gain, G_a includes individual antenna gains and propagation loss.
- G_a is obtained by measuring s-parameters.

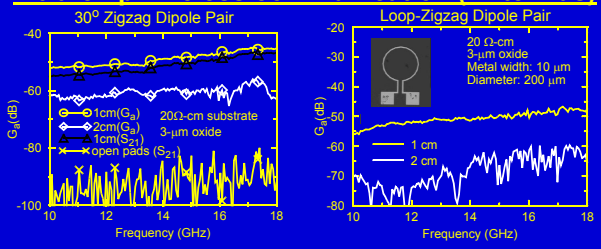
Intra-chip wireless communication (Antennas)



15 GHz, Antenna separation of 10 mm

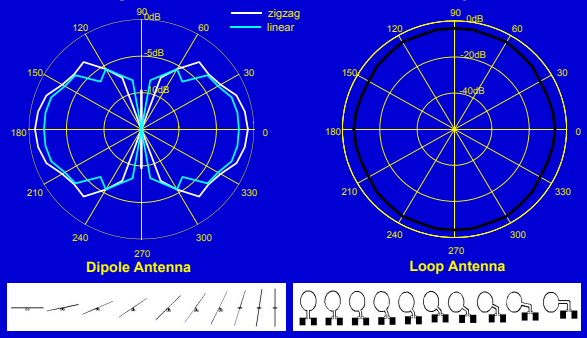
- Zigzag dipole antennas have higher gain than linear dipole antennas.
- 5-mm antenna pair shows ~30 dB higher gain than 1-mm antenna pair.
- Antennas on SOS show the highest gain due to negligible substrate loss.
- 10-dB gain increase by increasing metal width from 2.5 to 30 μm.

Intra-chip wireless communication (Antennas)



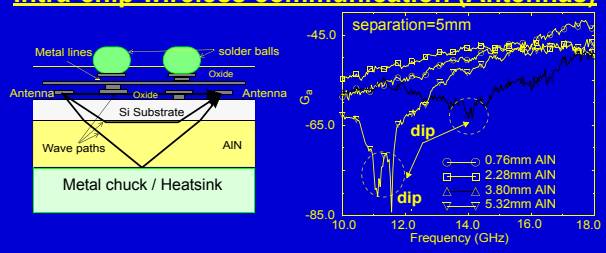
- The zigzag dipole pair shows -56 dB gain for 2cm separation near 17 GHz.
- Loop-zigzag pair shows ~-60 dB for 2 cm separation.
- Signal transmission is lossy and need large gain in the system.
- It is possible to couple signals on-chip using integrated antennas.
- Many knobs to improve and optimize antenna performance.

Intra-chip wireless communication (Antennas)



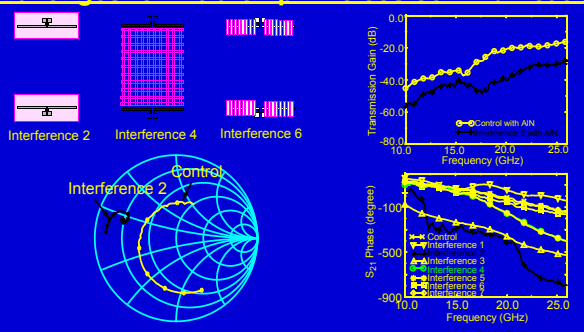
- The dipole antennas have patterns similar to that of a short linear dipole antenna.

Intra-chip wireless communication (Antennas)



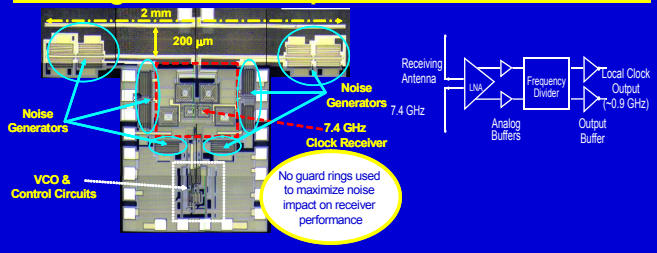
- Many possible paths for signal propagation.
- Destructive and constructive interference effects.
- Destructive interference dips are seen in gain versus frequency plots.
- The dip frequency decreases as AlN thickness is increased.
- Clear indication that the signal coupling is due to wave propagation.
- Interference effect should be smaller in a package.

Challenges for intra-chip wireless communication



- Adjacent metal structures can affect S_{11}, and G_a.
- Design guidelines and rules, and in some applications, compensation techniques are needed.

Challenges for Intra-chip Wireless Communication



- A 7.4-GHz clock receiver fabricated in a 0.25-µm CMOS process was surrounded by 800 1X and 800 10X inverters. The total capacitance is ~ 50 pF.
- No guard ring to maximize noise impact. Clock is transmitted from an antenna. The receiver output is used to drive the inverter chains.
- Transmitted power levels were 15 dBm (32 mW) and 17.5 dBm (56 mW).

Intra-chip wireless communication

Transmitted power to Antenna	32 mW	56 mW
Quiet	0.57%	0.41%
All of small inverters	0.96%	0.76%
Half of small and half of large antennas	3.20%	1.83%
All inverters	No Lock	3.63%

- Mismatch loss for the antenna pair is 15 dB. G_a is ~ 15 dB lower than that at 24 GHz. Corresponds to -15 and -12.5 dBm transmitted power at 24 GHz.
- As more inverters are turned on, jitter which is the variation of a period increases and can eventually lead to a failure of the clock receiver.
- Changes in bias currents for the LNA and divider due to substrate noise.
- Can be re-locked by increasing the transmitted power and adjusting the self-oscillation frequency of the divider.
- Possible to better protect the receiver using guard rings and deep n-wells. More robust receiver design should also improve noise immunity.
- The first use of wireless clock to drive digital circuits.

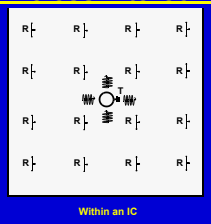
Why intra-chip wireless interconnects

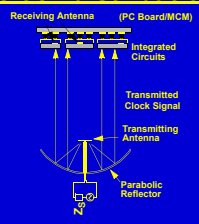
- Global interconnection problem is a serious concern as the operating frequency and chip size are increased.
- Potential interconnection architectures unanticipated in current systems which could bring about a paradigm shift.
  - Optical interconnects
  - Superconducting interconnects
  - Biological interconnects
- Wireless approach is an interconnect architecture in which signals propagate at the speed of light and which fits better to the CMOS technology trend.

2003 ITRS

Year Minimum Feature Size	2007 65 nm	2009 50 nm	2013 32 nm
# I/O Pins (ASICS)	2200	2400	2700
Chip Clock Frequency	9.29 GHz	12.4 GHz	22.4 GHz
Chip-to-board Clock Frequency	4.88 GHz	7.63 GHz	18.6 GHz
ASIC Chip Size (mm^2)	24x24	24x24	24x 24
µP Chip Size (mm^2) Linear Dimension (mm)	310 17.6	310 17.6	310 17.6
f_T (GHz)	200	280	500
RF Circuit Frequency (GHz)	~67	~93	~170
# of Metal Layers	11	12	16
025λ in Si	330 µm	235 µm	130 µm
Power Supply (V)	1.1	1.0	0.9
Max. Power (uP), Heat Sink	190 W	210 W	250 W

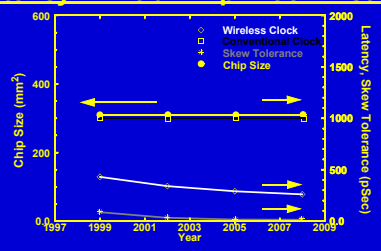
Wireless Interconnect for clock distribution





- Clock distribution has been used as the technology driver.
- Dispersion increases the rise time and fall time of square waves used for clock. Almost no dispersion in wireless systems.
- With each generation, balancing delays through clock networks requires subtraction of delays to obtain smaller differences or skew.
- Jitter or variation of clock period is the major source of clock phase mismatches.

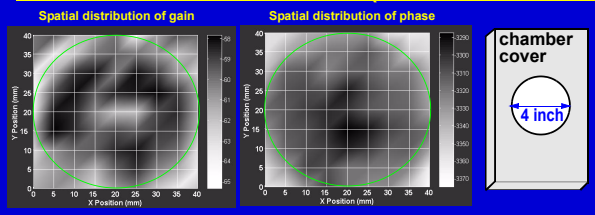
Latency in Intra-Chip Clock Dist. Systems



16 receivers

- The latency in a conventional clock system stays flat with time, while that for a wireless clock system decrease with time.
- By 2008, to meet the skew specification, the latencies need to be matched within ~ 0.9% versus ~ 3% for a wireless system.
- If more receivers are utilized, the latency can be made even smaller.
- Distributed clock network should decrease temperature variations.

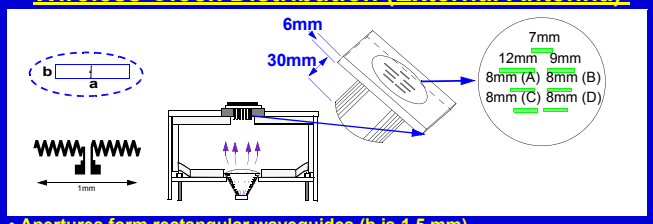
Wireless Clock Distribution (External Antenna)



in a 4-inch-diameter opening, 7.5-inch separation

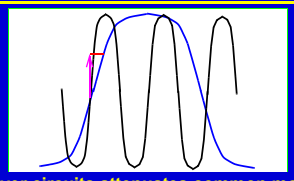
- Phase and amplitude vary between -3290 and -3350 degree at 24 GHz and ~5 dB over 12.6 cm^2. When divided down to 3 GHz, approximate skew is around 3% of a period including the gain and phase variations.
- This is ~4X larger than that thought possible for synchronization at 3 GHz.
- Potentially better clock skew performance.

Wireless Clock Distribution (External Antenna)



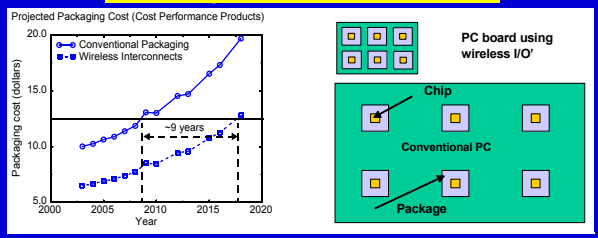
- Apertures form rectangular waveguides (b is 1.5 mm).
- TE_{10} mode.
- Fins form parallel plate waveguides.
- Measured antenna gain through a heatsink is ~1-5 dB higher than the case without a heat sink.
- The phase and amplitude distributions are little affected by the heat sink.
- A heat sink can be incorporated into a system with an external antenna.

Jitter in Wireless Clock Dist. Systems



- Differential receiver circuits attenuates common mode supply noise.
- Eliminates long clock lines which pick up noise from nearby circuits.
- Wireless clock distribution systems have a smaller bandwidth compared to conventional systems. This decreases the noise bandwidth and jitter. (3 GHz conventional clock containing 7 harmonics should have a bandwidth of 21 GHz versus ~ 5-6 GHz of a wireless clock distribution system)
- The amplitude to phase conversion occurs at higher frequency than the local clock frequency. Sharper transitions result smaller jitter.
- RMS Jitter in the absence of the noise of other circuits is ~1 pS.

Inter-chip data communication



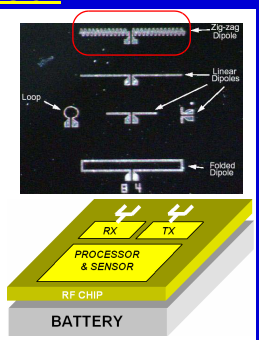
- By 2013 (32 nm), the number of I/O's is expected to be as high as 2700.
- Frequency and Code Division Multiplexing can be used to replace the I/O's with wireless channels. This can reduce I/O counts while maintaining parallel I/O architecture. Shift out the packaging cost curve by as much as 9 years.
- Elimination of off-chip wires reduces chip spacing, latency, and size.

Inter-chip data communication

- Additional capability
  - A bus where more than one pair of devices can communicate.
  - A bus where more than one set of information can be broadcasted.
- Total data rate of ~200-400 GBits/sec can be achieved using the 32 nm generation. This is a limitation.
  - Approaches to increase the over-all data rate are needed.
  - Finding appropriate applications will be critical.
- Overhead/latency associated with transmitter and receiver is a concern.

μNode Vision

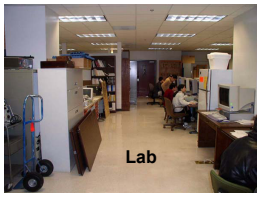
- A μNode incorporates a transceiver, a digital processor, and CMOS compatible sensors.
- A μNode transceiver makes use of on-chip antennas
- Requires only power and ground connections to a battery.
- Wireless transmission and reception at ~ 24 GHz over short distances (1-5 meters).
- A typical μNode will be fabricated using digital CMOS technology (130 nm or beyond).

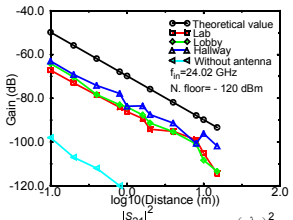


μNode Vision

- A μNode when packaged with a battery will be ~ 3 mm x 3 mm x 5 mm, weigh less than 20 mg, and have a battery life of 1 to 30 days depending on duty cycle.
- Disposable Radios. Costs less than $1.
- Smart Dusts using RF for communication. Groups of μNodes can form self-organizing communication networks.

Sufficient power transfer between integrated antennas separated by 1 to 15 m at 24 GHz?



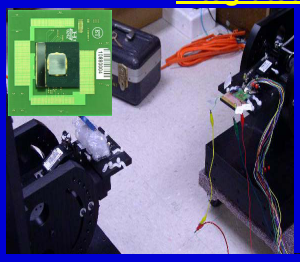


2 mm zigzag dipole (bend angle= 30°, metal width= 30 mm)
51 cm from the ground

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2$$

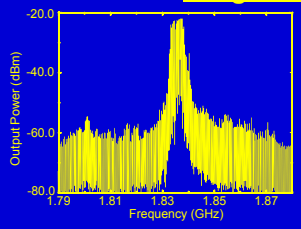
- For line of sight links, path loss is around 15 dB below the ideal 2-mm long dipole case.
- R^{-2} dependence up to ~ 8 m. Interference effects above 8 m.
- The corresponding efficiency is ~15%.

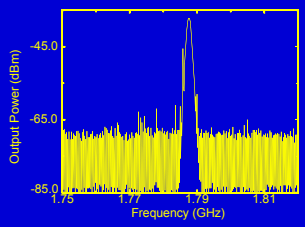
Wireless communication over air using integrated antennas



- Communication between a transmitting antenna and a receiver mounted on a PC board separated by 40 cm.
- Transmitted power level is 21 dBm at ~ 15 GHz.

Wireless communication over air using integrated antennas





- Output spectrum without the transmitted clock signal is broad due to the self-oscillating nature of the frequency divider.
- Output spectrum is well defined with the transmitted clock signal.
- This modest and not optimized demonstration suggests communication over air using integrated antennas is possible.

Wireless communication over air using integrated antennas

A 20-GHz CMOS Down-Converter with On-chip Antenna (Paper 14.8 in 2005 ISSCC)

S. Yu, J. J. Lin, and K. K. O

Using a 20 GHz down-converter fabricated in a 0.13-μm CMOS process, this paper demonstrates the feasibility of a pair of IC's with on-chip antennas communicating over free space. The circuit achieves 9 dB conversion gain and 6.6 dB SSB NF while consuming 12.8 mW from a 1.5 V supply.

Conclusions

- Wireless interconnection within a packaged integrated circuit is possible.
- Wireless inter-chip data communication should also be possible.
- It should be possible to use integrated antennas for conventional over the air communication. This can be used to implement a true single chip radio.
- On-chip antennas could also be used in radar/sensor applications.
- As CMOS technology advances, it will require smaller areas to implement wireless interconnects. Wireless interconnects fit well with the projected technology trend compared to the other potential paradigm shifts.

Acknowledgments

- The work on wireless clock distribution is supported by SRC (Task ID: 885).
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- The work on inter-chip data communication is supported by NSF.