A Wireless Chip Interconnect Using Resonant Coupling Between Spiral Inductors

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1. Research Target

With the continuous downsizing of CMOS technology, various components such as processors, memories, analog circuits, RF interface, are integrated in a single chip. It is called a system LSI. However, it takes considerable time to develop system LSIs, and the integration of a wide variety of system functions on a single chip invites considerable low yield. As an alternative, attention has been drawn to the System-in-Package. Also in our COE program, development of the 3-Dimensional Custom-Stack System (3DCSS) is one of the significant themes. In conventional 3D IC fabrication technique, vias with large aspect-ratio are required, in order to connect the stacked chip [1]. A wireless interconnect utilizing capacitor coupling has been proposed and it may avoid forming the vias [2]. However, the distance between the stacked chips can not be extended so as cool the internal circuits, because of the capacitive coupling. Thus, the heat dissipation issue is still unsolved. Two types of wireless connection are studied in our COE program. One is global connection, which communicates beyond neighboring chips using microwave [3]. The other is local connection, which is pass massively parallel between two chips placed in face-to-face. The global connection is useful for broadcasting, global control, etc. On the other hand, the local connection can handle huge data volumes due to the massive parallel structure, and it is useful for communication of 2D vision information. In this manuscript, we propose a wireless interconnect for the local connection utilizing resonant coupling between spiral inductors (see Figure 1).

2. Analysis and modeling of spiral inductor pair

In order to utilize circuit simulators for the design, we introduce an equivalent circuit of the spiral inductor pair. Figure 2 shows the simple equivalent circuit. L, C, and R are the self-inductance, parasitic capacitance and loss resistance of the spiral inductor, respectively. M and k are the mutual inductance and the coupling coefficient between the spiral inductor pair. 2-port S-parameter data has been obtained from FDTD 3D electromagnetic-field analysis. Then, the element values in Figure 2 were calculated by data-fitting to the 2-port S-parameter data. In layout of the spiral inductor, line width and space were 10μm and 2μm, respectively. The shape was square and the outer diameter was fixed at 300μm. As parameters, the number of turns and distance between the spiral inductor pair were selected. When the number of turns of the spiral inductor is 5-turn and the distance between the spiral inductor pair is 100μm, the inductance of L_1 and L_2 are about 9nH and the coupling coefficient k is about 0.2.

2. Circuit configuration and test chip design

Figure 3 shows a circuit diagram including the model of the spiral inductor pair. Note that capacitors Ca_1 and Ca_2 are connected to the inductors L_1 and L_2, in order to implement resonators in both the transmitter and the receiver. Although the spiral inductor without the additional capacitor has self-resonant frequency, Ca_1 and Ca_2 reduce the resonant frequencies until the convenient frequency for typical communications. A MOSFET M_1 works as driver in the transmitter. A return zero signals (RZ) is given to the gate of M_1. The resonant frequencies of the resonators in both the transmitter and the receiver are made equal to the transmission frequency of the return zero signals, by connecting the capacitors Ca_1 and Ca_2. The resonance property enlarges the received signal. On the other hand, it causes the excess oscillation due to the resonance phenomenon as shown in Figure 4. In order to suppress the excess oscillation, MOSFETs M_2 and M_3 are employed. Timing signals t_1 and t_2 in Figure 4 control the M_2 and M_3, respectively. They short out L_1 and L_2 at the timing as shown in Figure 4 and the excess oscillation can be suppressed. The timing signal t_1 for transmitter has same phase of transmission data. On the other hand, the timing signal t_2 should be tuned to the timing of the receiving data. The 125ps phase resolution is sufficient for 1Gbps transmitting. 1Gbps transmitting is possible when t_2 has the 125ps phase resolution.

3. Test-Chip Evaluation Results

A test-chip was designed and fabricated with a 0.25μm 5 metals CMOS technology. Figure 5 shows the microphotograph of the test chip. The inductor size is 300μm. Two chips were set on manipulators in face-to-face and transfer characteristics were measured. The measurement setup is shown in Figure 6. The surface of the chip for transmitter and the surface of the chip for receiver are oppose. Figure 7 shows a measured result. The input data is return zero signals (RZ) and the output data is not return zero signals (NRZ). The data rate of 800Mbps was obtained at 2.5V supply and 9mW power dissipation.

4. Conclusions

We have presented an interconnect scheme between the stacked chips based on resonant coupling of the integrated spiral inductor pair. The test chip was evaluated

and transmission of 800Mbps/Channel was realized.

5. Future plan

The next studies are “Size-reduction of the spiral inductor”, “Less power consumption” and “Higher frequency communication”, which are necessary conditions for more multiplex channel communication. 100 channels for multiplex communication, 100μm x 100μm size for spiral inductor, 1mW power consumption per channel and 5Gbps communication are next targets.

References

[1] J.Burns, *et al.*, *ISSCC Digest of Tech. Papers*, pp.142-143, Feb.2001.

[2] K.Kanda, *et al.*, *ISSCC Digest of Tech. Papers*, pp.186-187, Feb. 2003.

[3] A.B.M.H.Rashid, *et al.*, *IEEE Electron Device Letters*, Vol.23, No.12, pp.731-733, Dec. 2002.

[4] D. Mizoguchi, et al., *ISSCC Digest of Tech. Papers*, pp.142-143, Feb. 2004.

[5] M. Sasaki, D. Arizono, A. Iwata, "A wireless chip interconnection using resonant coupling between spiral inductors," *Proc. of Second Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing*, (2004) pp.104-108.

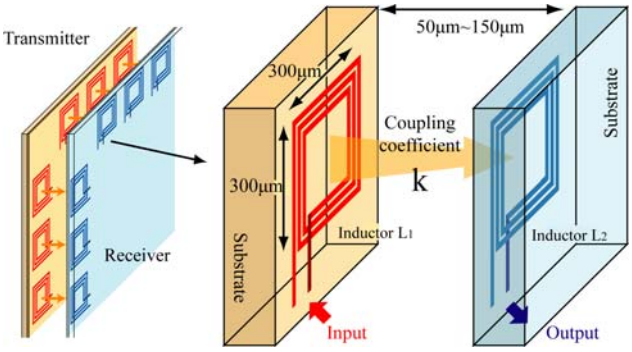

Figure 1: Spiral inductor based wireless interconnects.

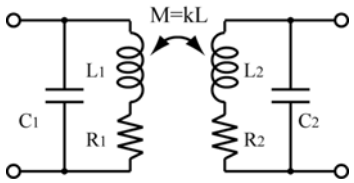

Figure 2: An equivalent model of spiral inductor pair.

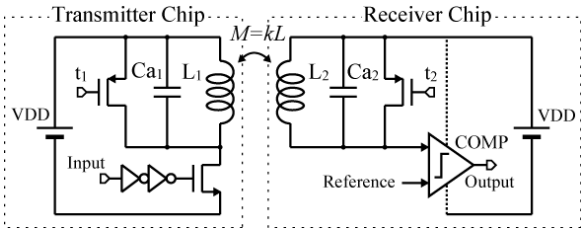

Figure 3: Circuit diagram.

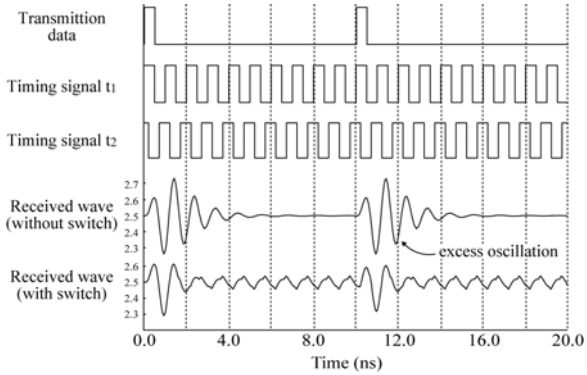

Figure 4: Simulation results.

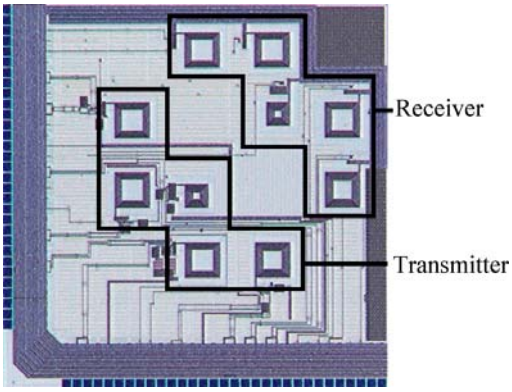

Figure 5: Microphotograph of the test chip.

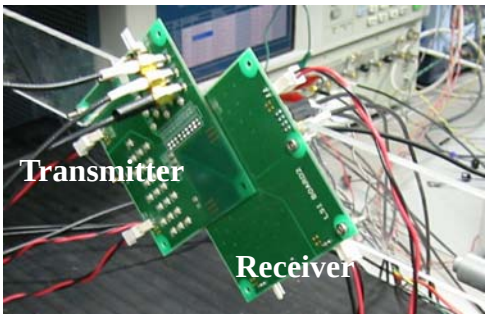

Figure 6: Measurement Setup

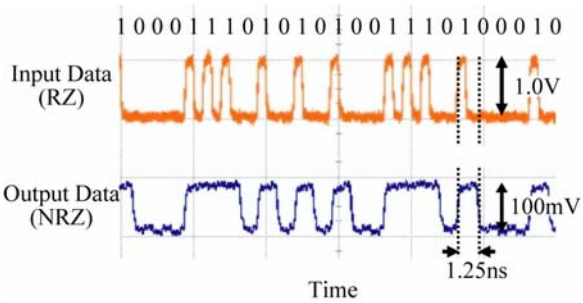

Figure 7: Measurement results.

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Background

Necessary Technology

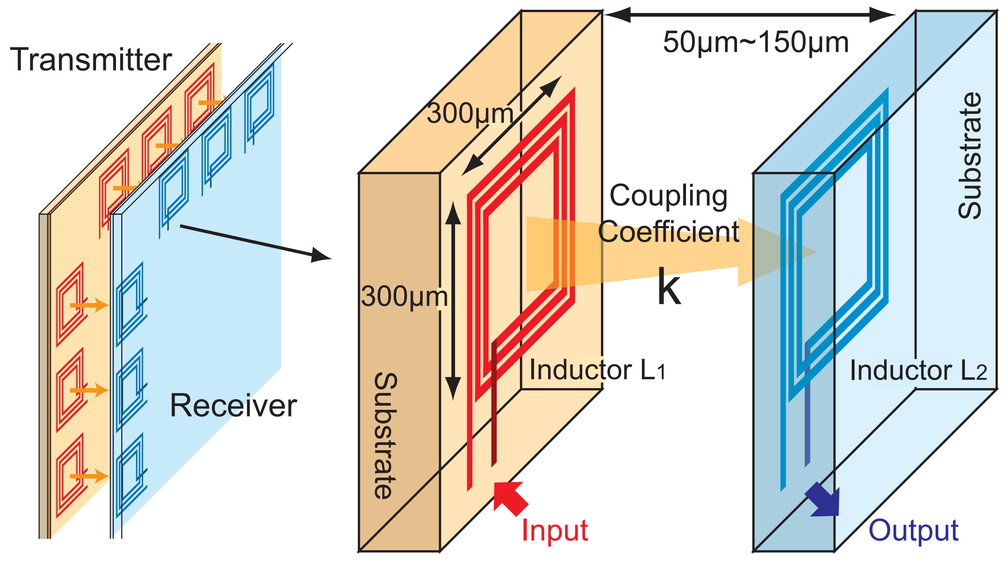
3D IC fabrication technique

3-Dimensional Custom-Stack System (3DCSS)

Communication between two Chips : Inductor Coupling

Handle huge data volumes due to the massive parallel structure

⇨ Communication of 2D vision information



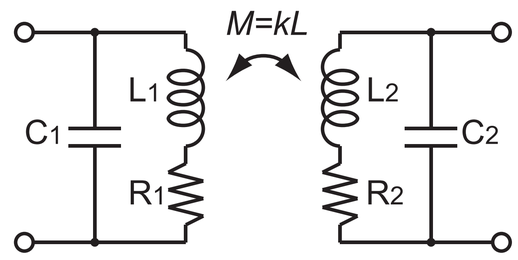
Spiral inductor based wireless interconnects

Analysis and Modeling of Spiral Inductor pair

Parameter extraction by data-fitting

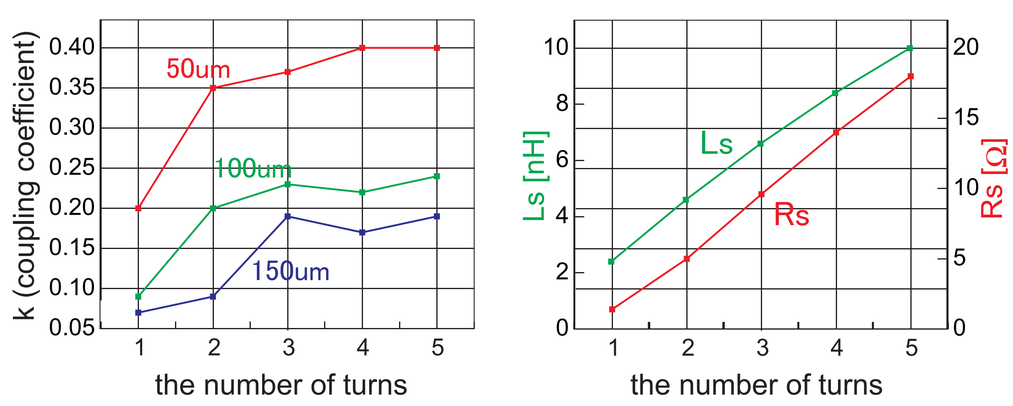
■FDTD 3D electromagnetic-field analysis

- 2-port S-parameter data
- Inductor-Size : 300μm x 300μm
- Line Width and Space : 10μm, 2μm



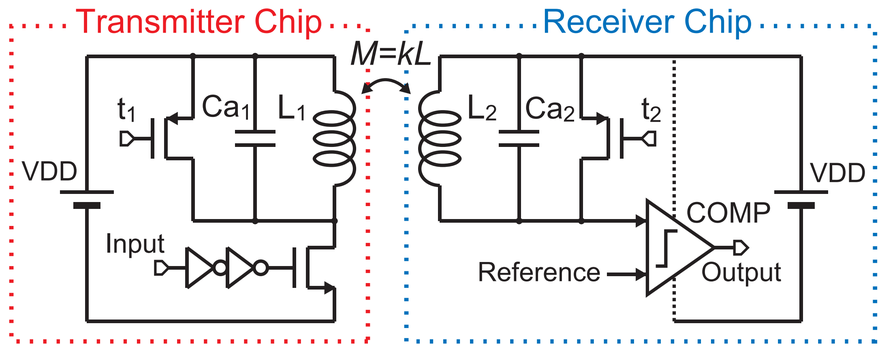
L : self-inductance
C : parasitic capacitance
R : loss resistance
M : mutual-inductance
k : coupling coefficient

An equivalent model of Spiral Inductor pair



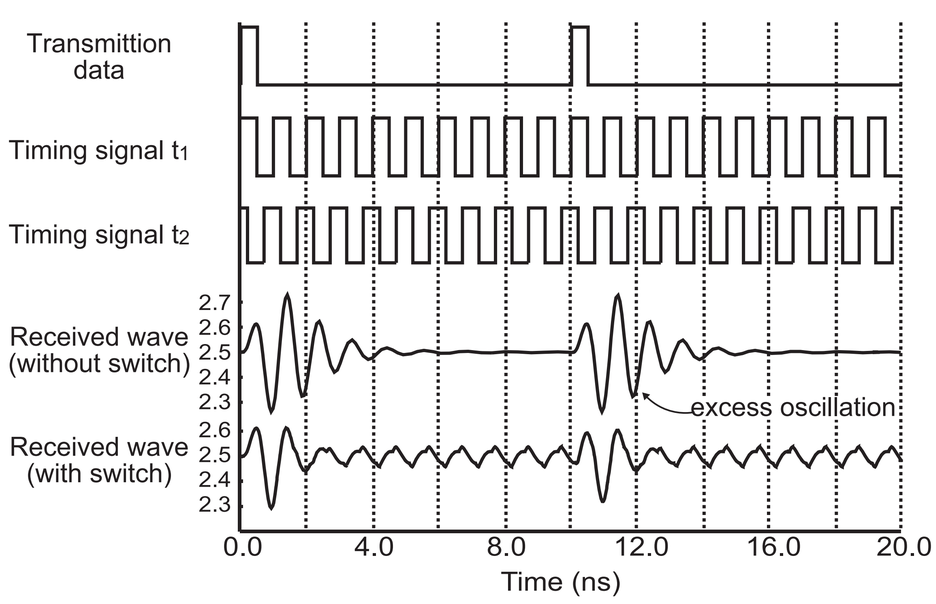
Results of 3D electromagnetic-field simulation

Circuit Configuration



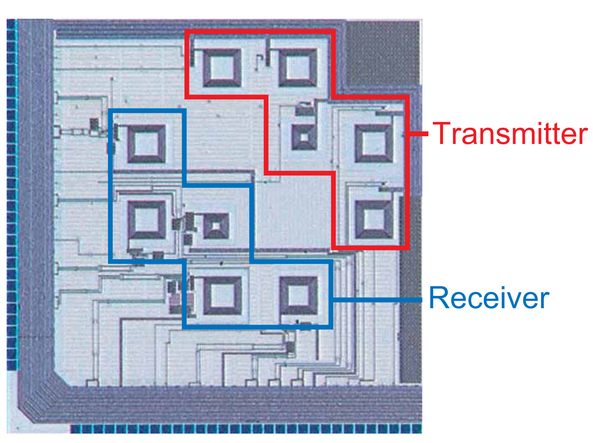
L : Inductor model
Ca : Capacitance for reduction the resonant frequency
t : Timing Signal for suppressing the excess oscillation
COMP : Comparator

- A MOSFET M_1 works as driver in the transmitter.
- The input data and output data are return zero signals and not return zero signals.
- MOSFETs M_2 and M_3 are employed to suppress the excess oscillation (right figure).



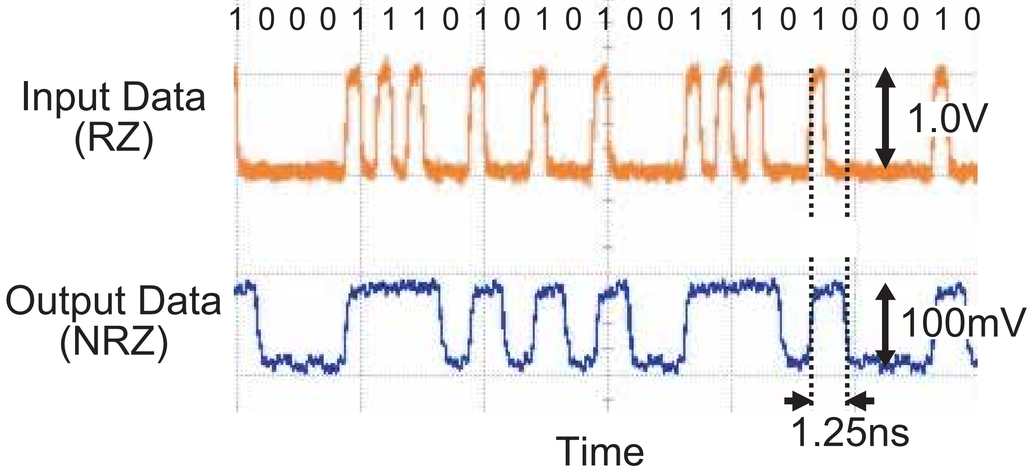
Simulation Result

Test-Chip Evaluation Results



Microphotograph of the test chip

- 0.25μm 5 Metals CMOS technology
- Supply voltage VDD : 2.5V
- Inductor-Size : 300μm x 300μm
- 800Mbps/Channel
- 9mW/Channel
  - Transmitter : 6mW/Channel
  - Receiver : 3mW/Channel



Measurement Result

Conclusions and Future plan

The test chip was evaluated and transmission of 800Mbps/Channel was realized.

- Size-reduction of the spiral inductor
- Less power consumption
- Higher frequency communication

⇨ Future

- 100μm x 100μm size for spiral inductor
- 1mW/Channel power consumption
- 5Gbps/Channel communication