A Low-Noise Circuit Technique for Sensing the Nerve Signals

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1 Introduction

The one of the COE targets is development of the Hyper Brain System implemented by the proposed 3D custom stack system [1]. In the state-of-the-art system, the achievement of the human interface using the nerve signals becomes significant. Neural sensors have been developed for implantable clinical and physiological applications [2-4]. The neural sensors fabricated in a CMOS technology that need to detect a small signal (a few ten μV and a few kHz), therefore the achievement of the low-noise circuit is required. In this paper, a low-noise amplifier which based on a chopper stabilization technique is described for the reduction of low-frequency noise.

2 Architecture of low-noise amplifier

The schematics of the low-noise amplifier using chopper stabilization and 4th-order active low pass filter (LPF) are shown in Fig.1 and 2, respectively. In the low-noise amplifier, the fully-differential Opamps are placed between the first chopper and the second chopper. The first chopper modulates the differential input signal at the chopping frequency. The second chopper demodulates the modulated signal with the chopping frequency; and the low-frequency noise (mainly flicker noise and DC offset voltage) of the fully-differential Opamps are only modulated by the second chopper. Thus the low-frequency noise and white noise at the chopper frequency of the fully-differential Opamps are converted to a chopper frequency component and low-frequency component of low-noise amplifier, respectively.

The modulated low-frequency noise at the chopping frequency are rapidly attenuated by the 4-th order active LPF. We designed the active LPF with a cut-off frequency of 50 kHz, because the modulated noise at the chopping frequency of 400-kHz are attenuated more than 60-dB. The bandwidth variation of active LPF due to fabrication process degrades the attenuation performance of the noise, therefore the active LPF is equipped with trimming circuits to compensate the characteristics of the bandwidth and voltage gain.

The reduction of the low-frequency noise including the flicker noise and DC offset is required for the low-noise amplifier with the voltage gain more than 80 dB. In addition, the input signal is modulated by the first chopper at the chopper frequency. Thus we designed the 2-stage feedback amplifier operates as a second-order active band pass filter (BPF) which implemented by feedback capacitors Cf of 37-pF and resistors Rf of 200 kΩ. Figure 3 shows the ac characteristic of 2-stage feedback amplifier, which demonstrates a total gain of about 70 dB, low cut-off frequency of 5-kHz and high cut-off frequency of 1 MHz. The high cut-off frequency is determined by the ac characteristic of the fully-differential Opamp.

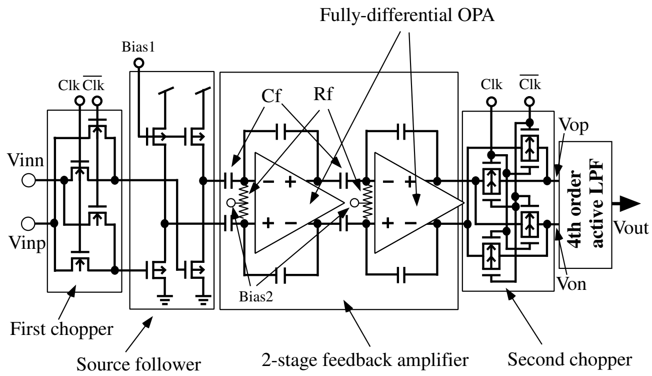

Figure 1: Proposed low-noise amplifier based on the chopper stabilization technique.

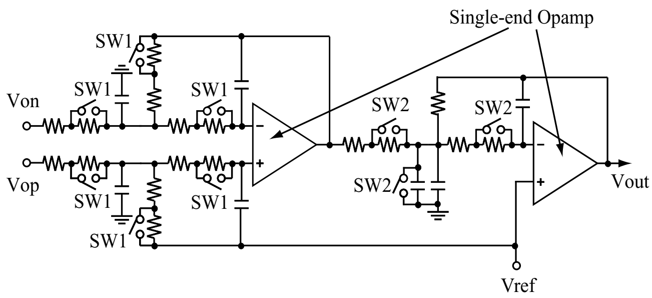

Figure 2: 4th-order active low pass filter .

3 Experimental Results

To evaluate the compensation of the process deviation, the noise spectral density of the low-noise amplifiers without the 4th-order active LPF is plotted in Fig. 4. The 2-stage feedback amplifier has the variation of flicker noise of 90 to 700-nV/root-Hz at a frequency of 1 kHz. On the other hand, the low-noise amplifiers operated with a chopper frequency of 400-kHz compresses its noise variation under 5-nV/root-Hz. Because the white noise of the fully-differential Opamp at the chopping frequency is hardly change. Figure 5 shows the noise spectral density of low-noise amplifier with the 4th-order active LPF. The low-noise amplifier achieved the equivalent input noise of

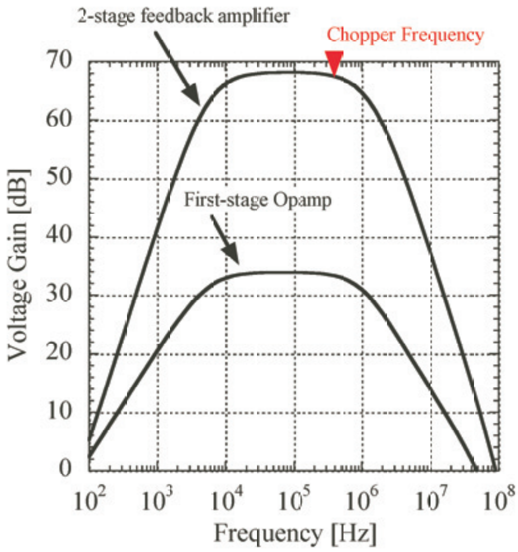

Figure 3: AC characteristic of 2-stage feedback amplifier.

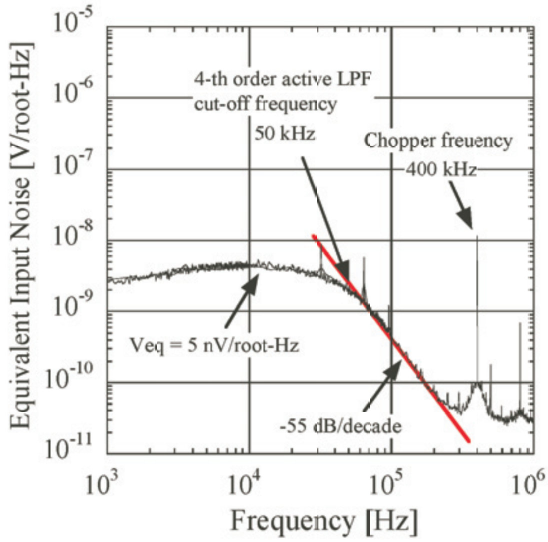

Figure 5: Noise spectral density of the low-noise amplifier.

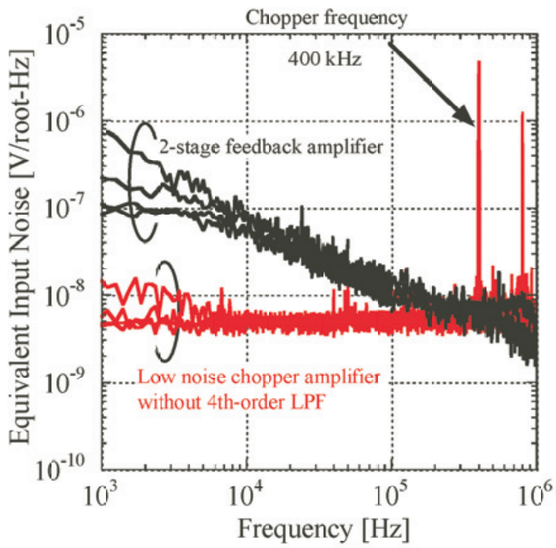

Figure 4: Deviation of the noise spectral density.

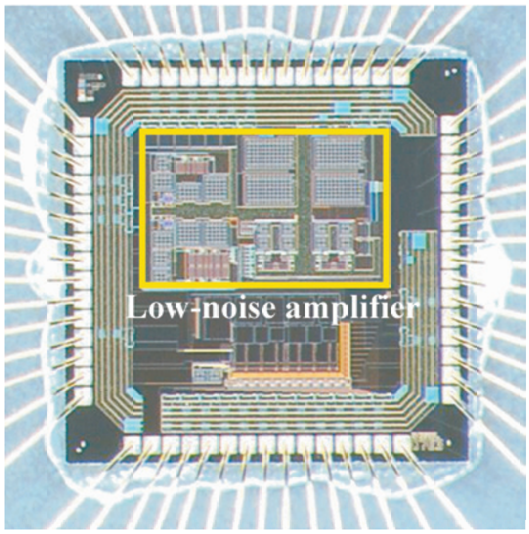

Figure 6: Chip micrograph.

6-nV/root-Hz, and a total in-band noise (∼50 kHz) of chopper amplifier was 1.3 μV. The active LPF attenuates the noise caused from flicker and process variation by the frequency characteristic of -55-dB/decade, therefore the low-noise amplifier can neglect the noise modulated by the chopper frequency. The micrograph of the chip which fabricated by a 0.35-μm CMOS technology is shown in Fig. 6. The chip area is 1.5mm × 1.0mm^2.

4 Conclusions

The chopper stabilized low-noise amplifier with feedback amplifier and post filter was designed. The low-noise amplifier was implemented in the 2-stage feedback amplifier, which operates as the second-order active BPF, and the 4th-order active LPF. The frequency domain analysis showed that the DC and flicker noise of the source-follower and fully-differential Opamp are dramatically reduced. The low-noise amplifier achieved the total in-band noise (∼50 kHz) of 1.3 μV. The power dissipation is 6-mW at a supply voltage of 3 V.

References

[1] A. Iwata et al., Proc. 1st Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing, pp.111-116, 2003.

[2] K. D. Wise, Symp. VLSI Circuit, pp.106-109, 2002.

[3] Q. Bai et al.,IEEE Trans. on Biomedical Eng. 48, pp.911-920, 2000.

[4] T. Yoshida, et al.,IEICE Trans. on Fund. E87-A, pp.376-383, 2004.

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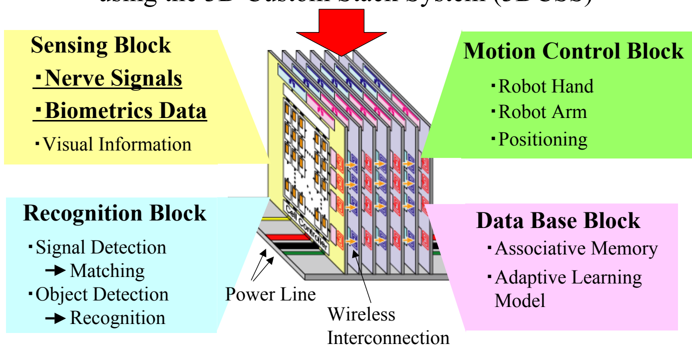
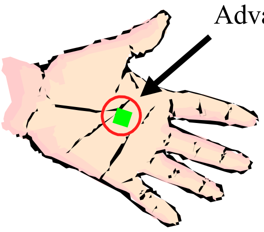
1. Introduction

Future Hyper Brain System
using the 3D Custom Stack System (3DCSS)



2. Objective



Advanced Human-Machine Interface

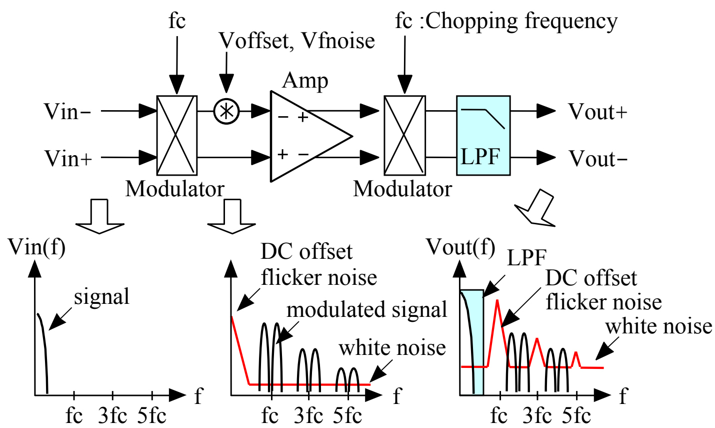
Low-Noise Analog Circuits

Sensing the Nerve Signals
(~50µVpp, ~5kHz)

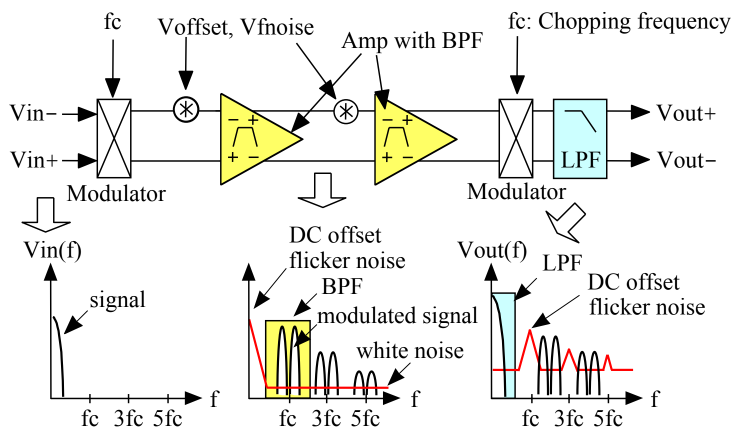
Sub-micron CMOS Process
+ speed
− flicker noise
− dc offset

Requirements for the low-noise amp:
- large bandwidth
- low noise and offset
- tolerance to process variation

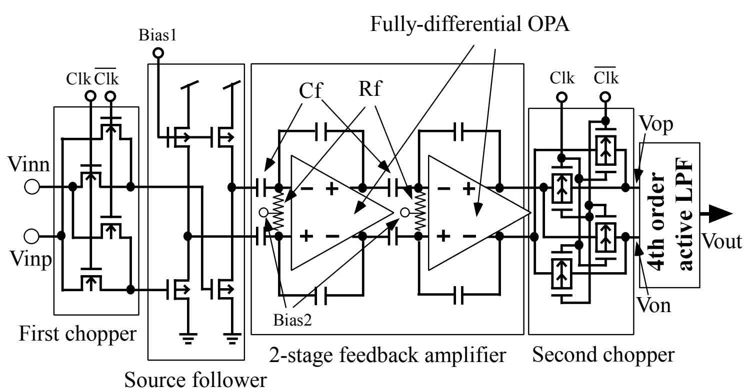
3. Principle of chopper amplifier



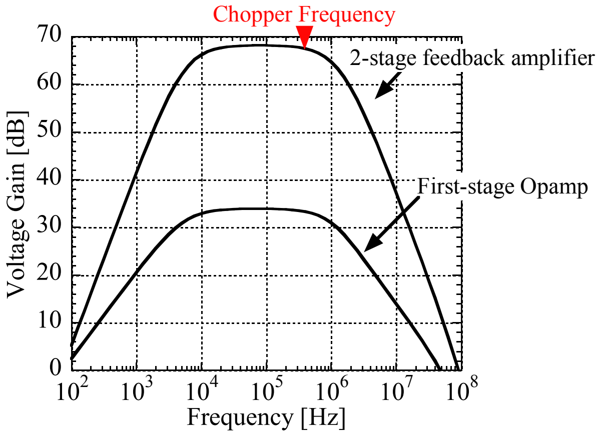
4. Our concept (low-noise chopper amplifier)



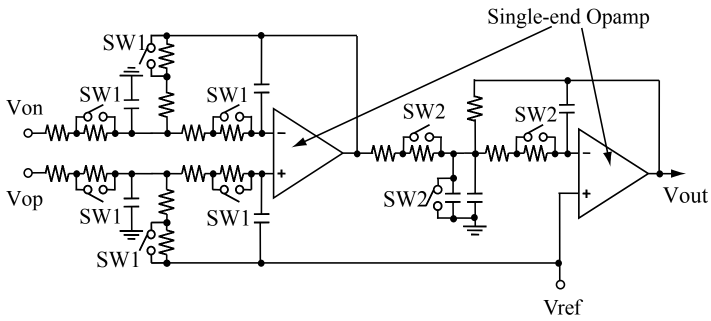
5. Low-noise chopper amplifier



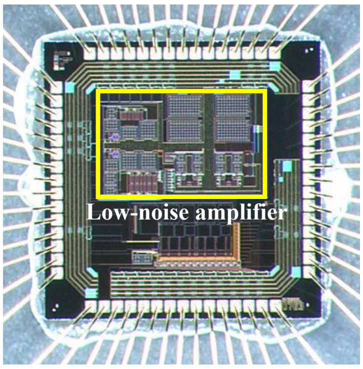
6. Frequency response of 2-stage feedback amp



7. 4-th order active LPF



8. Chip micrograph



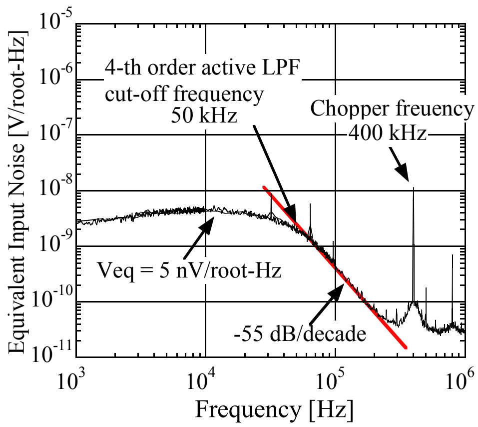
Technology

2-poly 3-metal
0.35-µm CMOS Process

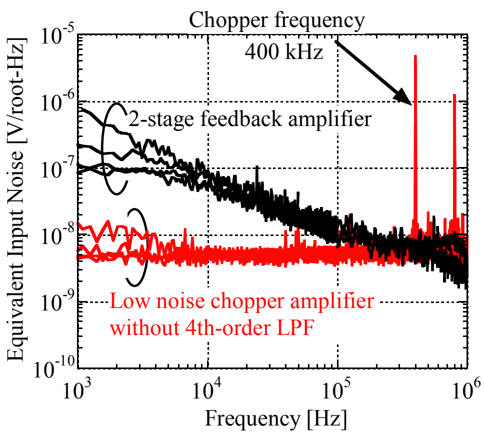
Chip area

1.5 x 1.0 mm^2

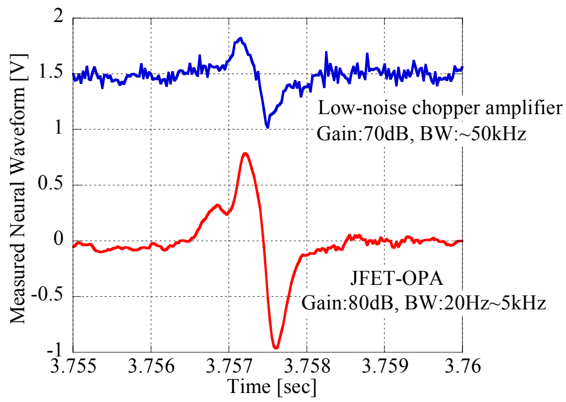
9. Equivalent input noise of low-noise amplifier



10. Deviation of noise PSD



11. Measured waveforms of a neural signal



12. Summary of measured characteristics

Process Technology	0.35μm CMOS
Supply voltage	3V
Power consumption	6mW
Chopping frequency	400kHz
Voltage Gain	70dB
Input equivalent noise	6nV/root-Hz
Deviation of noise floor	5nV/root-Hz
Total noise	1.3μV (~50kHz)
LPF bandwidth	50kHz
Chip area	1500μm x 1000μm

13. Summary

- Low-noise chopper amplifier is implemented
  - 2nd-order active BPF
  - 4th-order active LPF
- The chopper amplifier avoids process variation
  - Noise floor variation ~ 5nV/ $\sqrt{\text{Hz}}$
- The chopper amplifier achieves 6nV/ $\sqrt{\text{Hz}}$ noise and 6mW@3V power consumption