A TH-UWB Transmitter and its Pulse Generation Circuit for Intra/Interchip Wireless Interconnection

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1. Introduction

Steady downscaling of semiconductor device dimensions has been the main stimulus to achieve higher speed and performance of integrated circuits over the past decades. Unfortunately scaling has a reverse effects on interconnect delay associated with the parasitic R, L and C of conventional wiring. The introduction of low resistivity copper and low-permittivity (*k*) dielectrics can mitigate this problem. But the integration of these materials into integrated circuit fabrication is a complex task requiring material process and new techniques. Moreover it has also material limits due to chip area and minimal power requirements. New technology such as RF wireless interconnect using integrated antenna, transmitter and receiver is proposed for intra/interchip clock and data distribution [1, 2]. This future wireless interconnection essentially will form a local area network (LAN) as shown in Fig. 1 on a chip or among different chips. For high data transmission rate and multiple access capability of this wireless interconnection system, it requires wideband characteristics of each component [3]. A fully integrated time-hopped (TH)-UWB transmitter and its pulse generation circuit for wireless interconnection in future ULSI is developed and presented in this paper.

2. TH-UWB transmitter

The circuit schematic of time hopped UWB transmitter is shown in Fig. 2. TH-UWB transmitter first generates a typical time shifting or time hopped with pulse position modulation pulse and this pulse is then used to generate UWB signal. A typical UWB signal generated by the kth transmitter (i.e. k^{th} user or k^{th} chip) is given as [4]

$$s^k(t) = \sum w_{tr}(t - jT_f - c_j^{(k)}T_c - \Delta d^{(k)}_{[j/N_s]}) \qquad (1)$$

Where, $w_{tr}(t)$ represents the transmitted Gaussian monocycle, T_f is the frame time, c_j^k is the hopping number, T_c is the chip rate, Δ is the modulation time and d_j^k is data (0 or 1). Here the time shifted pulse train is generated from the frame clock. The multiplexer selects the time shifted frame clock which is generated by the voltage controlled oscillator(VCO), divider and delay line, according to PN (pseudorandom) sequence with three hopping bits (i.e hopping number c_j^k varies from 0 to 7). Here, eight channels are considered for initial investigation of the proposed system. Linear feedback shift register which consists of four clocked D-type Flip-Flop along with an exclusive-or logic as feedback is used to generate such PN sequence. The time shifting due to pulse position modulation (PPM) to encode data is done by the fine delay line which provides a delay of approximately the modulation time (0.05ns). Two to 1 multiplexer finally selects the time shifted pulse train due to PN sequence and PPM according to data symbol ("0" or "1"). The time shifted pulse train is then used to produce monocycle pulse with wide bandwidth by monocycle pulse (MCP) generator. It consists of RLC network with RC filter, pass gate and pulse generation circuit for generating the short rectangular pulse (SRP) and gate control pulse (GCP) [5]. The chip is fabricated using TSMC 0.18μm CMOS mixed signal process. The die microphotograph and chip layout is shown in Fig. 3a and Fig. 3b respectively. The Hspice simulation is done from extracted view of the layout and results are shown in Fig, 4. The performance of the transmitter is given in table 1.

3. Monocycle pulse measurement

The test chip of monocycle pulse (MCP) generator shown in Fig. 5 is designed and fabricated by using TSMC 0.18 μm CMOS mixed signal process. The die microphotograph of the circuit is shown in Fig.3. The MCP generation circuit occupies an area of $0.19mm^2$. The fabricated chip is bonded on a test PCB as shown in Fig. 6.

The measurement system consists of Agilent 81134A pulse pattern generator, infiniium digital oscilloscope and dc power supply. The SRP of width 0.1ns and GCP of width 0.5ns as shown in Fig. 7 are applied to MCP generator by using pulse pattern generator. Both applied pulses has equal rise and fall time of 70ps with a repetition rate of 400 MHz. The monocycle pulse is measured by infiniium digital oscilloscope and is shown in Fig. 8. The fig. 8 shows that the measured monocycle pulse is not symmetric because of low amplitude of negative part which may be due to the effect of high distributed parasitic resistance. The simulation also confirms this effect as shown in Fig. 9 where the black curve is the simulated monocycle pulse for the same inputs and without considering the effect of output pad buffer. The measured monocycle pulse width (1.13ns) as shown in fig. 8 differs from the desired pulse width of 0.5ns. This is due to the effect of low frequency buffer of the TSMC output pad. To investigate this effect, the monocycle pulse generator along with low frequency output buffer instead of TSMC output pad buffer is simulated. The simulation result as shown in red curve of fig. 9 depicts the same effect as found in measurement. The absence of asymmetric in this case is due to not considering the output buffer parasitic effect.

4. Conclusion

We developed and fabricated a single chip TH-UWB transmitter by using 0.18 μm CMOS technology and its performance is analysed by simulation. UWB transmitter pulse generator circuit which generates monocycle pulse is tested and measurement result is presented. The measurement results show that the monocycle pulse can be generated from RLC network along with RC filter and pass gate from the time hopped signal.

References

[1] A B M H Rashid, S Watanabe and T. Kikkawa, IEEE EDL, Vol.23, No.12, Dec 2002, p. 731-733.
[2] Brian A. Floyd, Chih-Ming Hung and Kenneth K.O. IEEE JSSC, vol 37, No. 5, May 2002, p. 543-552.
[3] P.K. Saha, N. Sasaki and T. Kikkawa, Proc. of IEEE ISSSTA'2004, Australia, p. 962-966.
[4] Moe Z Win and Robert A. Scholtz, IEEE Transactions on communications, vol 48, No. 4, April 2000, p. 679-691.
[5] P.K. Saha, N. Sasaki and T. Kikkawa, Extended Abstract of SSDM' 2004, Japan, p. 394-395.

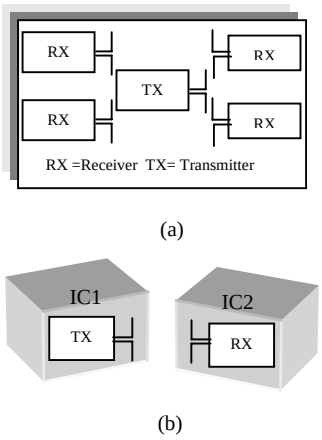

Fig. 1 Wireless interconnect system for future ULSI (a) Intrachip and (b) Interchip.

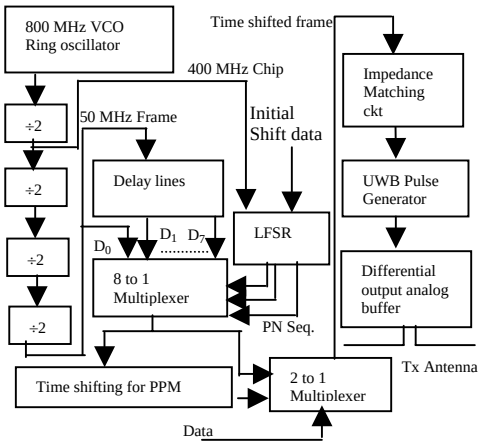

Fig. 2 TH-UWB Transmitter Schematic.

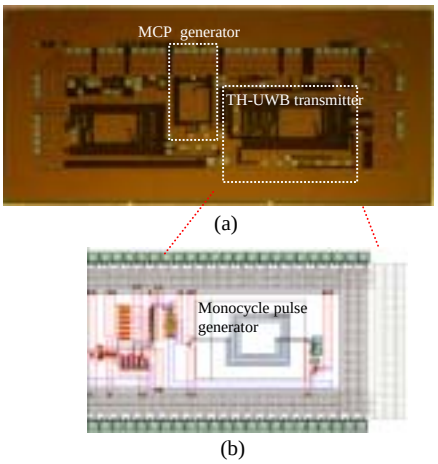

Fig. 3 (a) Die Microphotograph; (b) TH-UWB transmitter layout.

Table I: Transmitter performance data

UWB system	Time hopping Impulse
Carrier Frequency	No carrier
Transmitter Signal bandwidth	3.3 GHz
Data rate	50 Mbps
Single Channel datarate	400 Mbps
Modulation	Pulse position modulation
Average power consumption	12.5 mW
Architecture	All digital except pulse generator
Technology	TSMC 1.8v, 0.18 µm CMOS mixed signal process
Implementation	Single chip
Circuit Size	0.729 mm^2 (excluding antenna)
Application	Short distance (on chip wireless interconnection for future ULSI)

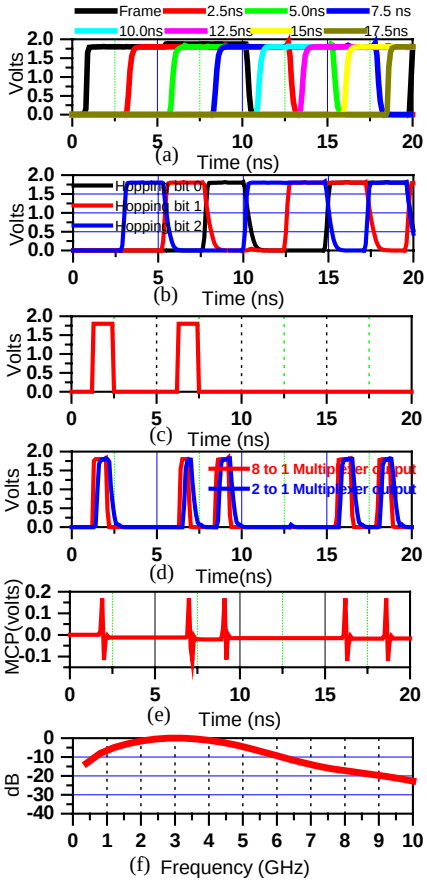

Fig. 4 Simulation output: (a) Delayed frame; (b) Three hopping bits; (c) RZ data [1 1 0 0 0] ; (d) Multiplexers output (e) Monocycle Pulse (MCP) train and (f) FFT of monocycle pulse.

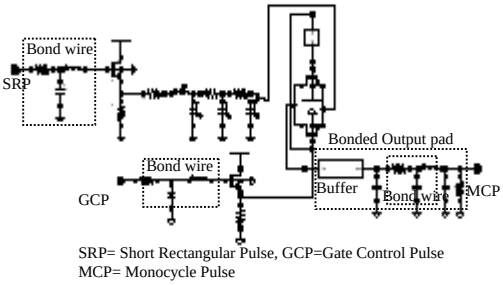

Fig. 5 Monocycle pulse generator with bonded wire and output pad buffer.

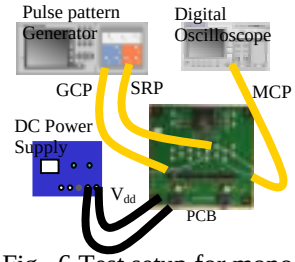

Fig . 6 Test setup for monocycle pulse generator.

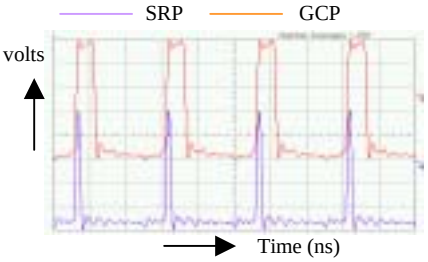

Fig. 7 Input pulses from pulse pattern generator to generate MCP.

Fig. 8 Measured Monocycle pulse.

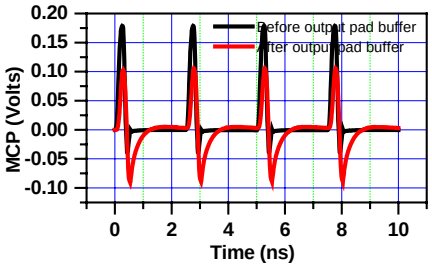

Fig. 9 Simulated monocycle pulse (considering bonded wire and output pad buffer).

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MOTIVATION

Advanced wireless interconnect system could be a solution for interconnect delay problem due to parasitic Resistance, capacitance and inductance in future ULSI

Wireless Interconnection

Tx=Transmitter, Rx=Receiver

Requirement

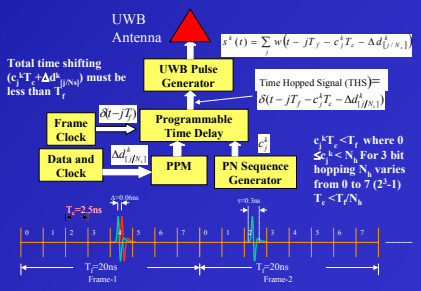
- High Data rate
- Multiple access

Shannon's channel Capacity theorem

$$C = B\log_2\left(1+\frac{S}{N}\right)$$

REQUIRE WIDEBAND Transmitter and Receiver

TH- UWB TRANSMITTER



$$s^k(t) = \sum_j w\left(t - jT_f - c_j^k T_c - \Delta d_{\{j/N_h\}}^k\right)$$

$$\delta(t - jT_f - c_j^k T_c - \Delta d_{\{j/N_h\}}^k)$$

UWB PULSE

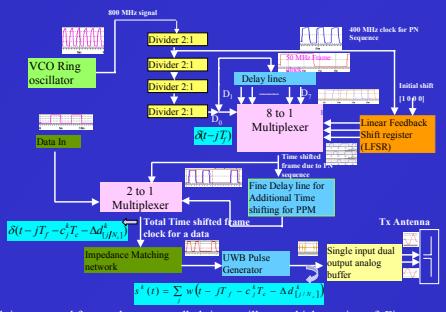
Monocycle pulse

$$w(t) = 5.84456\ A\frac{t}{\tau}e^{-2\pi\left(\frac{t}{\tau}\right)^2}$$

τ- Pulse Width

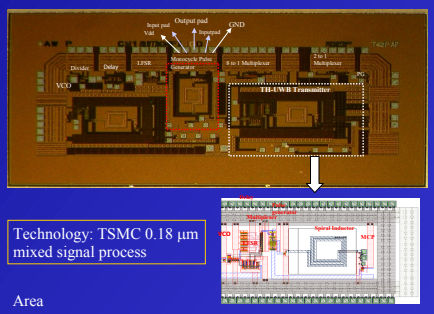
A –Amplitude

TH-UWB TRANSMITTER CIRCUIT SCHEMATIC



- Frame clock is generated from voltage controlled ring oscillator which consists of Five stage current straved inverter with transmission gate in series at each stage and divider .
- Frame clock is delayed through delay circuits.
- PN sequence is generated by Linear feed back shift register with Exclusive-or (XOR) as Feedback logic.
- Multiplexers is implemented using combinational logic gates.

CHIP MICROPHOTOGRAPH AND LAYOUT

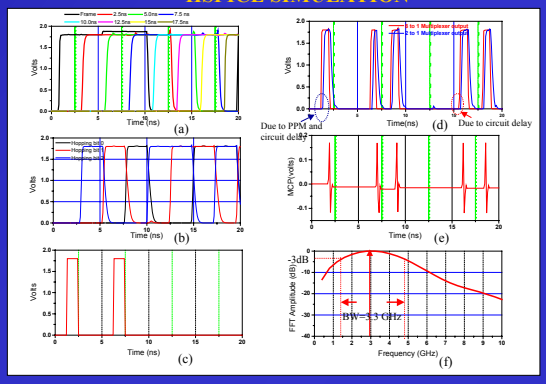


Technology: TSMC 0.18 µm mixed signal process

Area

UWB Transmitter 0.729 mm²
Monocycle pulse Generator: 0.19mm²

HSPICE SIMULATION



Simulation output: (a) Delayed frame; (b) Three hopping bits; (c) RZ data [1 1 0 0 0] ; (d) Multiplexers output (e) Monocycle Pulse (MCP) train and (f) FFT of monocycle pulse.

TRANSMITTER PERFORMANCE DATA

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Data Rate (Considering Eight Channel)	50 Mbps
Single Channel Data rate	400 Mbps
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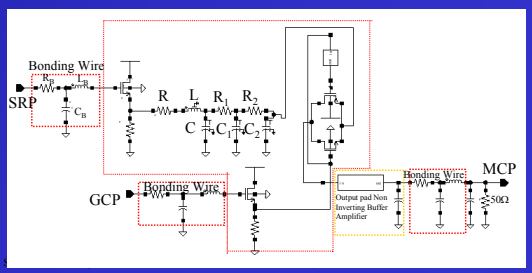
Average Power Consumption	12.5 mW
Architecture	All digital except pulse generation circuit
Technology	TSMC 1.8V, 0.18 µm CMOS Mixed Signal Process
Implementation	Single Chip
Circuit Size	0.729 mm² (excluding antenna)
Application	Short distance (On chip wireless interconnection for future ULSI)

MONOCYCLE PULSE GENERATOR



RLC network with RC filter produces damped sinusoidal signal (V_{osc}) from SRP

RLC network start oscillation for

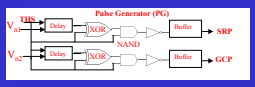
$$\frac{1}{LC} > \frac{R^2}{4L^2}$$

Frequency of Oscillation

$$f = \frac{1}{2\pi}\sqrt{\left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)}$$

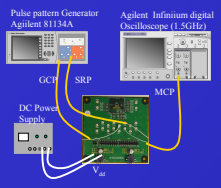
SRP and GCP are generated from Time hopped signal (THS) which contains information by pulse generator (PG) consisting of voltage controlled delay circuit, exclusive-or (XOR), NAND and inverter.

SRP AND GCP GENERATION CIRCUIT



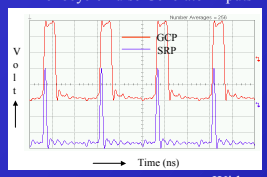
- Two identical circuit are used to produce SRP and GCP from THS
- Number of transistors required to generate SRP and GCP are same
- Thus delay due to parasitics RC will be same in both SRP and GCP generation
- No delay between SRP and GCP, rising time of both the pulses will be same.

MCP MEASUREMENT SETUP

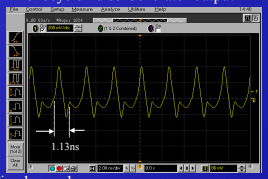


MEASURED MCP FOR A GIVEN INPUT PULSES

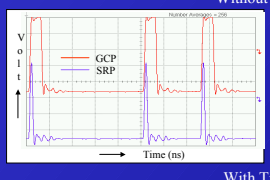
Monocycle Pulse Generator Inputs

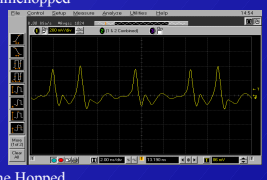


Monocycle Pulse Generator output



Without Timehopped





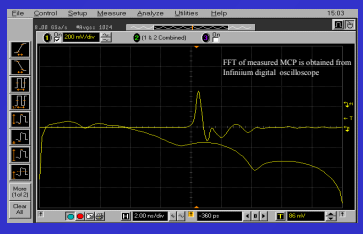
With Time Hopped

GCP- Pulse width 0.5ns, Rise and fall time ~70 ps

SRP-Pulse width 0.1ns, Rise and fall time ~70 ps

Measured Monocycle Pulse width=1.13 ns
Peak to peak amplitude 0.6V

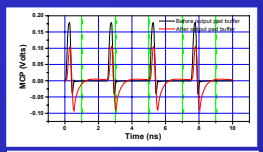
FFT of MEASURED MCP

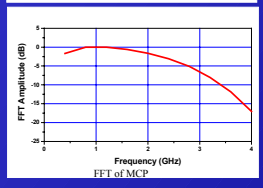


- Low amplitude of negative part of measured monocycle pulse may be due to the effect of high distributed Parasitic resistance .

- Increase of pulse width and asymmetric waveshape change the monocycle pulse center frequency to 0.8GHz.
- Increase of pulse width maybe due to low frequency buffer of the output pad and ground inductance.
- MCP generator along with non-inverting output buffer instead of TSMC output pad buffer is simulated.
- Simulation confirms that output pad buffer change the pulse width as found in measurement.

MCP FROM SIMULATION





FFT of MCP

CONCLUSIONS

- TH-UWB transmitter is designed and fabricated . Time hopped signal due to PN sequence and PPM is generated from time shifted frame. Time shifting is performed by delay circuit. Thus it is only necessary to keep constant delay with any variation of V_{dd} and substrate voltage.
- Monocycle pulse can be generated from RLC network with RC filter and Pass gate. The circuit can be implemented by using the current CMOS technology which led us to implement the UWB transmitter in a single chip.
- Pulse width of generated monocycle limits data rate of UWB transmitter because data rate is inversely proportional to the monocycle pulse width. Data rate can be increased by generating short monocycle pulse. This can be done by using low value of inductance in RLC network of MCP generator.

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