Single-Metal Tunable-Workfunction Technology with NiSi and Mo Gate Electrode

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1. Introduction

Metal gate technology is expected to solve the problem of poly-Si gate depletion. Since single gate material with dual-workfunction is required for the existing CMOS integration process, workfunction tuning technique for several metals has been extensively investigated. We have reported Mo workfunction tuning with nitrogen introduction at the last COE workshop [1]. This technique still has a trade-off problem between workfunction tunable range and device reliability [2-5]. As an alternative way for the workfunction tuning, we have investigated NiSi. It has been reported that fully silicided NiSi workfunction can be modulated by impurity pileup formed at $NiSi/SiO_2$ interface [6-10]. In this paper, the relationship between impurity depth profile and NiSi workfunction is described. In addition, an application of Nitrogen solid-phase diffusion (N-SPD) to Mo-gate MOSFET process is described.

2. Workfunction Tuning of NiSi Gate

Figure 1 shows the fully silicided NiSi gate MOS diode fabrication process flow. As illustrated in Fig. 2, implanted impurity in poly-Si is swept out toward the $NiSi/SiO_2$ interface during silicidation by the snowplow effect [11]. It is considered that the workfunction shift originates from electric dipoles formed at the $NiSi/SiO_2$ interface as shown in Fig. 3 [5]. The previously reported NiSi workfunction shift by using B, P, As, and Sb [6,7] is insufficient for CMOS application (Fig. 4).

In this work, we have investigated the dependence of NiSi workfunction on impurities and silicidation temperature. Silicidation was carried out at 400 ^{o}C, 450 ^{o}C, or 500 ^{o}C by in-situ lamp heating in a vacuum. The detailed conditions of impurity ion implantation and a brief summary of resulting flat-band voltage (V_{FB}) shift are listed in Table I. Sb, As, P, B, and Ge yielded flat-band voltage shift, in contrast to the cases of N and F. It is noteworthy that Ge, which is not a dopant for Si, gave rise to V_{FB} shift. This indicates that the NiSi workfunction could be modulated more widely with impurities other than dopants.

Figure 5 shows the N and F depth profiles after full silicidation at 500 °C. Though the slight impurity pileup at the $NiSi/SiO_2$ interface is observed, the V_{FB} shift was not obtained. Figure 6 shows the Sb depth profiles after full silicidation at various temperatures. The Sb pileup at the $NiSi/SiO_2$ interface silicided at 450 ^{o}C is larger than that at 500 ^{o}C. Sb peak formed by the implantation (observed at ~50 nm) vanishes at 450 ^{o}C. Lower silicidation temperature leads to lower silicidation rate, and hence increase in swept-out impurities by snowplow effect. The V_{FB} shift of -0.34 V was obtained at 400 ^{o}C and 450 ^{o}C. However, pileup growth results in impurity precipitation at the interface in the end. As shown in Fig. 7, partial film peeling was found after unreacted Ni removal with acid only for specimens silicided under 450 ^{o}C [10]. This is attributed to void formation at the $NiSi/SiO_2$ interface. This void formation was also observed for the sample with In [12]. Though the void formation mechanism is not clear yet, it is assured that impurity concentration in the vicinity of the interface is the key factor. This voiding should be noted as a potential roadblock against practical use of fully silicided NiSi gate.

2. Mo-Gate MOSFET

Figure 7 shows the Mo gate nMOSFET fabrication process flow. Though the obtained V_{FB} shift by N-SPD in MOS diode process was -0.45 V, that in MOSFET process was only -0.1 V, as shown in Fig. 8. Nitrogen EELS signals at the Mo/SiO_2 interface and the SiO_2/Si interface in both Mo MOS structures were evaluated to discuss the reason why the V_{FB} shift shrunk (Fig. 9). Nitrogen pileup at the Mo/SiO_2 interface in the diode process reduces by subsequent source and drain (S/D) activation annealing, in other words, by changing fabrication process to MOSFET process. Nitrogen depth profile obtained by back-side SIMS supports this result. These results indicate that the nitrogen pileup reduction due to the nitrogen redistribution in the Mo film causes the reversible workfunction behavior. Therefore, the Mo gate MOSFET fabrication process, especially thermal annealing, should be modified to control the nitrogen redistribution.

4. Summary

Workfunction tuning utilizing impurity pileup at the $metal/SiO_2$ interface has been investigated. It was found that silicidation temperature was an important factor to enhance the snowplow effect in NiSi. However, problems such as the void formation at the $NiSi/SiO_2$ interface and the interfacial reaction should be cleared. In the case of Mo-gate MOSFET with N-SPD, a reversible redistribution was observed by subsequent thermal treatment. Thus, the optimization of the fabrication process is required for workfunction tunable Mo-gate MOSFET.

Acknowledgements

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References

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- p-Si (100)
- LOCOS formation
- Gate oxidation(10 nm)
- poly-Si deposition(100 nm)
- **Impurity Ion Implantation**
  (N, F, B, P, Sb, Ge, In)
- Ni deposition(60 nm)
- **NiSi Full-Silicidation**
  (400, 450, 500 °C)
- Unreacted Ni removal
- Post metallization annealing

Fig. 1 Fabrication process flow of fully silicided NiSi gate MOS diodes.

Table I Impurity implantation conditions and resulting V_{FB} shift. Standard silicidation temperature was 500 °C.

	Dose (cm^{-2})	Energy (KeV)	ΔV_{FB} (V)
N	5.0×10^{15}	10	~ 0
F	2.5×10^{15}	10	~ 0
B	1.0×10^{15}	5	+0.1
P	5.0×10^{15}	15	-0.1
Sb	5.0×10^{15}	30	-0.3
Ge	5.0×10^{15}	30	-0.1
In	5.0×10^{15}	30	-0.1 ?

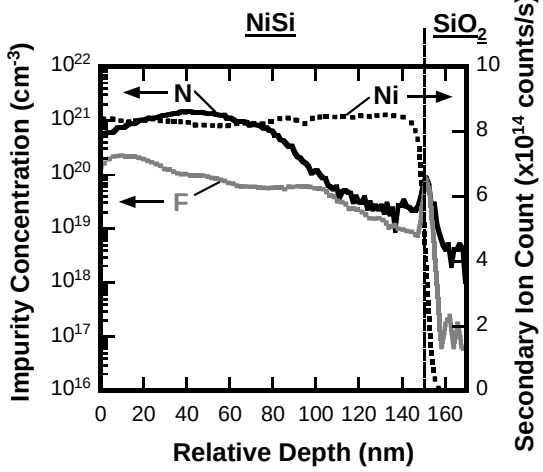

Fig. 5 N and F depth profiles measured by back-side SIMS. The slight impurity pileup at the NiSi/SiO_2 interface resulted in no V_{FB} shift.

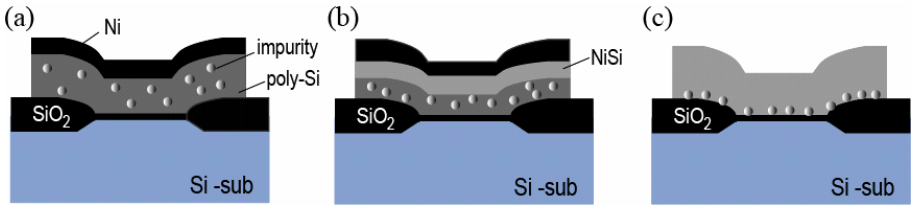

Fig. 2 Schematic illustration of impurity pileup formation at the NiSi/SiO_2 interface by the snowplow effect [11] (a) before, (b) in progress, and (c) after full silicidation.

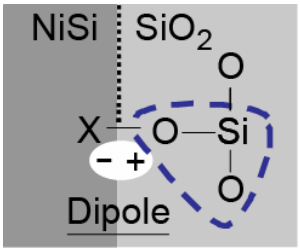

Fig. 3 Electric dipole model to explain workfunction shift at the NiSi/SiO_2 interfaces [5]. X stands for an impurity atom.

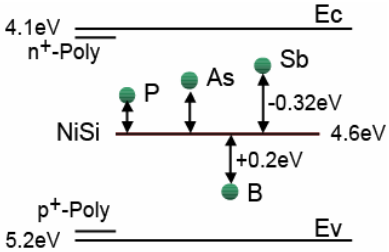

Fig. 4 NiSi workfunction tunable range. Drawn based on the data reported by Kedzierski *et al*. [6,7].

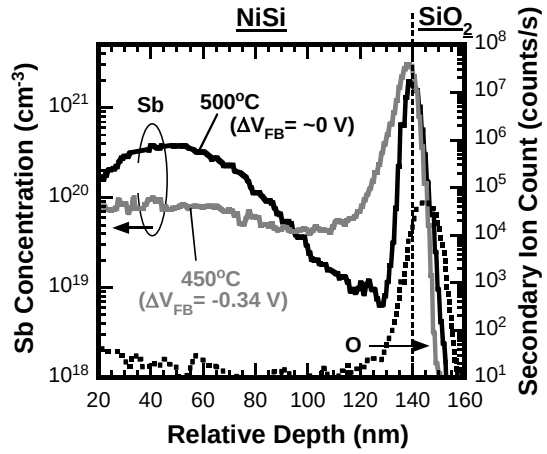

Fig. 6 Sb depth profiles measured by back-side SIMS. Lower silicidation temperature leads to a significant snowplow effect, resulting in larger V_{FB} shift.

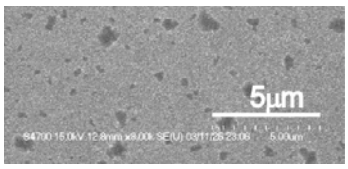

Fig. 7 Plan-view SEM micrograph of NiSi gate with Sb silicided at 450 °C. Partial NiSi peeling off was found after unreacted Ni removal process.

- p-Si (100)
- LOCOS formation
- Gate oxidation(5 nm)
- Mo and TiN sputter (50 and 30 nm)
- **Nitrogen Solid-Phase Diffusion**
  (800°C, 1min)
- TiN removal by dry etch
- S/D implantation
  (As : $5x10^{15}cm^{-2}$, 30keV)
- RTA for S/D activation (900°C, 1min)
- Al wiring and PMA

Fig. 8 Fabrication process flow of Mo gate nMOSFETs with N-SPD.

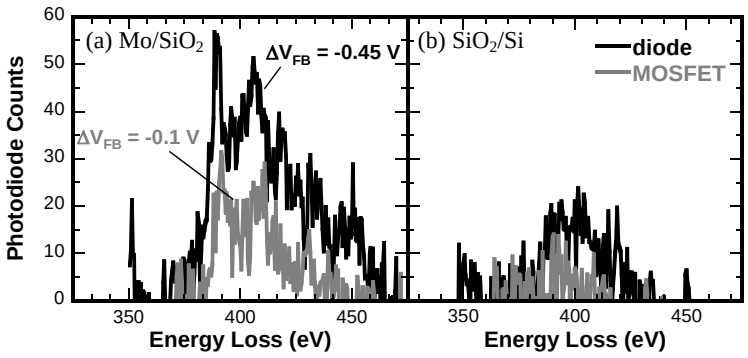

Fig. 9 Nitrogen EELS signals at (a) the Mo/SiO_2 interface and (b) the SiO_2/Si interface. In MOSFET process, S/D activation annealing reduces the nitrogen pileup formed by N-SPD, resulting in the less V_{FB} shift.

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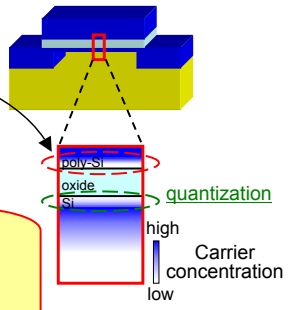
Motivation

- poly-Si Gate
  - **Gate depletion**
  - Effective oxide thickness increase
  - Solution : **Metal Gate**



Issue Dual Metal Gate for CMOS
(~4.1eV for nMOS, ~5.2eV for pMOS)
➡ **Complicated** fabrication process

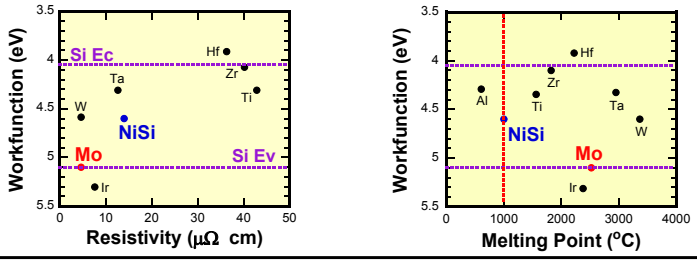
- **Requirement**
  - Workfunction-tunable gate with **single metal**

Properties of Metal Materials

Required Properties
- Stability at high temperature (>1000°C)
- Low resistivity
- Suitability for the conventional processes

➡ **Mo** and **NiSi**

Possibility of **Workfunction Tuning** ?



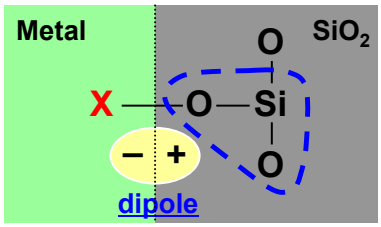
Workfunction Tuning Techniques

- **Fully Silicided NiSi** Gate
  - ► **Impurity pileup by snowplow effect**
    - W.P. Maszara et al., IEDM 2002
    - J.Kedzierski et al., IEDM 2002 & 2003
    - C. Cabral, Jr. et al., VLSI Symp. 2004
    - K. Sano et al., SSDM 2004
- **Mo** Gate
  - – N^+ Implantation
    - Q.Lu et al., VLSI Symp. 2001
    - T.Amada et al., MRS 2002
    - K.Shibahara, 2003 COE Workshop
  - ► **Solid-phase diffusion from TiN Film**
    - R.J.P. Lander et al., MRS 2002
    - M.Hino et al., SSDM 2003

Aim of this work
NiSi : Optimization of silicidation condition
Mo : Integration into MOSFET fabrication

Mechanism of Workfunction Shift

- Electric dipole and workfunction shift



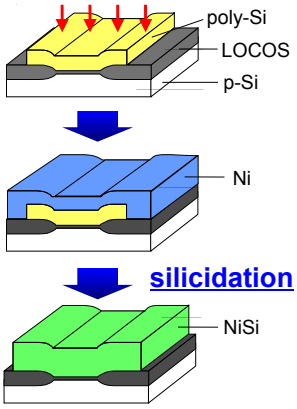
M.Hino et al., SSDM 2003

High density **electric dipole** formation by **impurities (X)** at the oxide interface
➡ **Workfunction shift**

NiSi-Gate MOS Diode Fabrication Process

- p-Si (100)
- LOCOS formation
- Gate oxidation (10 nm)
- poly-Si deposition (100 nm)
- **Impurity Ion Implantation**
  (N, F, B, P, **Sb**, **Ge**, **In**)
- Ni deposition (60 nm)
- **NiSi Full-Silicidation**
  (400°C, 450°C, 500°C)
  standard
- Unreacted Ni removal
- Post metallization annealing

Ion implantation



Workfunction Tuning of NiSi

Introduction of impurities in poly-Si

⇓ **Full-Silicidation**

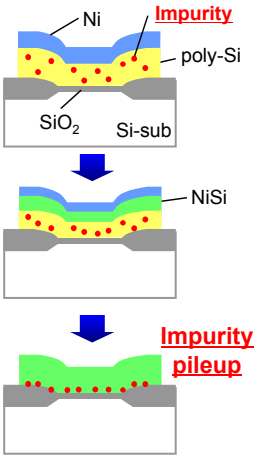
Impurities pileup at NiSi/SiO_2 interface by **snowplow effect**

⇓

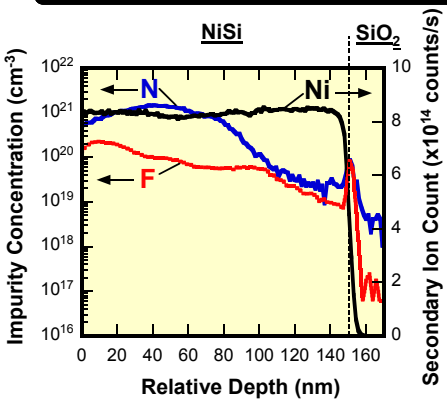
Workfunction shift

Snowplow effect

Segregation phenomenon due to silicidation reaction. Impurities at silicide/Si interface are swept out toward remaining Si.



NiSi gate with N or F



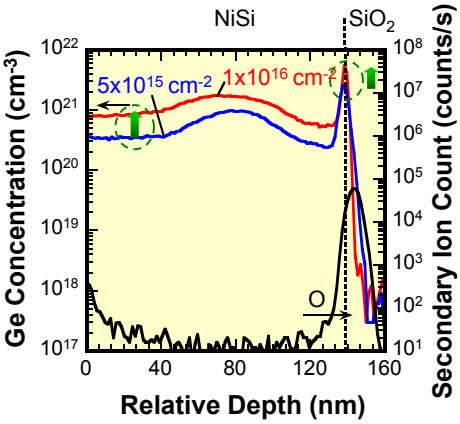
Slight Impurity Pileup at NiSi/SiO_2 interface

⇓

No V_{FB} shift

High-density impurity pileup is required

NiSi gate with Ge



Ge is not a **Dopant** for Si

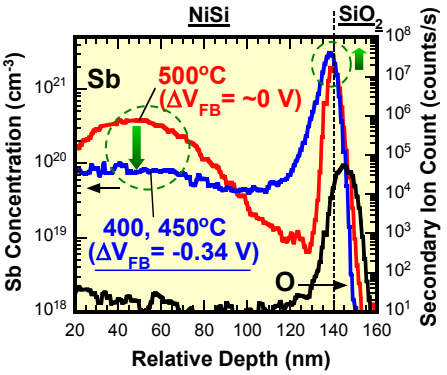
Dose (cm^{-2})	5 x 10^{15}	1 x 10^{16}
Pileup peak (cm^{-3})	2 x 10^{21}	5 x 10^{21}
ΔV_{FB} (V)	-0.10	-0.12

Increase in Ge pileup

⇓

not enough for V_{FB} shift

NiSi gate with Sb



Silicidation time

400˚C : **32 min**
450˚C : **25 min**
500˚C : 5 min

Lower silicidation temperature

⇓

Lower silicidation rate

Snowplow effect enhancement by slow silicidation ➡ **Large ΔV_{FB}**

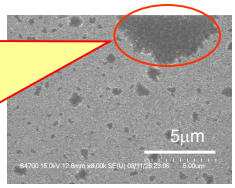
Issues of NiSi:Sb

NiSi peeling off for lower silicidation temperature

⇓

Void formation at oxide interface

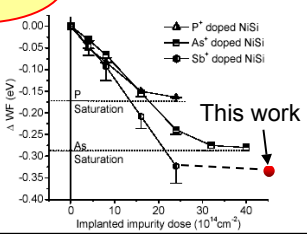
(also observed in **NiSi:In**)



plan-view SEM micrograph

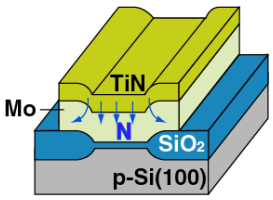
V_{FB} shift saturates with increasing impurity dose

Further V_{FB} shift : Difficult



Mo-Gate MOSFET Fabrication

- p-Si (100)
- LOCOS formation
- Gate oxidation (5 nm)
- Mo & TiN sputter (50 & 30 nm)
- **Nitrogen Solid-Phase Diffusion** (800˚C, 1min)
- TiN removal by dry etch
- S/D implantation (As : 5x10^{15} cm^{-2}, 30 keV)
- **RTA for S/D activation** (900˚C, 1min)
- Al wiring and PMA

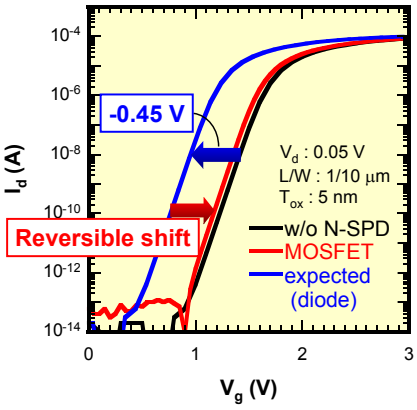


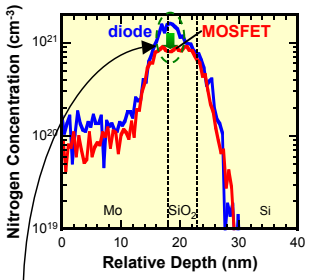
TiN/Mo-gate diode with N-SPD

⇓

ΔV_{FB} : -0.45 V

Workfunction shift in Mo-gate MOSFET

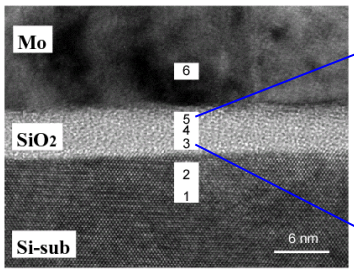




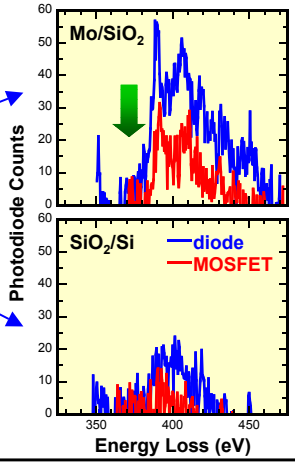
Nirtogen redistribution by S/D annealing

Reversible shift

Nitrogen Distribution (EELS)



Cross-section TEM micrograph



Summary

NiSi-gate

	N, F	As, P	B	Ge	Sb
ΔV_{FB} (V)	No	-0.1	+0.1	-0.1	400°C: -0.34 500°C: ~0

Ge is not a dopant for Si
➡ Chance for other impurities

Snowplow effect was affected by silicidation temperature

Issue : Void formation at $NiSi/SiO_2$ interface (also observed in NiSi:In)

Mo-gate MOSFET

Nirtogen redistribution by S/D annealing
➡ **Optimization of fabrication process**

Acknowledgement

This work was partly supported by STARC (Semiconductor Technology Academic Research Center).