Characterization of Atom Diffusion in Polycrystalline Si/SiGe/Si Stacked Gate

Hideki MURAKAMI, Yoshikazu MORIWAKI, Masafumi FUJITAKE, Daisuke AZUMA, Seiichiro HIGASHI and Seiichi MIYAZAKI

Graduate School of Advanced Sciences of Matter, Hiroshima University, Kagamiyama 1-3-1, Higashi-Hiroshima 739-8530, Japan
Phone: +81-82-424-7648, Fax: +81-82-422-7038, E-mail: hideki@hiroshima-u.ac.jp

1. Introduction

In the aggressive scaling of the gate dielectric thickness for continuous shrinkage of MOSFETs, a increase in the gate resistance emerges as one of major concerns from the viewpoint of eliminations in both the voltage drop through the gate under higher gate leakage current [1] and the gate depletion effect [2]. Especially, in case of poly-Si gate, with decreasing gate size, the gate depletion effect becomes serious due to dopant loss reflecting impurity pile-up [3]. Poly-SiGe gate is one of the promising candidate for a gate material of next-generation MOSFETs because of lower resistivity and less depletion effect [3–5] in comparison with poly-Si gate in addition to the consideration about controllability of work function and matching with conventional silicon process [6,7]. In the implementation of poly-SiGe gate, the control of the redistribution of Ge atoms in a gate stack structure during dopant activation anneal is of great importance.

In this work, we have studied the thermal diffusion and redistribution of Ge atoms in the poly-Si/poly-SiGe/poly-Si stacked structures.

2. Experimental

After conventional wet-chemical cleaning steps of p-type and n-type Si(100) wafers, SiO_2 layers in the thickness range of 2.0-4.0nm were grown at 1000°C in dry O_2 and then poly-Si/SiGe/Si/SiO_2 stacked structures were fabricated on the wafers by the following low-pressure chemical vapor deposition (LPCVD) steps at a substrate temperature of 570°C. First, ∼30nm-thick poly-Si as a buffer layer was formed from the thermal decomposition of pure SiH_4 under 0.36torr and subsequently, ∼100nm thick poly-SiGe was deposited under 0.42torr of a pure SiH_4 and 10%GeH_4 diluted with He, in which the gas molar ratio of SiH_4 to GeH_4 was varied from 2 to 10, and followed by LPCVD of ∼100nm thick poly-Si film as a cap layer with the same conditions as the buffer layer. BF_2^+ ions or As^+ ions accelerated at 30keV or 15keV were implanted with a dose of 5×10^{15}cm^{-2} to the stack structures so prepared and followed by activation annealing in the temperature range of 800∼1000°C for 30 or 10 min in N_2 ambient. The crystallinity of the stacked film was evaluated by X-ray diffraction(XRD) using a Cu Kα line and Raman scattering measurements using a 441.6nm light from a He-Cd laser. The depth profiles of Ge, Si and dopant atoms in the stack structures were evaluated by secondary ion mass spectrometry(SIMS) using Cs^+. The resistivity measurements for the annealed samples were performed using a four-point probe method. Also, the gate leakage current and capacitance-voltage characteristics of fabricated MOS capacitors were evaluated to check the influence of the Ge redistribution on the gate oxide.

3. Results and Discussion

XRD measurements for 250nm-thick $Si_{1-x}Ge_x$ single film formed on 2nm-thick SiO_2 confirm an improvement of the crystallinity by post deposition anneal and no significant different in the crystallinity between the annealed samples as shown in Fig. 1. The relative intensity of the diffraction peaks due to (111), (220) and (311) planes indicates that polycrystallites are oriented preferentially to the (111) direction, but not strongly, and the preferential orientation is not changed by N_2 anneal subsequent to ion implantation at the temperature range of 850-1000°C . In 850°C annealed cases, the BF_2^+ implanted sample show a slightly degraded crystallinity in comparison with undoped and As^+ implanted samples. This can be interpreted in terms of a negative impact of implanted fluorine atoms on the crystallization, presumably because of thermal stability of Si-F bonds. Changes in the Raman scattering spectra for poly-Si(100nm in thickness)/poly-$Si_{0.7}Ge_{0.3}$(100nm)/poly-Si(30nm) /SiO_2(2nm)/Si(100) show the diffusion and incorporation of Ge atoms in the Si layer by N_2 anneal as represented in Fig. 2. For as-deposited sample, two sharp peaks due to TO phonons involving Si-Si stretching motions in the poly-Si cap and in the poly-SiGe layers are clearly observable at ∼520cm^{-1} and ∼505cm^{-1}, respectively, where the signals from the bottom poly-Si layer can not be detected because of the probing depth of the excitation laser light. After 850°C anneal, the TO phonon peaks are shifted towards the lower wavenumber side. The observed peak shift implies the diffusion of Ge atoms into the poly-Si cap layer. Since, for the BF_2^+ implanted case, the TO phonon peak at the higher wavenumber side is significantly decreased, the Ge incorporation to the cap is likely to be more pronounced than the As^+ implanted case. Notice that, by N_2 anneal at 1000°C, the signals from TO phonons in Si-Ge network becomes dominant, suggesting that Ge atoms diffuse uniformly in the cap layer as also confirmed by SIMS measurements. As shown in SIMS profiles for BF_2^+ implanted case of Fig. 3, the Ge concentration in the cap layer is increased remarkably by 850°C anneal. Obviously, by 1000°C anneal, a quite uniform depth profile for Ge atoms is obtained. In addtion, for the As^+ implanted case, the same result was obtained.

Lower resistivities were measured for poly-SiGe annealed at temperatures higher than 850°C in comparison to the cases of poly-Si (Fig. 4), which can be interpreted interms of the impurity activation ratio.

Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MOS capacitors with n^+ and p^+ poly-SiGe stack structures on 4nm-thick SiO_2 were compared to those of controlled MOS capacitors with poly-Si gate in order to confirm less impact of the Ge redistribution in the stack gate on gate SiO_2 in the annealing condition at 850°C for 30min (Fig. 5, 6). For the cases with n^+ gate, no difference in flat-band voltage(V_{FB}) between poly-Si and poly-SiGe gates was observed. The result of Fig. 5 indicates that, by 850°C for 30min, Ge atoms are diffused well near the interface between the buffer layer and SiO_2. As for I-V characteristics of the MOS capacitors, the gate leakage current due to Fowler-Nordheim(F-N) tunnel is only observed, indicating the impact

of Ge redistribution in the gate stack on the gate leakage is negligible(Fig. 6). In addition, for p^+ poly-SiGe gate, an increase in current level at positive gate voltages, which reflect the V_{FB} shift of 0.2V, is measured compared with the p^+poly-Si gate case, while no difference in the leakages current level at negative gate biases is obtained because the tunneling current is limited by hole generation rate in the substrate. For n^+ poly-Si and poly-SiGe gates, the I-V characteristics are almost identical, and this result was consistent with the C-V characteristics.

4. Conclusions

The Ge redistribution in the poly-SiGe stack structure, which consists of 100nm-thick poly-Si cap, 100nm-thick poly-SiGe and 30nm-thick poly-Si buffer, on ultrathin SiO_2/Si(100) by N_2 anneal in the temperature range of 800-1000°C has been studied. By 1000°C anneal for 30min, a uniform depth profile of Ge atoms throughout the whole sack structure was obtained. By 850°C anneal for 30min, expected I-V and C-V characteristics of MOS capacitors with p^+ and n^+ poly-SiGe stack gate with a Ge content of ∼30at.% were confirmed. The flat band voltage shift of 0.2V was evident only for p^+ poly-SiGe, being attributable to the difference in the energy band structure between Si and $Si_{0.7}Ge_{0.3}$, without extra current leakage.

References

[1] H. Murakami, T. Mihara, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. Vol. 41 No. 5A (2002)pp. L512-L514.
[2] W-C. Lee, T-J. King and C. Hu, IEEE Electron Dev. Lett. 20(5)(1999)pp. 9-11.
[3] K. Uejima, T. Yamamoto and T. Mogami, IEDM Tech, Dig., (2000) p. 445.
[4] C. H. Chen, Y. K. Fang, C. W. Yang, S. F. Ting, Y. S. Tsair, C. N. Chang, T. H. Hou, M. F. Wang, M. C. Yu, C. L. Lin, S. C. Chen, C. H. Yu, M. S. Liang, Solid-State Electronics 46 (2002) pp. 597-599.
[5] Y. H. Kim, S. J. Kwon, K. J. Chun and J. D. Lee, Jpn. J. Appl. Phys. Vol. 33 (1994) pp. 2468-2473.
[6] Y. V. Ponomarev, C. Salm, J. Schmitz, P. H. Werlee, P. A. Stolk and D. J. Gravesteijn, IEDM Tech, Dig,. (1997) pp. 829-832.
[7] W-C. Lee, T. J. King and C. Hu, Symp. VLSI Tech. (1998) pp. 190-191.
[8] M. Chandrasekhar, H. R. Chandrasekhar, M. Grimsditch and M. Cardna, Phys. Rev. **B22** (1980) pp. 4825-4833.

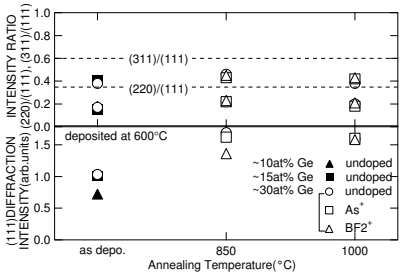


Fig. 1: The (111) peak intensity measured by XRD and the intensity ratio of (220) and (311) peaks to the (111) peak for as-deposited poly-$Si_{1-x}Ge_x$(100nm, x=0.1, 0.15 and 0.3)/SiO_2(2nm)/Si(100) formed by LPCVD at 600°C and annealed samples of x=0.3 after As^+ or BF_2^+ implantation. The annealing time was 30min. The dashed lines denote the relative intensity ratio for (220) and (311) peaks with respect to the (111) peak or the random orientation case as observed in powdered c-Si.

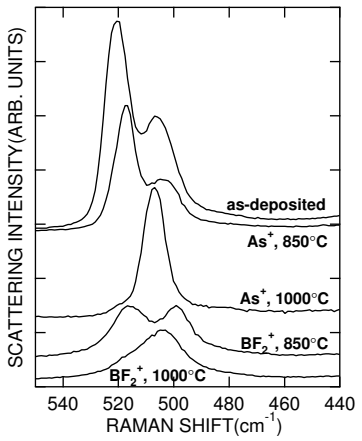


Fig. 2: Raman scattering spectra of as-deposited and N_2 annealed samples of poly-Si/SiGe/Si/SiO_2 stacked structures. The Ge concentration in the poly-SiGe layer before ion implantation was 30 at.%. The peak around ∼520cm^{-1} and the peaks in the region 510∼500cm^{-1} are attributable to Si-Si TO phonon modes in Si layer or Si-rich regions and Ge-incorporated region, respectively.

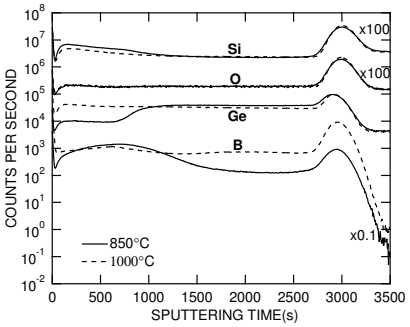


Fig. 3: SIMS profiles for the N_2-annealed sample after BF_2^+-implantation shown in Fig. 2, which were measured by using O_2^+ ions.

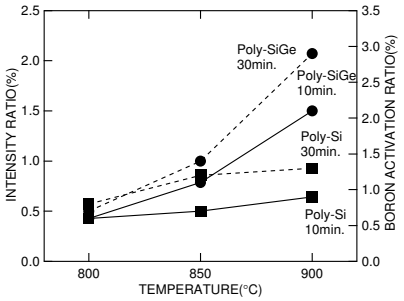


Fig. 4: The resistivity of the samples shown in Fig. 6 measured using a four-point probe.

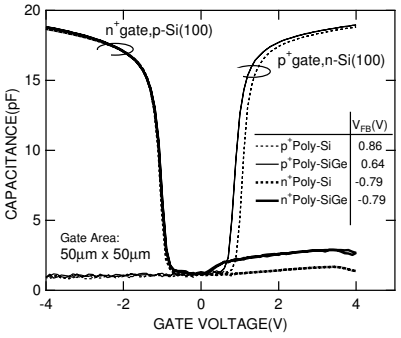


Fig. 5: C-V characteristics of MOS capacitors with poly-SiGe and poly-Si gates, which were measured at 100KHz. The N_2 anneal after As^+ implantation was performed at 850°C for 30min.

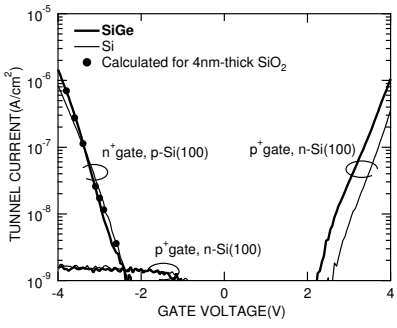


Fig. 6: I-V characteristics of MOS capacitors shown in Fig. 5.

Background

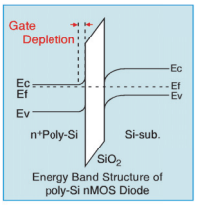
Scaling of the Gate Dielectric Thickness for MOSFETs

Gate resistance is crucial factor.

- Potential Drop in the Gate under High Gate Leakage Current
- Gate Depletion Effect

Major Problems in Poly-Si Gate

- Gate Depletion Effect
  W-C. Lee et al., IEEE Electron Dev.Lett. (1999)
- High Resistance in turns of Redistribution of Impurity in Gate Electrode
  H. Murakami, et al., Jpn. J. Appl. Phys. (2002)



Energy Band Structure of poly-Si nMOS Diode

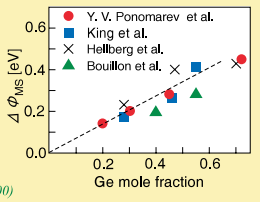
Promising candidate for a gate material of next-generation MOSFETs

- Poly-SiGe Gate

Poly-SiGe Gate

- Lower resistivity
- Less depletion effect
- Controllability of work function by tuning of Ge concentration
- Matching with conventional silicon process

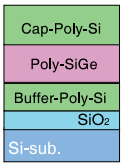
Y. V. Ponomarev IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 4, (2000)



Research Concern : Diffusion of Germanium Atoms

This Work

Thermal Diffusion and Redistribution Evaluation of Ge and Impurity atoms in the Poly-Si/Poly-SiGe/Poly-Si/SiO_2 Stack Structures



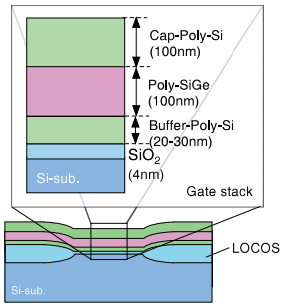
Poly-Si/Poly-SiGe/Poly-Si/SiO_2 Stack Structure

Poly-SiGe Gate Stack Formation Process

Substrate : p-Si or n-Si 8-12Ω-cm

- LOCOS Formation
- Gate Oxidation (4nm)
- Buffer Poly-Si Deposion
  SiH_4, 570℃, 0.36Torr
- Poly-$Si_{1-x}Ge_x$ Deposion (x～0.3)
  SiH_4+GeH_4, 570℃, 0.36Torr
- Cap Poly-Si Deposition
  SiH_4, 570℃, 0.36Torr
- Ion Implantation
  As^+ : 30keV $5E^{15}$ions/cm^2
  BF_2^+ : 15keV $5E^{15}$ions/cm^2
- Anneal
  N_2,800-1000℃ 30minutes
- n^+Poly-SiGe Gate / p^+Poly-SiGe Gate) MOS Capacitors

Evaluation of Ge and Impurity atoms Diffusion after Dopant Activation Anneal

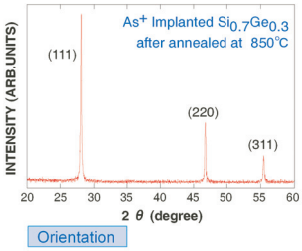


Evaluated Method

- Surface Oxidation(10%H_2O_2) / Etched Back(1%HF)) 1nm/cycle 50times
- Measurement（each 50nm）
  - Four-point probe method → The Resistivity in each etching stage
  - Secondary Ion Mass Spectroscopy (SIMS) / Raman Scattering Measurements) The Depth Profile of Ge and Impurity atoms
  - X-ray Diffraction → Crystallinity

- Energy Dispersive X-ray Analysis(EDX) → The Spatial Distribution of Ge atoms
- The Gate Leakage Current and Capacitance-Voltage Characteristics → The Influence of the Ge Redistribution

XRD Analysis of Annealed Poly-SiGe Layer



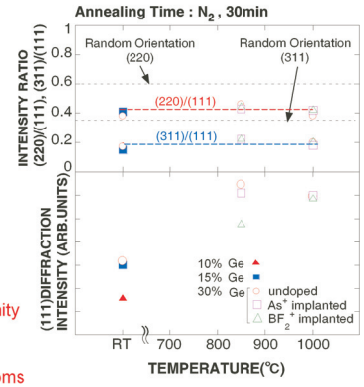
Orientation

- No change with annealing
- (111) Oriented

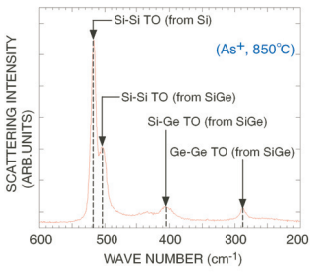
Crystallinity

- 850℃,B dope ⇒ Low crystallinity

Negative impact of implanted F atoms

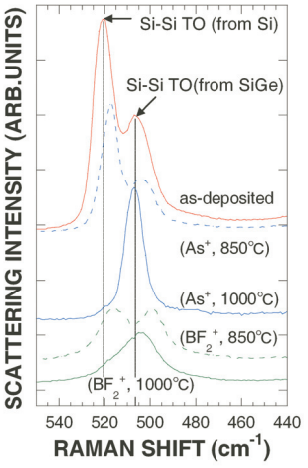


Raman Spectra for Poly-SiGe Stacked Structure

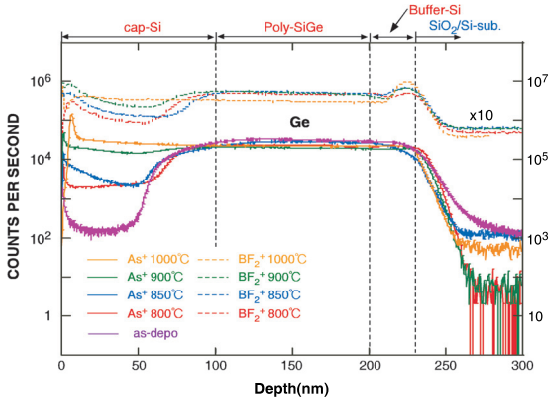


- 850℃ Anneal
  Si-Si TO(from Si)⇒Shift to lower wavenumber
- 1000℃ Anneal
  Si-Si TO(from SiGe) factor is dominant

Ge atoms diffusion into cap-poly-Si layer

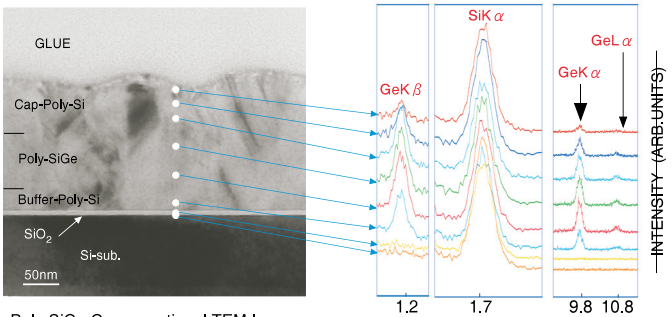


Evaluation of Ge Atoms Diffusion in poly-SiGe Gate Stacked Structure by SIMS



- Ge atoms diffused to the surface of poly-Si cap layer at 800℃ anneal.
- Ge atoms diffuse uniformly into the cap layer at over 900℃ anneal in As^+ implanted sample and at 1000℃ anneal in BF_2^+ implanted sample.

Depth Profile of Ge atoms in poly-SiGe Gate Stacked Structure by EDX

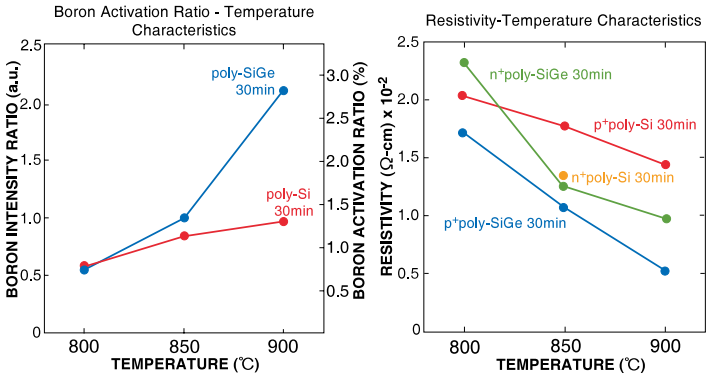


Poly-SiGe Cross-sectional TEM Image after 800℃ 30min Anneal

Characteristic X-rays Spectra of Si and Ge

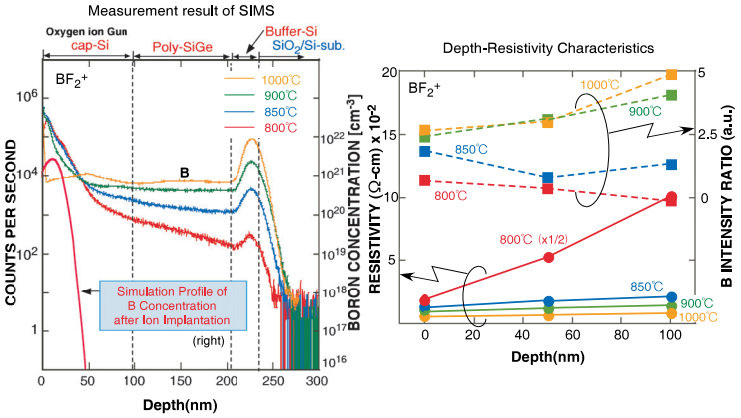
- Ge atoms in the gate SiO_2 layer were not detected, and Ge atoms diffused to the surface of the poly-Si cap layer at 800℃ 30min anneal.

Anneal Independence of Boron Activation Ratio and Resistivity



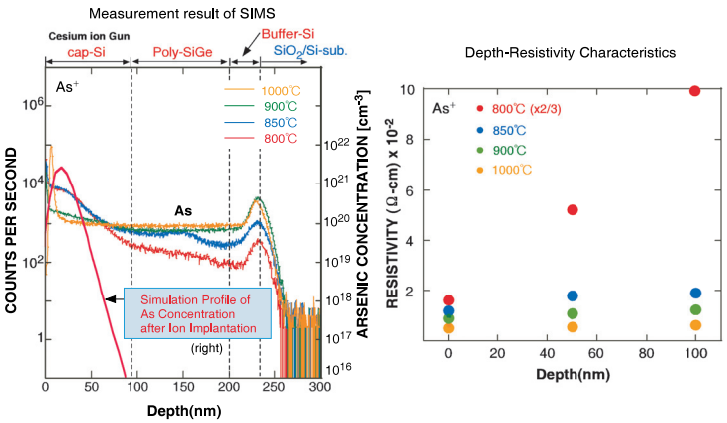
- For the case of BF_2^+ implanted sample, the resistivity decrease by 40% at 850℃ anneal case and higher B activation ratio was obtained in poly-SiGe case in comparison with the poly-Si case.
- In the case of As^+ implanted, there is no difference in As activation ratio, since there is no difference in the resistance between poly-Si and poly-SiGe.

Depth Profile of B atoms and Resistivity in p+poly-SiGe Gate



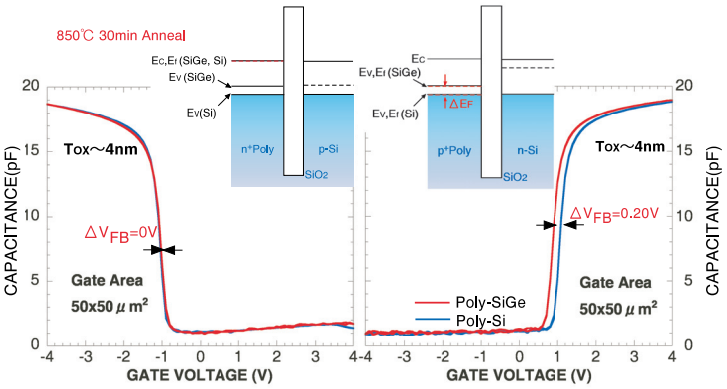
- B atoms diffused almost uniformly in the cap layer at more than 850℃ anneal and the results was consistent with the activation ratio and resistivity.

Depth Profile of As atoms and Resistivity in n+poly-SiGe Gate



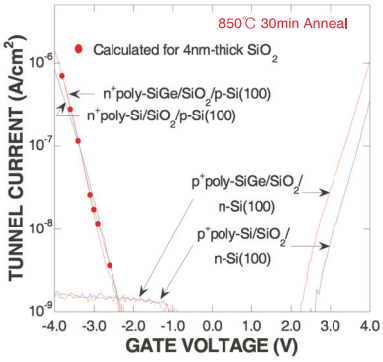
- As atoms diffused almost uniformly in the cap layer at more than 850℃ anneal and the results was consistent with the activation ratio and resistivity.

Capacitance-Voltage Characteristics of MOS Capacitors with Poly-SiGe Gate



The decrease in flat-band voltage of 0.2V for p^+ poly SiGe gate is attributable to the energy shift of the valence band edge

Current-Voltage Characteristics of MOS Capacitors with Poly-SiGe Gate



- The impact of Ge redistribution in the gate stack on the gate leakage is negligible.
- For p+ poly-SiGe gate, an increase in current level at positive gate voltages reflect the Flat-band voltage shift of 0.2V.

Summary

- Ge atoms were not detected in the SiO_2 layer and reach near the top surface through the cap layer at 800℃ 30min anneal by EDX and SIMS.
- In the case of BF_2^+ implanted, resistivity decrease at over 850℃ anneal and for 40% at 850℃ anneal in poly-SiGe case compared with the poly-Si case. Impurity atoms is distributed almost uniformly in the cap layer at over 850℃ anneal according to depth profile by raman scattering measurements, SIMS and EDX and also resistivity correspond to the result.
- By 850℃ anneal for 30min,expected I-V and C-V characteristics of MOS capacitors with p^+ and n^+ poly-SiGe stack gate were confirmed.