Local Electronic Transport through Si Dot with Ge Core as Detected by AFM Conductive Probe

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1. Introduction

Characterization of electron charging and discharging of nanometer-size Si dots is primarily of concern to realize single electron transistors [1] and quantum dot floating gate MOS memories [2]. To control the electron storage in the dots and enhance the carrier confinement, the introduction of Ge core into Si dots [3] is thought to be a promising way. Recently, we have demonstrated that an AFM/Kelvin probe technique enables us to characterize the electronic charged states of pure nanometer Si dots [4] and Si dot with Ge core [5] on SiO_2/Si(100) through the surface potential changes caused by electron injection and emission. The surface potential images after electron injection and emission confirms the injected electrons are located in the Si clad while holes are stably retained in the Ge core, which can be interpreted in term of the energy band profile expected for the Si/Ge/Si system.

In this work, to gain a better understanding of electronic transport through the dots consisting of the Si clad and the Ge core, we have extended our research to the investigation of the local electronics transport through the Si dot with Ge core on ultrathin SiO_2 layer.

2. Experimental

Si dots with Ge core (~25nm in average dot diameter) were prepared on ~2.5nm-thick SiO_2 by highly selective low-pressure chemical vapor deposition (LPCVD) [3]. First hemispherical single-crystalline Si dots with an areal density of ~$1.5x10^{11}$ cm^{-2} were grown on OH-terminated SiO_2 using pure SiH_4. Subsequently, Ge deposition was performed on pregrown Si dots/SiO_2 at 400°C using 5% GeH_4 diluted with He and then followed by Si cap deposition under a SiH_4 pressure of 0.02Torr at 540^{o}C. High-resolution TEM, XPS and AFM measurements were carried out to confirm the formation of Si dots with Ge core. Using a Rh-coated Si_3N_4 cantilever, topographic and local electric transport were measured simultaneously with a contact AFM mode in clean room ambient at room temperature. A dc voltage was applied between the cantilever and Al-evaporated back side of the Si(100) substrate and the current flowing through the sample to the cantilever was registered to render the current images.

3. Results and Discussion

Distinct current images correlated with the topographic images are obtained in both bias polarities as demonstrated in Fig. 1. Notice that a unique polarity dependence of the current image is observable. When a negative bias is applied to the tip, current images in which lower current flows through the central part of the dot than through other regions. In contrast to this, for positive bias conditions, the current flow through the central part of the dot becomes significantly high and a clear image contrast is obtained between the central and the peripheral regions in each dot, which is associated with the presence of Ge core in each Si dot. The current-voltage characteristics for the dots, which are derived from the current images, show an exponential increase in the current level through the central part of the dot at positive biases above +1V as shown in Fig. 2. The current contrast at the negative bias conditions is attributable mainly to the change in the distance between the tip and the substrate. A unique current contrast

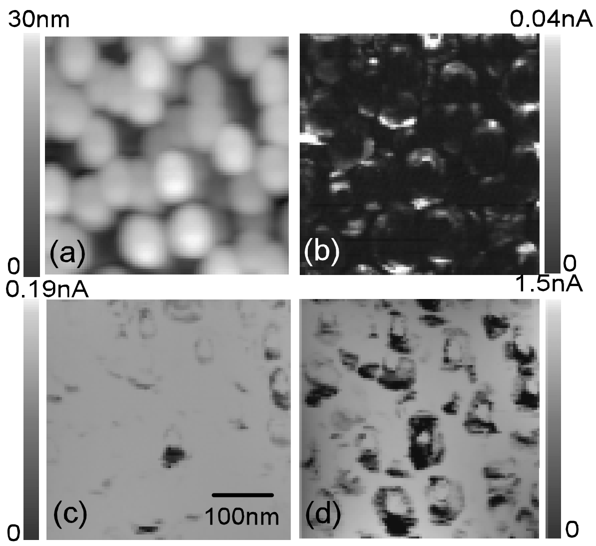

Fig. 1. An AFM topographic image (a) and corresponding current images for tip bias –3V(b), +2V(c) and +3V(d).

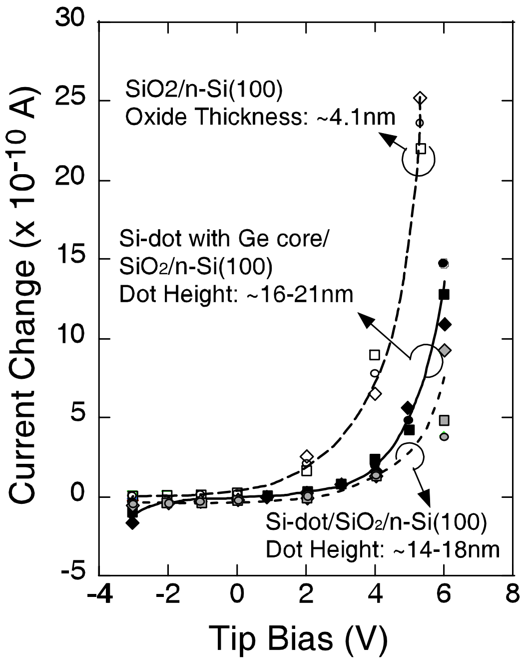

Fig. 2. Current-voltage (I-V) characteristics for Si dots with and without Ge core derived from corresponding current images.

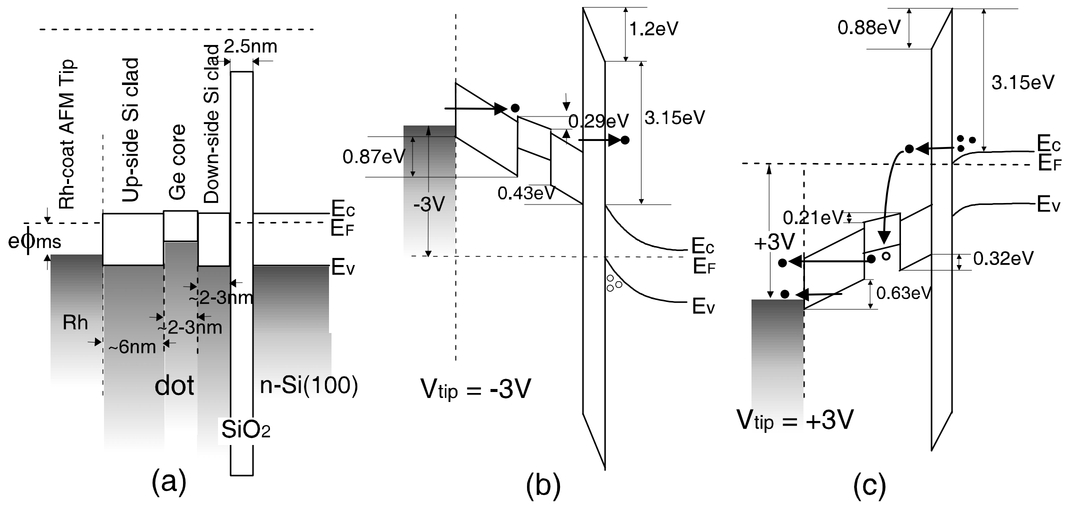

Fig. 3. Ideal energy band profile at the flat band condition (a), and after applying Vdc = -3 and +3V to the AFM tip.

obtained at the positive bias conditions can be interpreted in terms that the emission of valence electrons from the Ge core plays an important role to enhance the current level. If we ignore the structural strain and compositional mixing at the Ge core/Si clad interface, an energy band profile in which the Ge core acts as a fairly deep well for holes and the Si clad as a shallow well for electrons as schematically illustrated in Fig. 3 (a). Since the Fermi level of Rh is located at ~0.1eV above the Si valence band edge for the case that surface states of the Si clad are negligible, the electron emission over the potential barrier height at the Rh/Si clad interface or hole tunneling from the substrate through the underling SiO_2 seems to be rate-limited in the current flow even at the negative tip bias as high as -3V (Fig. 3(b)). Under the positive bias conditions, valence electron(s) can be extracted from the Ge core as confirmed from the surface potential changes in the previous work [5] (Fig. 3(c)). Considering that the inversion region of the Si substrate is formed at biases higher than +1V, it is likely that electron tunneling through the underling SiO_2 from the substrate is more pronounced by holes generated in the Ge core.

4. Conclusion

In conclusion, we have demonstrated that, for dots consisting of the Ge core and the Si clad on ultrathin SiO_2/Si(100), the presence of the Ge core is detectable from the bias dependent contrast in the current image. Valence electron can be extracted from Si clad and Ge core, holes accumulated into Ge core can recombine with electrons tunneling through the bottom oxide.

References

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[2] S. Tiwari. E. Rana, H. Hanafi, A. Hartstein, E. E. Crabb and K. Chan: Appl. Phys. Lett. **68** (1996) 1377.

[3] Y. Darma, H. Murakami and S. Miyazaki, Jpn. J. Appl. Phys. **42** (2003) 4129.

[4] K. Takeuchi, H. Murakami and S. Miyazaki, Abst. of intern. Semicond. Technol. Conf. (2002 Tokyo) No. 33

[5] Y. Darma, K. Takeuchi and S. Miyazaki, Extended Abst. of Int. Conf. Solid State Devices and Materials (2003,Tokyo), p. 300.

Local Electronic Transport through Si Dot with Ge Core as Detected by AFM Conductive Probe

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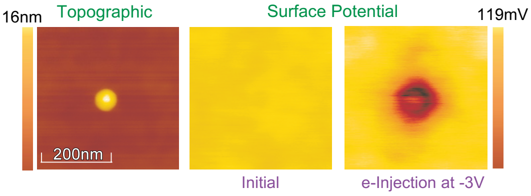
Abstract

Spherical nanometer Si dots with Ge core have been prepared by alternately controlling the selective growth conditions in LPCVD using pure SiH_4 and GeH_4 on ultrathin SiO_2.
The distinct current images through Si dots with Ge core have been measured using conductive AFM probe in both bias polarities.
From the current images taken with conductive AFM probe, current level through the dots with Ge core is enhanced in comparison with pure Si dot due to the generation and collection of the holes in the Ge core.
Under the positive bias condition, valence electrons can be extracted from Si clad and Ge core, resulting in the generation and collection of holes in the Ge core, and accumulated holes can recombine by electron tunneling from the Si substrate through the bottom SiO_2 layer.
For the negative tip bias, current is rate-limited by electron tunneling through the bottom oxide from the conduction band of Si clad rather than electron injection from the tip to the Si clad.

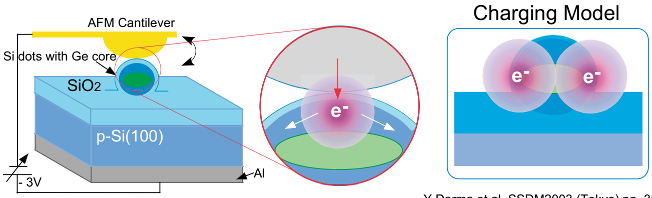
Background & Motivation (I)

From the AFM/Kelvin Probe Measurement of Si Dot with Ge core

Electron Injection → Electron retained at Si Clad



Charging Model



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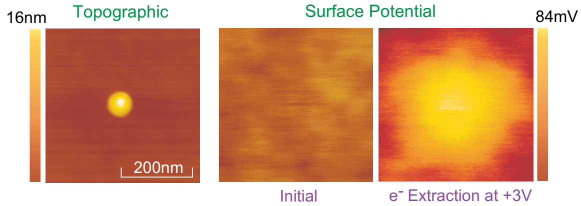
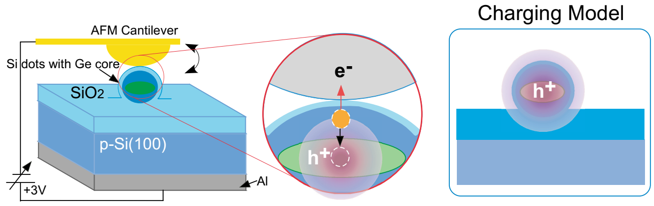
Background & Motivation (II)

Electron Extraction → Holes retained in Ge core



Charging Model



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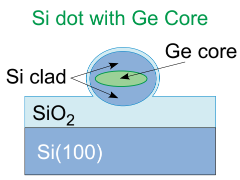
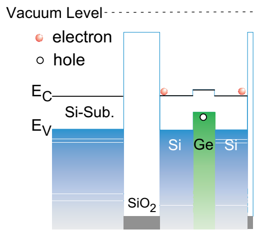
Background & Motivation (III)

Simplified Energy Band Diagram of Si Dot with Ge Core





Si Clad → shallow potential well for electron

Ge core → deep potential well for hole

This work

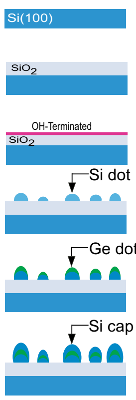
To gain a better understanding of electrical property of Si dots with Ge Core Structure

Characterization of Local Electronics transport of Si Dot with Ge Core

Experimental

Formation of Si Dot with Ge Core

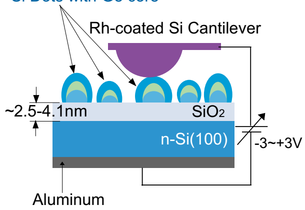
- Precleaned HF-last: $NH_4OH:H_2O_2:H_2O$=0.15:3:7; 80°C,10min and 4.5% HF 2min
- Oxidation: 2% O_2, 1000°C, 10min
- Surface Modification: 0.1% HF, 2min; Pure water 60s
- Dot Formation by LPCVD
  - Si-Dot: 100% SiH_4, 560°C, 0.5Torr, 60s
  - Ge-Core: 5% GeH_4, 400°C, 0.2Torr, 3min
  - Si-Cap: 100% SiH_4, 540°C, 0.02Torr, 30s



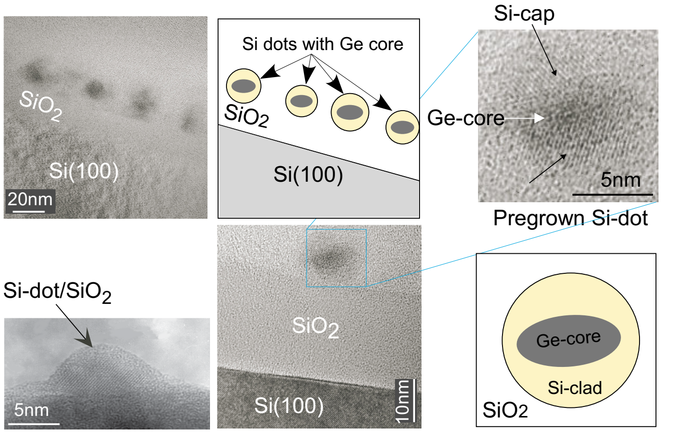
Electronic Transport Characterization using AFM

Topography and corresponding current images measurements

AFM/contact Mode:



Cross-Sectional TEM images of Si Dots with Ge core



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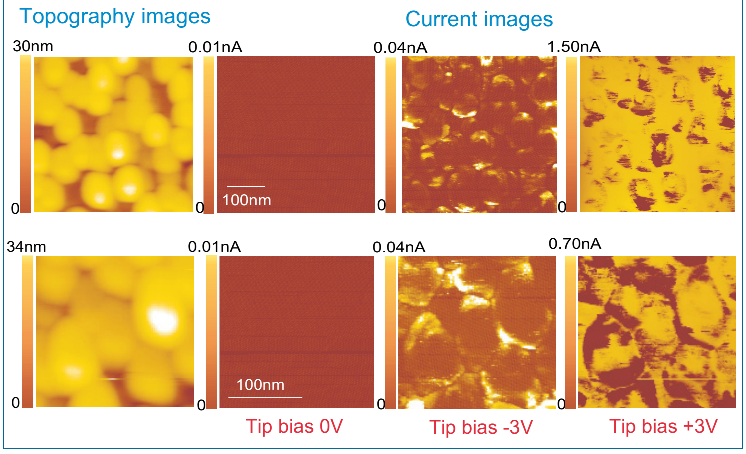
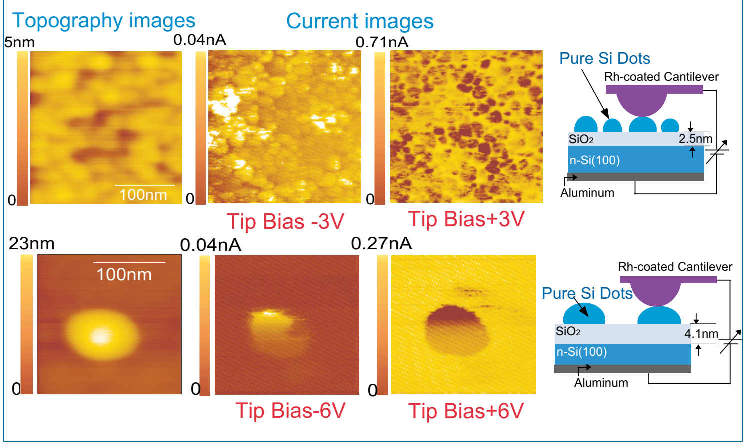
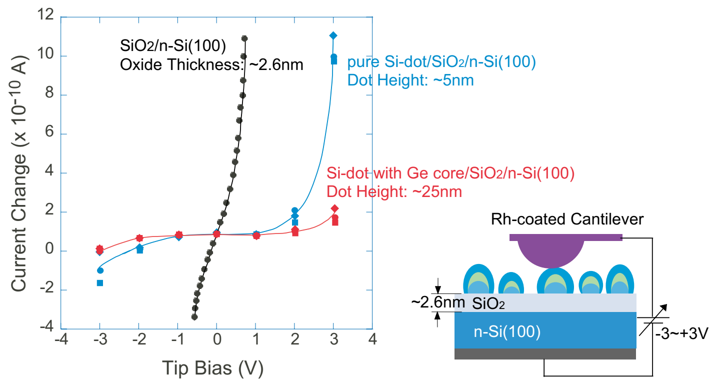
Topography and Coressponding Current Images through Si Dots with Ge core Using Conductive AFM Probe



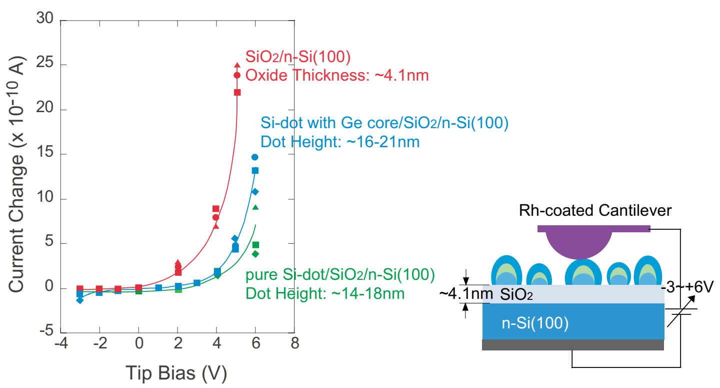
Topography and Current Images through Pure Si Dots Using AFM Conducting Probe



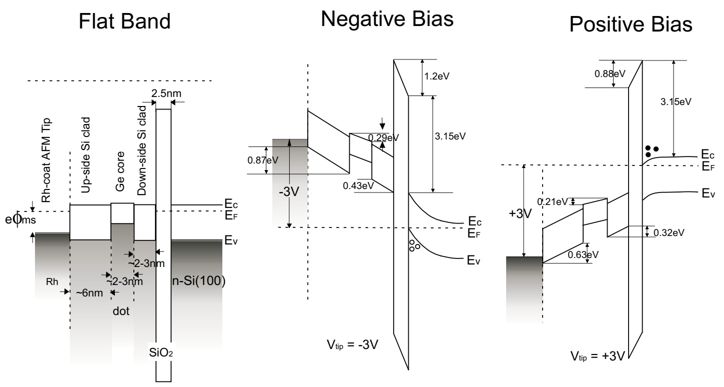
I-V Characteristics Derived from Corresponding Current Images Using AFM Conducting Probe Measurement



I-V Characteristics Derived from Corresponding Current Images Using AFM Conducting Probe Measurement

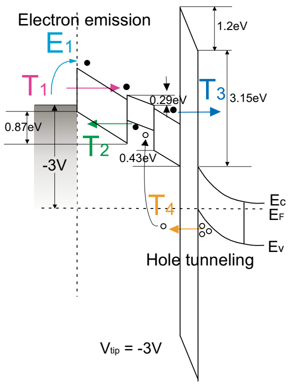


Ideal Energy Band Profile of Si Dots with Ge core

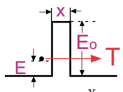


Schematic Electronic Transport at Negative Tip Bias

Negative Bias



$T_1 > T_2 > T_3 \gg E_1 > T_4$



$$T = T_o \, Exp\left[\left(\frac{-2}{\hbar}\sqrt{2m}\int_0^{X_o}\sqrt{(E_o(x) - E)}\,.dx\right)\right]$$

$$E = E_o \, Exp\left(\frac{E_o(x) - E}{kT}\right)$$

Electrons

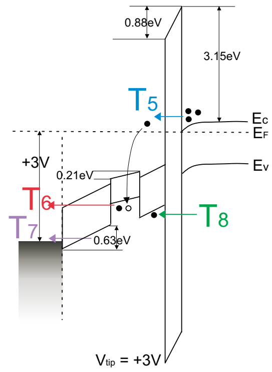
- $E_1 \sim 5.20 \times 10^{-16}$
- $T_1 \sim 2.33 \times 10^{-11}$
- $T_3 \sim 1.03 \times 10^{-12}$

Holes

- $T_2 \sim 1.24 \times 10^{-11}$
- $T_4 \sim 5.44 \times 10^{-17}$

Schematic Electronic Transport at Positive Tip Bias

Positive Bias



$T_7 \gtrsim T_6 > T_5 \gg T_8$

Electrons tunnelling

- $T_5 \sim 3.37 \times 10\text{-}13$

Holes generation

- $T_6 \sim 6.80 \times 10^{-11}$
- $T_7 \sim 4.15 \times 10^{-10}$

Holes Tunneling

- $T_8 \sim 6.04 \times 10^{-15}$

Summary

- The presence of the Ge core is detectable in the current images taken by conductive AFM probe.
- For the negative tip bias, current is rate limited by electron tunneling through the bottom oxide from the conduction band of Si clad rather than electron injection (tunnelling and/or thermionic emission) from the tip to the Si clad.
- Under positive bias conditions, valence electron can be extracted from Si clad and Ge core, holes accumulated into Ge core can recombine with electrons tunneling through the bottom oxide.

Acknowledgement

We would like to thanks Prof. Seiichiro Higashi and Mr. Hideki Murakami for their help and suggestion.