Electrical characterization of HfAlOx/SiON dielectric gate capacitors

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1. INTRODUCTION

Continual device scaling requires high-k gate dielectric as the replacement of conventional silicon oxide gate dielectric to suppress the gate leakage current with an allowable level. HfAlOx is considered to be the most promising candidate for high-k gate dielectric, especially for low standby-power devices because of its good thermal stability and the permitivity of 15 [1-2]. In this paper, we focused on HfAlOx/SiON stacked gate dielectric and evaluated the electrical properties.

2. EXPERIMENT

HfAlOx films were deposited by ALCVD (atomic layer CVD) with the thickness range of 3~7nm on 300mm P-Si(100) (~10ohm) substrate, and followed by the series of post-deposition anneals at 800^0C for 5sec, 900^0C for 5sec and 1000^0C for 1sec in 0.2% O_2 ambient diluted by N_2. The Hf/(Hf+Al) is 0.3 measured by XPS. The oxynitride interfacial layer (~1.2nm) was formed by oxidation at 850^0C in NO_2/H_2 ambient followed NH_3 annealing at 700 ^{0}C. MIS capacitors with $HfAlO_x$ (ε=14)/SiON(ε=4.6) stack dielectric gate (EOT= 1.9, 2.5, 2.84nm) were fabricated with diameter 0.5mm aluminum electrode deposited by thermal evaporation. The electrical characterization of HfAlOx/SiON dielectric gate capacitors was performed by I-V and C-V techniques.

3. RESULTS AND DISCUSSION

3.1 CHAEGE TRAPPING CHARACTERISTICS

The I-V curves were dawn after interrupting the negative voltage stress. As showed in Fig.1, in low field region (>-3v) the gate leakage current of capacitor with 3nm-thick $HfAlO_x$ was increased after constant voltage stress at –3.8V, which is analogous to the stress induced leakage current (SILC) in silicon oxide induced by the trap assisted tunneling process [3-4]. However, in high field region (<-3v), the decrease of leakage current was induced, which is usually attributed to electron trapping in HfAlOx layer [3]. To confirm the origin of the current decrease, the time dependence current under constant voltage stress was measured as shown in Fig.2. The decrease of current was observed, which support the electron-trapping model.

The variation of fixed oxide charge response to flat band shift as a function of stress time was extracted from HF(1KHz) C-V curves before and after constant voltage stress at same electrical field about 3.9MV/cm in $HfAlO_x$ layer. From Fig.3, the stress time was normalized with T_{BD} (breakdown time), it was found that net-positive charges of ~0.6×10^{12}/cm^2 were decreased by constant voltage stressing for the case with 3nm-thick HfAlOx. In contrast, for the case with 5nm and 7nm HfAlOx, net-positive charges of ~2×10^{11}/cm^2 and ~1×10^{12}/cm^2 respectively were increased. It is generally considered that the flat band shift were mainly because of exist fixed positive charges in interfacial layer. The trend different of the flat band shift can be explained with the competition of positive charge trapping and detrapping. For the case with 3nm thick HfAlOx, the detrapping process is dominant while the trapping process due to anode hole injection is dominant for the case with 5~7nm HfAlOx.

3.2 CRITICSL ELECTRICAL FIELD STRENGTH OF SOFT BREAKDOWN

The measured I-V characteristics for the capacitor with 5nm-thick HfAlOx were shown in Fig.4, where the gate voltage was ramped up and down by 20mV step for each cycle of voltage scan to a maximum value. Two distinct degradation modes were observed, being quite similar to SILC (> Voxi) and soft breakdown (SBD) (at Voxc) observed in ultra-thin silicon oxide [5]. The Fig.5 showed the soft breakdown field determined at 63% of cumulative failures as a function of HfAlOx thickness. It was found that the soft breakdown electric field in the interfacial SiON layer reaches to be as high as 10~13MV/cm, and that in HfAlOx were estimated to be only 3~4MV/cm. Since the estimated breakdown electric field in HfAlOx is less than two thirds of theoretically-predicted breakdown field [6], it is likely to be more pronounced that the dielectric breakdown of the stack structure is controlled by the breakdown of SiON rather than HfAlOx.

3.3 TDDB CHAEACTERISTICS

The Weibull distributions were showed in Fig.6, where the time to breakdown was normalized by maximum value. It was found that the weibull slope was increased as increasing high-k layer thickness. This result implies that the dielectric stack reliability was improved by increasing of the high-k layer thickness. The Weibull slope is higher than 1.8, which is comparable to the case of ultra-thin silicon oxide.

4 CONCLUSIONS

The charge trapping characteristics after negative constant voltage stresses were interpreted in term of the composite effect of three components: neutral trap generation, electron trapping, and positive charge generation in the gate stacks. Critical electrical field strength from SILC to soft breakdown was confirmed to be 3~4MV/cm for HfAlOx and 10~13MV/cm for SiON respectively. It is indicated that the stack dielectric breakdown is controlled by the interfacial layer (SiON). Reliability of this stack dielectric gate was evaluated by TDDB characteristics. The weibull slopes are higher than 1.8, which dependence on the thickness of high-k layer.

5 REFERENCES

1 Manisha Kundu, Noriyuki Miyata, Yukinori Morita, and Tsuyoshi Horikawa, Appl. Phys. Lett. 86, 5326(2004),

2 Riichiro Mitsuhashi,k Kazuyoshi Torii, Hiroshi Ohji, , Solid stage devices and materials(SSDM), 34(2004).

3 Zhen Xu, Michel Houssa, Richard Carter, J. Appl. Phys. 91, 10127 (2002).

4 M.Houssa, A.Stesmans, M.Naili, M.M.Heyns, Appl. Phys. Lett. 77, 1381(2000),

5 Wataru Mizubayashi and Seiichi Miyazaki, JJAP, 43, 6925(2004),

6 J.McPherson, J-Y.Kim, A.Shanware, and H.Mogul, Appl. Phys. Lett. 82, 2121(2003).

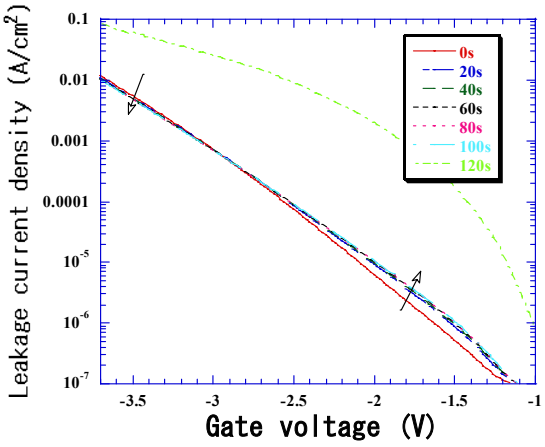

Fig.1 the gate leakage current as a function of gate voltage before and after constant voltage stress at –3.8v for MIS capacitor with 3nm HfAlOx layer

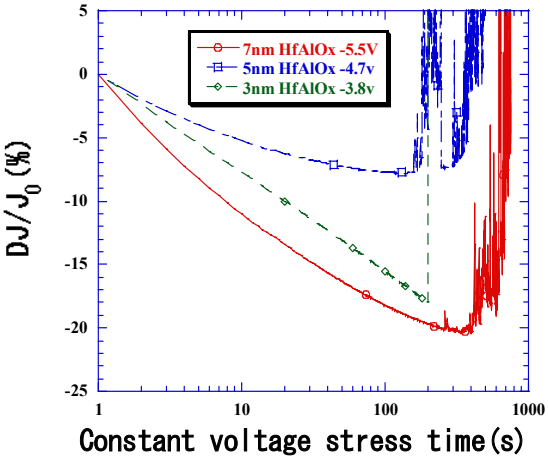

Fig.2 Time dependence of the current density decreasing during constant gate voltage stress of MIS capacitors with different thickness of HfAlOx layer

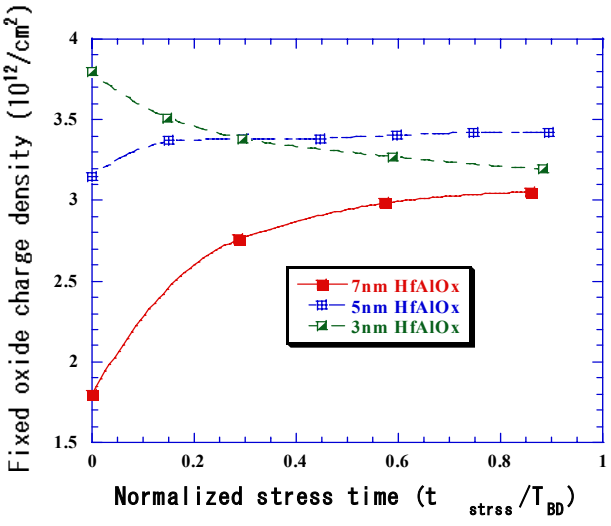

Fig.3 the variation of fixed oxide charge density as a function of stress time normalized by soft breakdown time for capacitors with different thickness of HfAlOx. The constant voltage stress was performed at 3.9MV/cm in HfAlOx layer.

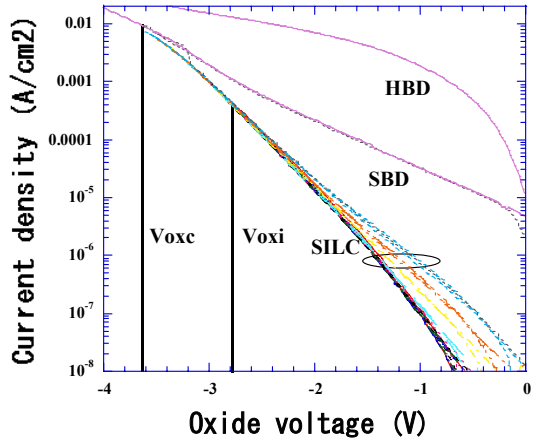

Fig.4 The leakage current as function of oxide voltage for the capacitance with 5nm $HfAlO_x$ layer.

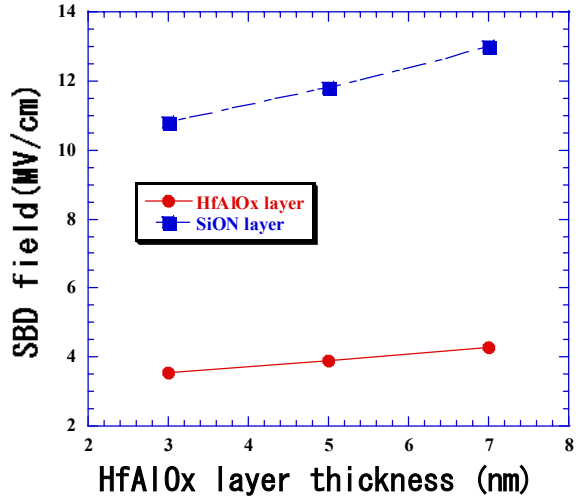

Fig.5 Soft breakdown field strength response to HfAlOx layer and SiON layer respectively for capacitors with different thickness of $HfAlO_x$ layer.

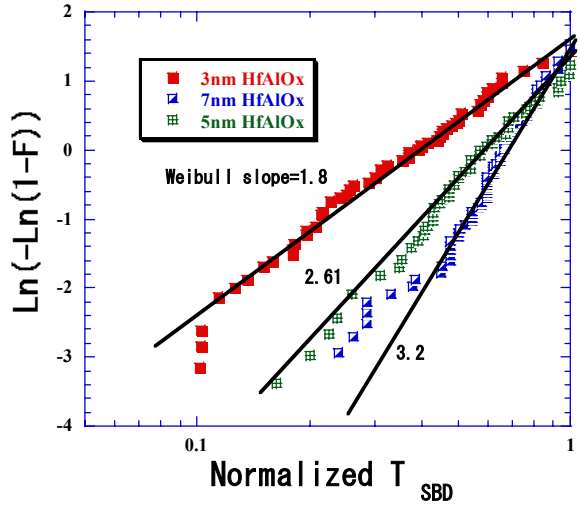

Fig.6 Normalized Weibull distribution of HfAlOx/SiON stack dielectric with different thickness of HfAlOx.

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OUTLINE

Back ground

Further increasing in the gate capacitance
Within an allowable gate leakage current
High-K gate dielectrics is required as the replacement of silicon oxide.

Electrical requirements for High-k transistor
- Stability after high temperature process
- Gate leakage current
- Uniformity and stable characteristics
- Reliability

HfAlOx
- Dielectric constant:~14
- Excellent thermal stability
  Against crystalization<1000 ^{0}C

Good candidate

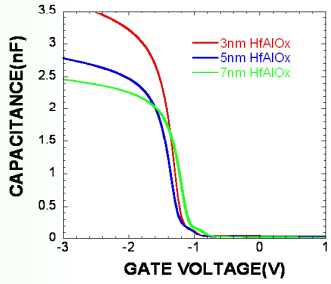
Our work focus on HfAlOx/SiON stack gate dielectrics and evaluated the electrical properties.

MIS capacitors fabrication

300mm p-Si(100) ~10ohm·cm^{-1}
Wet-Cleaning
Nitridation 700°C, NH3
Oxidation 850°C, N_2O/H_2 — 1.2nm SiON / P-Si(100)
ALCVD : $HfAlO_x$ [Hf/(Al+Hf)=0.3] (3~7nm)
Precursors
$Hf[N(C_2H_5)CH_3]_4$,
$Al(CH_3)_3$, H_2O,
$HfAlO_x$ / P-Si(100) — 1.2nmSiON
PDA : 0.2% O_2 in N_2
800°C:5sec
900°C:5sec
1000°C:1sec
Aluminum electrode diameter 0.5mm — Al / $HfAlO_x$ / p-Si(100) — 1.2nm SiON

MEASUREMENTS
- I-V, C-V combining constant voltage stress (CVS)
  - Charge trapping
  - Breakdown field
  - TDDB characteristics

C-V characteristics and oxide equivalent thickness



EOT

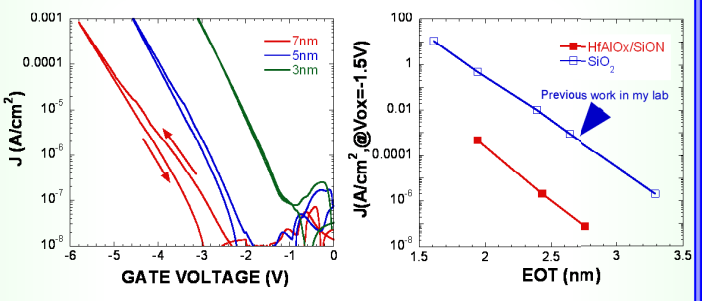
3nmHfAlOx/1.2nmSiON	1.9nm
5nmHfAlOx/1.2nmSiON	2.4nm
7nmHfAlOx/1.2nmSiON	2.9nm

PERMITTIVITY

HfAlOx	SiON
14	4.6

The C-V curves were measured at 1KHz.

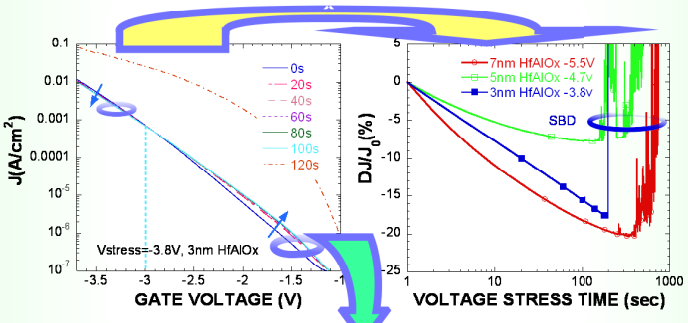
Leakage current characteristics



The leakage current is lower than that of SiO_2 with the same EOT about 3 orders

The hysteresis of current corresponds to the defects in HfAlOx/SiON stack layer

Leakage current characteristics during CVS

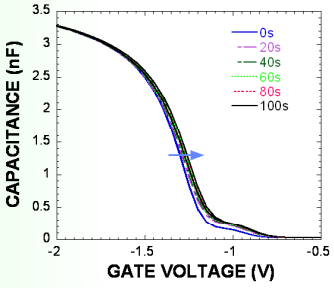


Trap assisted tunneling process like SILC in silicon oxide

Electron trapping was generated during negative constant voltage stress

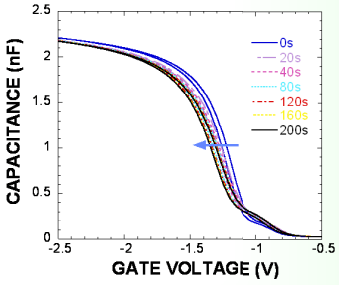
C-V characteristics during CVS

Capacitor with 3nm-thick HfAlOx



Positive shift of C-V curve for capacitor with 3nm-thick HfAlOx at -3.8V

Capacitor with 7nm-thick HfAlOx

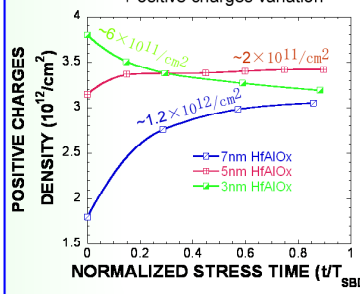


Negative shift of C-V curve for capacitor with 7nm-thick HfAlOx at -5.5V

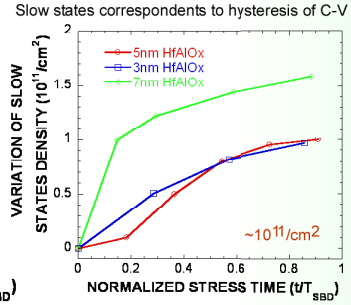
Variation of positive charges and slow states during CVS

Constant voltage stress at -3.8MV/cm in HfAlOx

Positive charges variation



Slow states correspondents to hysteresis of C-V

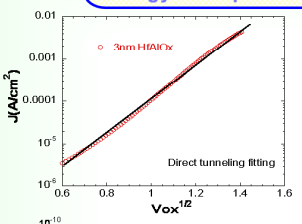


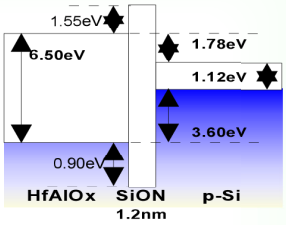
The generation of positive charges was decreased as decrease of HfAlOx layer thickness

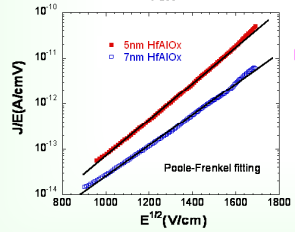
The positive charges was decreased for the capacitor with 3nm-thick HfAlOx

The variation of C-V hysteresis after constant voltage stress corespondents to ~10^{11}/cm^2 slow states for all the cases

Energy band profile and conduction mechanism



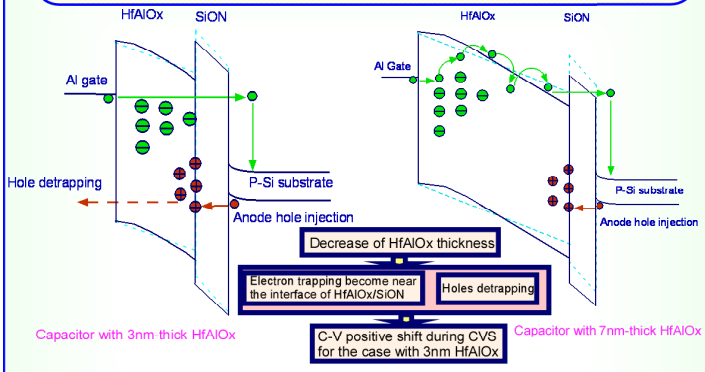




Energy band profile for HfAlOx/SiON/Si(100) measured by O1s energy loss spectra and valence band spectra

Direct tunneling conduction mechanism for the case with 3nm-thick HfAlOx and Poole-Frenkel conduction mechanism for with 5~7nm thick HfAlOx are confirmed by DT and PF fitting

Breakdown model using charge trapping in different spatial sites

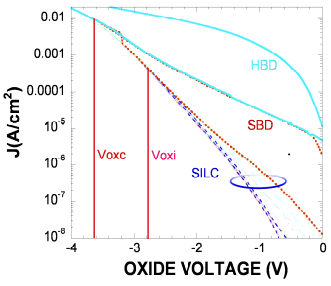


The electron trapping and Holes trapping were located at different spatial sites near Al Gate and interface of HfAlOx respectively to induce energy band distortion

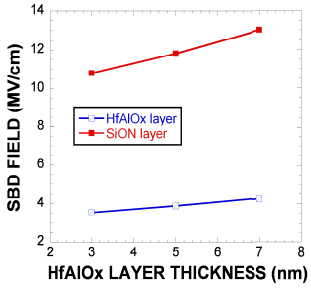
Energy band distortion and release energy due to combination of electron and holes in interface will induce the breakdown spots in interface and extend to High-k bulk, leading to breakdown

Soft breakdown field in the stack gate

Capacitance with 5nm-thick HfAlOx



SBD Field in HfAlOx and SiON respectively

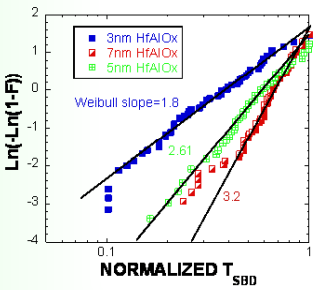


Theoretically predict breakdown field according to the experimental function E_{BD}=24.5(K)$^{-0.51}$ is 6.4MV/cm for HfAlOx

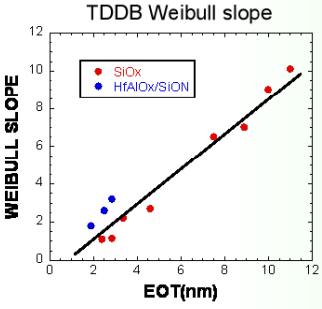
The stack dielectric breakdown was controlled by interfacial layer----SiON.

Thickness dependence of Weibull distribution

SBD Weibull distribution



TDDB Weibull slope



Weibull slope was increased as increase of HfAlOx layer thickness

Weibull slope is comparable to the silicon oxide with same EOT

Conclusions

Charge trapping

Electron trapping and net positive charges located in different spatial sites correspondence to High-k bulk and interface respectively.

Energy band distortion and release energy due to charge chapping and combination will induce the breakdown

Soft breakdown field

The interfacial layer SiON has a strong breakdown field (10~13MV/cm)

The HfAlOx layer breakdown field is only 3~4MV/cm

TDDB characteristics

The slope of Weibull plots for TDDB characteristics was obtained to be 1.8 or higher, which is comparable to the case of ultra-thin silicon oxide.

Acknowledgements

This work was supported in part by the high-k network project invested by selete.